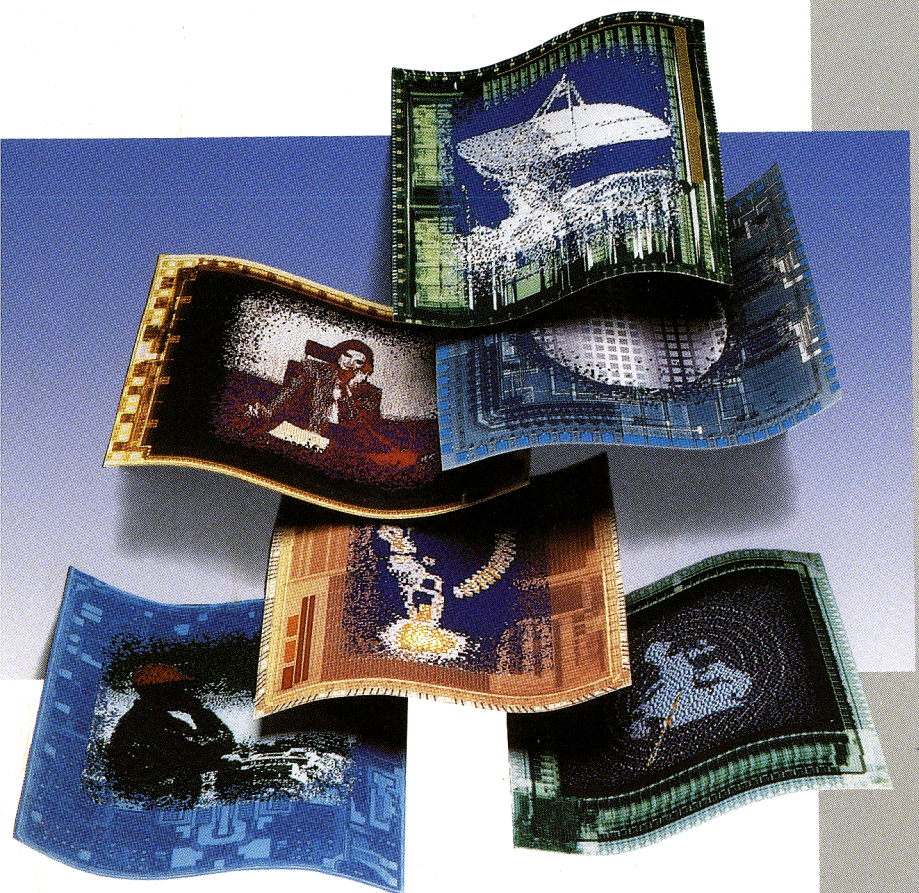
Professional Products

IC Handbook

May 1991



GEC PLESSEY

SEMICONDUCTORS

PROFESSIONAL PRODUCTS

IC Handbook

GEC PLESSEY

SEMICONDUCTORS

Contents

Foreword

The Professional Products IC Handbook replaces the Linear IC Handbook (Publication Number PS1973, September 1988) and the Frequency Dividers and Synthesisers IC Handbook (Publication Number PS1937, February 1988). It excludes certain specialist personal communications products which are now published in the Personal Communications IC Handbook (Publication Number PS2123, June 1990).

Pre-existing circuits are, of course, covered – as well as a range of new designs. Many of these incorporate the enhanced performance that results from the steady design and process improvements that have taken place. A good example would be the SL3522 Single-Chip Log Strip. This uses an advanced bipolar process with on-chip decoupling to give a 75dB dynamic range over the frequency range 100MHz to 600MHz – replacing at least four earlier generation ICs, reducing size, improving reliability and reducing overall system cost.

Many devices included in this Handbook also have extended operating temperature ranges and more package options, especially surface mount.

New products are continually under development and GEC Plessey Semiconductors' Sales Force always welcomes enquiries. Shortly, we will be announcing a new range of 5GHz frequency dividers, new higher frequency parallel and hard wire synthesisers up to 2GHz and a lower frequency single-chip log strip.

Product list, Linear Circuits

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +85°C	0°C to +70°C	A	B	C	BSS2	X	
SL360 G CM	2-transistor array				•					•	1-111
SL362 C CM	2-transistor array				•					•	1-111
SL521 A CM	140MHz log amp.	•								•	1-6
SL521 AB CM		•					•				
SL521 AC CM		•						•			
SL521 ABSS2 CM		•							•		
SL521 B CM	130MHz log amp.	•								•	1-6
SL521 BB CM		•					•				
SL521 C CM	100MHz log amp.	•								•	1-6
SL521 CB CM		•					•				
SL523 AC CM	Dual 100MHz log amp.	•						•			1-10
SL523 B CM		•								•	
SL523 BB CM		•					•				
SL523 C CM		•								•	
SL523 CB CM		•					•				
SL523 HB CM	Matched set of eight SL523s	•					•				1-10
SL531 AC CM	250MHz true log amp.	•						•			1-14
SL531 C CM		•								•	
SL531 CB CM		•					•				
SL532 AC CM	Low phase shift limiter	•									1-17
SL532 C CM		•								•	
SL532 CB CM		•					•				
SL541 B CM	High slew rate op amp.		•							•	1-70
SL541 B DG			•							•	
SL541 BB DG			•				•				
SL550 G DG	Low noise wideband amp.w. gain control		•							•	1-56
SL550 GB DG			•				•				
SL560 AC CM	300MHz low noise amp.	•						•			1-62
SL560 C CM		•								•	
SL560 C DP			•							•	
SL560 C LC		•								•	
SL560 CB CM		•					•				
SL560 CBSS2 CM		•							•		

NOTES

1. The last two characters of each ordering code specifies the package type, as described on page (xxi).
2. See detailed data sheet for guaranteed temperature range.
3. Screening levels: **A** is GPS Hi-Rel A, **B** is GPS HI-Rel B, **C** is MIL-STD 883C Class B, **BSS2** is BS9400 Level S2 and **X** is GPS Standard Product. See pages (xix) and (xx).

Product list, Linear Circuits (continued)

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +85°C	0°C to +70°C	A	B	C	BSS2	X	
SL561 AC CM	Ultra low noise preamplifier	•						•			1-89
SL561 B CM		•								•	
SL561 BB CM		•					•				
SL561 C DP			•							•	
SL610 C CM	RF/IF amplifier			•						•	1-127
SL610 CB CM				•			•				
SL611 C CM	RF/IF amplifier			•						•	1-127
SL611 CB CM				•			•				
SL612 C CM	RF/IF amplifier			•						•	1-127
SL612 CB CM				•			•				
SL621 C CM	AGC generator			•						•	1-130
SL621 CB CM				•			•				
SL623 C CM	AMSSB detector			•						•	1-133
SL623 CB CM				•			•				
SL640 C CM	Mixer			•						•	1-135
SL641 C CM	Mixer			•						•	1-135
SL952 NA DP[4]	UHF limiting amp.									•	1-67
SL952 NA DG[4]										•	
SL952 CB DP[4]							•				
SL1521 A CM	300MHz log amp.	•								•	1-20
SL1521 AB CM		•					•				
SL1521 C CM		•								•	
SL1521 CB CM		•					•				
SL1523 C CM	300MHz dual log amp.	•								•	1-23
SL1610 C DP	RF/IF amplifier			•						•	1-137
SL1611 C DP	RF/IF amplifier			•						•	1-137
SL1612 C DP	RF/IF amplifier			•						•	1-137
SL1613 C DP	Log IF strip amp.			•						•	1-25
SL1613 C MP				•						•	
SL1615 NA MP	Log IF strip amp.			•						•	1-28
SL1640 C DP	Mixer			•						•	1-140
SL1641 C DP	Mixer			•						•	

NOTE 4. Operating temperature range = 0°C to +65°C.

Product list, Linear Circuits (continued)

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +85°C	0°C to +70°C	A	B	C	BSS2	X	
SL2363 C CM	6-transistor array				•					•	1-113
SL2363 CB CM					•		•				
SL2364 C DC	6-transistor array				•					•	1-113
SL2364 C DP					•					•	
SL2364 C LC					•					•	
SL2364 C MP					•					•	
SL2364 CB DC					•		•				
SL2521 B LC	1.3GHz log amp.			•						•	1-32
SL2521 C LC	1GHz log amp.			•						•	1-43
SL3127 C DC	5-transistor array				•					•	1-115
SL3127 C DP					•					•	
SL3127 CB DC					•		•				
SL3127 A DG					•					•	
SL3145 C DC	5-transistor array				•					•	1-119
SL3145 C DP					•					•	
SL3145 C MP					•					•	
SL3145 CB DC					•		•				
SL3145 E DC					•					•	
SL3145 E DP					•					•	
SL3227 NA DC	5-transistor array				•					•	1-123
SL3227 NA DP					•					•	
SL3227 NA MP					•					•	
SL3245 NA DC	5-transistor array				•					•	1-125
SL3245 NA DP					•					•	
SL3245 NA MP					•					•	
SL3521 A BM	75dB log amp.	•								•	1-153
SL3521 AC BM		•						•			
SL3522 A MC	75dB log amp.	•								•	1-3
SL3522 AC MC		•						•			
SL6140 NA MP[5]	400MHz AGC amp									•	1-142
SL6140 A CM		•								•	
SL6140 B CM			•							•	
SL6140 AC CM		•						•			
SL6270 C CM	Gain-controlled microphone preamplifier/ VOGAD			•						•	1-146
SL6270 C DP				•						•	
SL6270 CB CM				•			•				
SL6270 NA DP				•						•	

NOTE 5. Operating temperature range = –30°C to +70°C.

Product list, Linear Circuits (continued)

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +85°C	0°C to +70°C	A	B	C	BSS2	X	
SL6310 C DG	500mW audio amp.			•						•	1-149
SL6310 C DP				•						•	
SL6310 NA MP				•						•	
SL6440 A DG	High level mixer	•								•	1-152
SL6440 C DP				•						•	
SL6601 C DG	FM IF/PLL/mixer			•						•	1-155
SL6601 C DP				•						•	
SL6601 C LC				•						•	
SL6700 A DG	AM IF and detector	•								•	1-161
SL6700 AB DG		•					•				
SL6701 A DG	AM IF and detector with noise blanker	•								•	1-165
SL6701 AB DG		•					•				
TAB1043 NA DP	Quad op amp.		•							•	1-75
ZN414Z[6]	AM radio receiver				•					•	1-169
ZN415E[6]	AM radio receiver				•					•	1-169
ZN416E[6]	AM radio receiver				•					•	1-169
ZN424P[6]	Gated op amp.				•					•	1-78
ZN459[6]	Ultra low noise wideband preamp.	•								•	1-93
ZN459CP[6]					•					•	
ZN460[6]	Ultra low noise wideband preamp.	•								•	1-102
ZN460AM[6]		•								•	
ZN460CP[6]					•					•	

NOTE 6. Package codes for ZNxxx types differ from GPS codes given on page (xxi) – see individual data sheets.

Product list, Frequency Synthesisers

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +70°C	0°C to +70°C	A	B	C	BSS2	X	
NJ8821 A DG	10MHz synthesiser, μP parallel interface, resettable counters	•								•	2-42
NJ8821 A GG		•								•	
NJ8821 AB DG		•					•				
NJ88C22 AA DG	10MHz synthesiser, μP serial interface, resettable counters	•								•	2-47
NJ88C24 AA DG	10MHz synthesiser, μP serial interface, non-resettable counters	•								•	2-52
NJ88C40 MA DG	200MHz single-chip synthesiser		•							•	2-27
NJ88C40 MA MP			•							•	
SP2001 B DG	100MHz direct frequency synthesiser (DFS)		•							•	2-32
SP2001 A DG		•								•	
SP2001 AA DG		•				•					
SP2001 B DG			•							•	
SP2001 A DG		•								•	
SP2001 AA DG		•				•					
SP2002 A AC	350/400MHz DFS	•								•	2-36
SP2002 B AC			•							•	
SP8853 A DG	1.3/1.5GHz low power single-chip synthesiser	•								•	2-3
SP8853 B DG			•							•	
SP8853 A HC		•								•	
SP8853 B HC			•							•	
SP8853 AC DG		•						•			
SP8853 AC HC		•						•			
SP8861 NA HP	1.3GHz low power single-chip synthesiser		•							•	2-15

Product list, 2-Modulus Dividers

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +70°C	0°C to +70°C	A	B	C	BSS2	X	
SP8720 A DG	300MHz ÷3/4	•								•	3-40
SP8720 B DG				•						•	
SP8720 AB DG		•					•				
SP8720 AC DG		•						•			
SP8740 A DG	300MHz ÷5/6	•								•	3-44
SP8740 B DG				•						•	
SP8740 AB DG		•					•				
SP8740 AC DG		•						•			
SP8741 A DG	300MHz ÷6/7	•								•	3-44
SP8741 B DG				•						•	
SP8741 AB DG		•					•				
SP8741 AC DG		•						•			
SP8691 A DG	200MHz ÷8/9	•								•	3-25
SP8691 B DG				•						•	
SP8691 AB DG		•					•				
SP8691 AC DG		•						•			
SP8743 A DG	450MHz ÷8/9	•								•	3-48
SP8743 AB DG		•					•				
SP8743 AC DG		•						•			
SP8743 B DG	500MHz ÷8/9			•						•	3-48
SP8695 A DG	200MHz ÷10/11	•								•	3-30
SP8695 B DG				•						•	
SP8695 AB DG		•					•				
SP8695 AC DG		•						•			
SP8695 ABSS2 DG		•							•		
SP8690 A DG	200MHz ÷10/11	•								•	3-25
SP8690 B DG				•						•	
SP8690 AB DG		•					•				
SP8690 AC DG		•						•			
SP8799 A DG	200MHz ÷10/11	•								•	3-73
SP8799 AC DG		•						•			
SP8647 A DG	250MHz ÷10/11	•								•	3-7
SP8647 B DG				•						•	
SP8647 AB DG		•					•				
SP8647 AC DG		•						•			
SP8647 ABSS2 DG		•							•		

Product list, 2-Modulus Dividers (continued)

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +70°C	0°C to +70°C	A	B	C	BSS2	X	
SP8643 A DG	350MHz ÷ 10/11	•								•	3-3
SP8643 AB DG		•					•				
SP8643 AC DG		•						•			
SP8685 A DG	500MHz ÷ 10/11	•								•	3-21
SP8685 B DG				•						•	
SP8685 AB DG		•					•				
SP8685 AC DG		•						•			
SP8782 A DG	1GHz ÷ 16/17, 32/33	•								•	3-52
SP8782 B DP			•							•	
SP8782 AC DG		•						•			
SP8789 A DG	200MHz ÷ 20/21	•								•	3-59
SP8789 AC DG		•						•			
SP8785 A DG	1GHz ÷ 21/22	•								•	3-55
SP8785 B DG				•						•	
SP8785 AA DG		•				•					
SP8786 A DG	1.3GHz ÷ 21/22	•								•	3-55
SP8786 B DG				•						•	
SP8786 AA DG		•				•					
SP8795 A DG	200MHz ÷ 32/33	•								•	3-66
SP8795 AC DG		•						•			
SP8797 A DG	225MHz ÷ 32/33	•								•	3-70
SP8793 A DG	200MHz ÷ 40/41	•								•	3-63
SP8793 AB DG		•					•				
SP8793 AC DG		•						•			
SP8716 A DG	520MHz ÷ 40/41	•								•	3-37
SP8716 AB DG		•					•				
SP8716 AC DG		•						•			
SP8718 A DG	520MHz ÷ 64/65	•								•	3-37
SP8718 AB DG		•					•				
SP8718 AC DG		•						•			
SP8792 A DG	200MHz ÷ 80/81	•								•	3-63
SP8792 AB DG		•					•				
SP8792 AC DG		•						•			
SP8719 A DG	520MHz ÷ 80/81	•								•	3-37
SP8719 AB DG		•					•				
SP8719 AC DG		•						•			
SP8710 A DG	225MHz ÷ 100/101	•								•	3-34
SP8710 B DP			•							•	

Product list, Fixed Modulus Dividers

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +70°C	0°C to +70°C	A	B	C	BSS2	X	
SP8604 A CM	300MHz ÷2	•								•	3-85
SP8604 B CM				•						•	
SP8604 AB CM		•					•				
SP8604 AC CM		•						•			
SP8602 A CM	500MHz ÷2	•								•	3-85
SP8602 B CM				•						•	
SP8602 AB CM		•					•				
SP8602 AC CM		•						•			
SP8607 A CM	600MHz ÷2	•								•	3-92
SP8607 B CM				•						•	
SP8607 AB CM		•					•				
SP8607 AC CM		•						•			
SP8605 A DG	1GHz ÷2	•								•	3-88
SP8605 B DG					•					•	
SP8605 AA DG		•				•					
SP8606 A DG	1.3GHz ÷2	•								•	3-88
SP8606 B DG					•					•	
SP8606 AA DG		•				•					
SP8822 A1 DG	1.3GHz ÷2	•								•	3-179
SP8822 B1 DG	1.6GHz ÷2		•							•	3-182
SP8812 A1 DG	1.6GHz ÷2	•								•	3-161
SP8812 B1 DG	2.0GHz ÷2		•							•	3-164
SP8802 A DG	3.3GHz ÷2	•								•	3-152
SP8802 AC DG		•						•			
SP8832 B DG	3.5GHz ÷2		•							•	3-200
SP8790 A CM	60MHz ÷4 (2-modulus extender)	•								•	3-146
SP8790 B CM				•						•	
SP8790 AB CM		•					•				
SP8790 AC CM		•						•			
SP8601 A CM	150MHz ÷4	•								•	3-81
SP8601 B CM				•						•	
SP8601 AB CM		•					•				
SP8601 AC CM		•						•			
SP8600 A CM	250MHz ÷4	•								•	3-77
SP8600 B CM				•						•	
SP8600 AB CM		•					•				
SP8600 AC CM		•						•			
SP8610 A DG	1GHz ÷4	•								•	3-95
SP8610 B DG					•					•	
SP8610 AB DG		•					•				
SP8610 AA DG		•				•					

Product list, Fixed Modulus Dividers (continued)

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +70°C	0°C to +70°C	A	B	C	BSS2	X	
SP8611 A DG	1.3GHz ÷ 4	•								•	3-95
SP8611 AB DG		•					•				
SP8611 AA DG		•				•					
SP8824 A1 DG	1.3GHz ÷ 4	•								•	3-185
SP8611 B DG	1.5GHz ÷ 4				•					•	3-95
SP8814 A1 DG	1.6GHz ÷ 4	•								•	3-167
SP8824 B1 DG	1.6GHz ÷ 4		•							•	3-188
SP8814 B1 DG	2.0GHz ÷ 4		•							•	3-170
SP8804 A DG	3.3GHz ÷ 4	•								•	3-155
SP8804 AC DG		•						•			
SP8835 B DG	3.5GHz ÷ 4		•							•	3-203
SP8620 A DG	400MHz ÷ 5	•								•	3-99
SP8620 B DG				•						•	
SP8620 AB DG		•					•				
SP8620 AC DG		•						•			
SP8794 A CM	60MHz ÷ 8 (2-modulus extender)	•								•	3-149
SP8794 B CM				•						•	
SP8794 AB CM		•					•				
SP8794 AC CM		•						•			
SP8670 A DG	600MHz ÷ 8	•								•	3-132
SP8670 B DG				•						•	
SP8670 AB DG		•					•				
SP8670 AC DG		•						•			
SP8735 B DG	600MHz ÷ 8 (binary outputs)				•					•	3-139
SP8828 A1 DG	1.3GHz ÷ 8	•								•	3-191
SP8678 B DG	1.5GHz ÷ 8				•					•	3-135
SP8678 M DG			•							•	
SP8818 A1 DG	1.6GHz ÷ 8	•								•	3-173
SP8828 B1 DG	1.6GHz ÷ 8		•							•	3-194
SP8818 B1 DG	2.0GHz ÷ 8		•							•	3-176
SP8808 A DG	3.3GHz ÷ 8	•								•	3-158
SP8808 AC DG		•						•			
SP8838 B DG	3.5GHz ÷ 8		•							•	3.206

Product list, Fixed Modulus Dividers (continued)

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +70°C	0°C to +70°C	A	B	C	BSS2	X	
SP8660 DP	150MHz ÷10			•						•	3-121
SP8660 A CM	150MHz ÷10	•								•	3-124
SP8660 B CM				•						•	
SP8660 AB CM		•					•				
SP8660 AC CM		•						•			
SP8660 ABSS2 CM		•							•		
SP8637 B DG	400MHz ÷10 (BCD outputs)				•					•	3-109
SP8635 B DG	600MHz ÷10 (BCD outputs)				•					•	3-109
SP8630 A DG	600MHz ÷10	•								•	3-106
SP8630 B DG				•						•	
SP8630 AB DG		•					•				
SP8630 AC DG		•						•			
SP8634 B DG	700MHz ÷10 (BCD outputs)				•					•	3-109
SP8665 B DG	1.0GHz ÷10				•					•	3-128
SP8668 B DG	1.5GHz ÷10				•					•	3-128
SP8830 A DG	1.5GHz ÷10	•								•	3-197
SP8830 B DG			•							•	
SP8830 AC DG		•						•			
SP8659 A CM	200MHz ÷16	•								•	3-117
SP8659 B CM				•						•	
SP8659 AB CM		•					•				
SP8659 AC CM		•						•			
SP8659 ABSS2 CM		•							•		
SP8650 A DG	600MHz ÷16	•								•	3-114
SP8650 B DG				•						•	
SP8650 AB DG		•					•				
SP8650 AC DG		•						•			
SP8657 A CM	200MHz ÷20	•								•	3-117
SP8657 B CM				•						•	
SP8657 AB CM		•					•				
SP8657 AC CM		•						•			
SP8657 ABSS2 CM		•							•		

Product list, Fixed Modulus Dividers (continued)

Type No. (boldface) with ordering code[1]	Brief description	Operating temperature range[2]				Screening level[3]					Page
		–55°C to +125°C	–40°C to +85°C	–30°C to +70°C	0°C to +70°C	A	B	C	BSS2	X	
SP8655 A CM	200MHz ÷ 32	•								•	3-117
SP8655 B CM				•						•	
SP8655 AB CM		•					•				
SP8655 AC CM		•						•			
SP8655 ABSS2 CM		•							•		
SP8755 A DG	1.2GHz ÷ 64	•								•	3-143
SP8755 B DG				•						•	
SP8755 AB DG		•					•				
SP8755 AC DG		•						•			
SP8629 DG	150MHz ÷ 100		•							•	3-102
SP8629 DP			•							•	

Product index – Linear Circuits

Logarithmic amplifiers

Type No.	Description	Supply voltage (V)	Supply current (mA)	Bandwidth (MHz) (typ.)	Noise figure (dB)	Gain (dB)	Page
SL3522	70dB dynamic range log/limiting amp.(1)	±5	I_{CC} = 25 I_{EE} = 150	40 (Video) 450 (RF)	10		1-3
SL521A	140MHz (min.) wideband log amp.	6	15	165	4	12	1-6
SL521B	130MHz (min.) wideband log amp.	6	15	165	4	12	1-6
SL521C	100MHz (min.) wideband log amp.	6	15	165	4	12	1-6
SL523	100MHz (min.) dual wideband log amp.	6	30	140	4	24 ± 1.4	1-10
SL531	250MHz (min.) true log amp.	9	17	500		10 ± 2	1.14
SL532	Low phase shift limiter	9	10	400	7	12 ± 2	1-18
SL1521	Wideband log amp.	5.2	15	280	6	12 ± 0.5	1-20
SL1523	Dual wideband log amp.	5.2	30	190	6	24 ± 3	1-23
SL1613	Wideband log IF strip amp.	6	15	145	4.5	12 ± 2	1-25
SL1615	Wideband log IF strip amp.	6	15	165	4	12 ± 1	1-18
SL2521B	1.3GHz dual wideband log amp.	6	80	1100	9	12	1-32
SL2521C	1.0GHz dual wideband log amp.	6	80	1000	9	12	1-43
SL3521	Hybrid 75dB dynamic range log/limiting amp.(2)	±5	I_{CC} = 25 I_{EE} = 150	40 (Video) 450 (RF)	10		1-53

NOTES
1. 30ns rise time; ± 0.75dB linearity
2. 14ns (typ.) rise time for 60dB step; ± 0.75dB linearity

Wideband amplifiers

Type No.	Description	Supply voltage (V)	Supply current (mA)	Bandwidth (MHz) (typ.)	Noise figure (dB)	Gain (dB)	Page
SL550	Low noise wideband amplifier with external gain control	6	11	125	2	42	1-56
SL560	Low noise amplifier	2-15	20	300	2	40	1-62
SL952	UHF limiting amplifier	5	70	1000		35	1-67

Operational amplifiers

Type No.	Description	Supply voltage (V)	Supply current	Bandwidth (MHz) (typ.)	Max. offset (mV)	Open loop gain (dB)	Page
SL541	High slew rate op. amp.	+ 12, –6	16mA	100	5	70	1-70
TAB1043	Quad programmable op. amp.	± 1.5 to ± 12	40μA to 2mA	0.05 to 4	5	95	1-75

Linear Circuit Selector (continued)

Low noise amplifiers

Type No.	Description	Noise figure (nV/√Hz)	Distortion (%)	Bandwidth (MHz)	Gain (dB)	Page
ZN424P	Gated linear amplifier	6	1.5	1	86	1-78
SL561	Ultra low noise preamplifier	0.8		6	60	1-89
ZN459	Ultra low noise wideband preamp.	0.8		15	60	1-93
ZN460	Ultra low noise wideband preamp.	0.8		6	50-60	1-102

Matched transistor arrays

Type No.	LV_{CEO} (V) Min.	Typ.	I_{CM} (mA)	Typ. cut-off frequency (GHz)	No. of Transistors	h_{FE} (min.)	Page
SL360	7	14	50	2.2	2	30 at 5mA	1-111
SL362	7	14	50	2.2	2	30 at 1mA	1-111
SL2363	6	9	12	5.0	6	20 at 8mA	1-113
SL2364	6	9	12	5.0	6	20 at 8mA	1-113
SL3127	15	25	20	1.6	5	40 at 1mA	1-115
SL3145	15	25	20	1.6	5	40 at 1mA	1-119
SL3227	6	9	12	3.0	5	40 at 1mA	1-123
SL3245	6	9	12	3.0	5	40 at 1mA	1-125

Radiocoms

Type No.	Description	Page
SL610, SL611, SL612	85MHz, 50MHz, 15MHz RF/IF amplifiers	1-127
SL621	AGC generator (from detected audio)	1-130
SL623	AM detector, AGC amplifier and SSB demodulator	1-133
SL640	Mixer (emitter follower output)	1-135
SL641	Mixer (open collector output)	1-135
SL1610, SL1611, SL1612	120MHz, 80MHz, 15MHz RF/IF amplifiers	1-137
SL1640	Mixer (emitter follower output)	1-140
SL1641	Mixer (open collector output)	1-140
SL6140	400MHz wideband AGC amplifier	1-142
SL6270	Gain controlled microphone preamplifier/VOGAD	1-146
SL6310	500mW switchable audio amplifier/op. amp.	1-149
SL6440	High level mixer	1-152
SL6601	FM IF, PLL detector (double conversion) and RF mixer	1-155
SL6700	IF amplifier and AM detector with noise blanker	1-161
SL6701	AM IF and detector (double conversion)	1-165
ZN414, ZN415, ZN416	AM radio receivers	1-169

Frequency Synthesiser Selector

Type No.	Description	Page
SP8853	1.3/1.5GHz low power single-chip bipolar frequency synthesiser	2-3
SP8861	1.3GHz low power single-chip bipolar frequency synthesiser	2.15
NJ88C40	200MHz single-chip CMOS frequency synthesiser	2.27
SP2001	100MHz direct frequency synthesiser (DFS), bipolar. Requires external DAC	2.32
SP2002	350/400MHz direct frequency synthesiser (DFS), bipolar. Dual DAC output	2.36
NJ8821	10MHz CMOS frequency synthesiser, parallel μP interface, resettable counters	2.42
NJ88C22	10MHz CMOS frequency synthesiser, serial μP interface, resettable counters	2.47
NJ88C24	10MHz CMOS frequency synthesiser, serial μP interface, non-resettable counters	2.52

The Quality Concept

Quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes (followed by strict control and on-going assessment) that quality products will be produced.

All designs conform to standard layout rules, all processes are thoroughly evaluated and all new piece part designs and suppliers are investigated before authorisation for production use.

The same basic procedures are used on all products up to and including device packing. It is only then that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures, all users benefit; the high reliability user gains the advantage of scale (hence improving thr confidence factor in the quality achieved), while the volume user gains from the benefits of basic high reliability design concepts.

GEC Plessey Semiconductors (GPS) have the following factory approvals:

BS9000
AQAP1
BS9450 (Capability Approval)
MIL-STD-883C Class B (In conformance with the requirements of MIL-STD-883C Notice 11, paragraph 1.2.1)
DESC (Department of Electronics Supply Center - device approvals)

Screening

Different screening procedures are carried out by GPS; a brief description of the differences involved are set out in Tables 1 and 2.

Table 1

Stage/ operation	Standard product	GPS Hi-rel A	GPS Hi-rel B	MIL-STD-883C Class B	BSS2 BS9400 Level S2	MIL-STD-883C Class S(4)
Wafer-fab						Wafer-lot accept Method 5007
Probe test	100%	100%	100%	100%	100%	100%
Visual inspect chips	Usually 2010 Cond.B	2010 Cond.B	2010 Cond.B	2010 Cond.B	BS9400 1.2.10 Cond.B(1)	2010 Cond.A
Assemble						Includes 100% bond pull
Screen	None	Method 5004 Class B	As Table 2	Method 5004 Class B	BS9400 1.2.9 Level B(2)	Method 5004 Class S
Test	100%	100%	100%	100%	100%	100%
Conformance testing	None	Method 5005 Class B Group A Group B Group C Group D	None	Method 5005 Class B Group A Group B Group C Group D	BS9400(3) Group A Group B Group C Group D	Method 5005 Class S Group A Group B Group C Group D

NOTES

1. Visual inspection BS9400 1.2.10 Cond. B is similar to MIL-STD 883 Method 2010 Cond. B.
2. Screening BS9400 1.2.9 Level B is equivalent to MIL-STD-883 Method 5004 Class B EXCEPT it does not include 100% hot and cold test.
3. Conformance testing BS9400 is similar to MIL-STD-883 Class B EXCEPT:
   Group A does not necessarily include hot and cold testing
   Group B does include 160 hour operating life test
   Group C does include 2000 hour operating life test and hot and cold testing
   Group D only usually includes 8000 hour life test and dimension checks.
4. MIL-STD-883C Class S/ESA SCC9000: GPS has supplied numerous devices to customer specifications for Space and Satellite applications. Please contact your local GPS sales office for information.

Table 2

Stage/operation	GPS Hi-rel B (References are to MIL-STD-883C)	MIL-STD-883C Class B Method 5004(5)
Internal Visual	Method 2010 Test Condition B 100%	Method 2010 Test Condition B 100%
Stabilisation Bake	Method 1008 24Hrs at Condition C 100%	Method 1008 24Hrs at Condition C 100%
Temperature Cycling	Method 1010 Test Condition C 100%	Method 1010 Test Condition C 100%
Constant Acceleration	Method 2010 Condition E Y1 only 100%	Method 2010 Condition E Y1 only 100%
Visual Inspection	-	100%
Initial Electrical	Those parameters requiring Delta calculations. 100%	Those parameters requiring Delta calculations. 100%
Burn-In	Method 1015 160Hrs at 125°C min. 100%	Method 1015 160Hrs at 125°C min. 100%
Post Burn-In Electrical Test	Full Electrical Test to Guarantee datasheet. 100%	Those parameters requiring Delta calculations. 100%
PDA Calculation	5% max. All lots	5% max. All lots
Final Electrical Test	Done as Post Burn-In Test. 100%	Full Group A tests as Method 5005 100%
Seal (a) Fine Seal (b) Gross	Method 1014 100%	Method 1014 100%
Qualification/Quality Conformance Test	-	Method 5005 Class B Samples as necessary
External Visual	GPS Spec. sample	Method 2009 100%

NOTE 5. See Section 5 for further information.

Package Codes

Package codes for the integrated circuits detailed in this handbook are given below. Dimensioned outline drawings are given in Section 6.

Code	Type	Description
AC	PGA	Pin Grid Array, multi-layer ceramic, metal sealed lid, through board.
BM	Box Metal	Hermetic metal package for hybrid circuits.
CM	TO-n	Cylindrical multi-lead metal can.
DC	DILMON	Dual-in-line, multi-layer ceramic, sidebrazed leads, metal sealed lid, through board.
DG	CERDIP	Dual-in-line, ceramic body, Alloy 42 leadframe, glass sealed, through board.
DP	PLASDIP	Dual-in-line, copper or Alloy 42 leadframe, plastic moulded, through board.
GG	Flatpack	Glass sealed ceramic flatpack, leads on four sides, surface mount.
HG	Quad Cerpack	Glass sealed ceramic chip carrier, J-formed leads on four sides, surface mount.
HP	PLCC	Plastic moulded chip carrier, J-formed leads on four sides, surface mount.
LC	Leadless Chip Carrier	Four sided, leadless, multi-layer ceramic, metal sealed lid, surface mount.
MC	Small Outline	Dual-in-line, multi-layer ceramic, brazed 'Gullwing' formed leads, metal sealed lid, surface mount.
MP	Small Outline	Dual-in-line, plastic moulded, 'Gullwing' formed leads, metal sealed lid, surface mount.

Section 1

Technical Data: Linear circuits

MIL-STD-883C Class B

Many of the integrated circuits detailed in this section are available screened in conformance with MIL-STD-883C Class B and are identified in their ordering codes by the letters **AC** immediately following the device type number. Separate data sheets for these circuits are available from your local GEC Plessey Semiconductors Sales Office.

SL3522

500MHz 75dB LOGARITHMIC / LIMITING AMPLIFIER

The SL3522 is a monolithic seven-stage successive detection logarithmic amplifer integrated circuit for use in the 100MHz to 600MHz frequency range. It features an on-chip video amplifer with provision for external adjustment of log slope and offset. It also features a balanced RF output. The SL3522 operates from supplies of ±5V. The device is also available as SL3522AC, screened to MIL-STD 883C Class B - contact GPS sales outlet for separate datasheet.

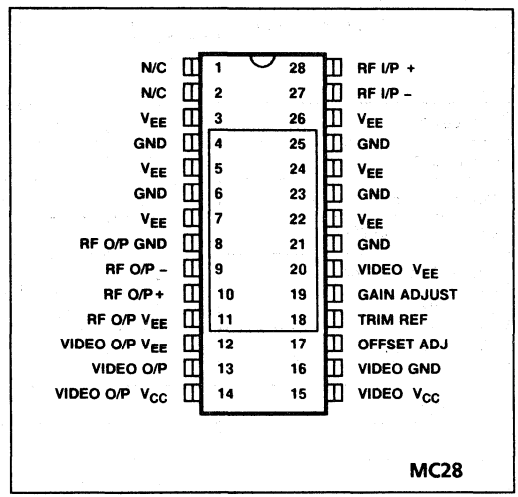


Fig.1 Pin Connections - top view

FEATURES

- 75dB Dynamic Range
- ±0.75 dB Log/Lin Accuracy
- Adjustable Log Slope and Offset
- 0dBm RF Limiting Output
- 70dB Limiting Range
- 2V Video Output
- Low Power (Typ. 1W)
- Full Military Temperature Range: -55°C to +125°C

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised Receiver
- Monopulse Radar
- Instrumentation

ORDERING INFORMATION

SL3522 A MC
SL3522 AC MC
SL3522 NA 1C (RF probe-tested bare die)

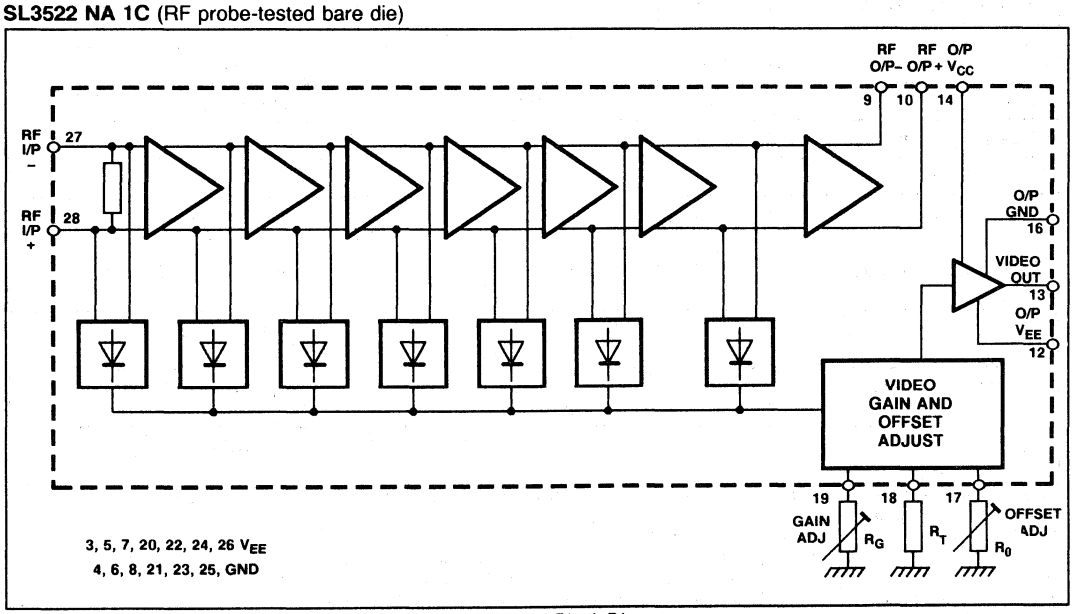


Fig.2 Functional Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

V_{CC} + 5V ± 10%, V_{EE} -5V ± 10%, $T_{mounting\ base}$ -55°C to + 125°C

Parameter	Pin	Value			Units	Conditions
		Min	Typ	Max		
QUIESCENT Positive Supply Current, I_{CC}	14, 15		25	35	mA	V_{CC} = + 5.0V
QUIESCENT Negative Supply Current, I_{EE}	3,5,7,11,12 20,22,24, 26		150	175	mA	Note 5
			180	210	mA	Note 6
Frequency Range	28, 27	100		500	MHz	Note 4
Input Level				+ 15	dBm	Without Damage
Noise Figure			10		dB	
Tangential Sensitivity	28, 27		-76		dBm	
Video Output Range	13			2	VDC	
Video Slope	13	19		21	mV/dB	Note 1.
Video Bandwidth	13	30	40		MHz	Critically Damped Transient Response
Rise Time	13		22	25	ns	Settled to within + /-0.7%
Rise Time	13		14		ns	10% to 90% (60dB step)
Linearity	13	- 0.75		+ 0.75	dB	Deviation from best fit straight line Note 1.
Video Output Impedance	13			10	Ω	
Video Load Impedance	13		200		Ω	Max Cap = 25pF
Input VSWR	13	1	1.5	2		50Ω System
RF Limiting Amp Output Impedance	9,10		50		Ω	
Limited Output Level	9,10		0		dBm	R_o = 50Ω
RF BW	9,10		450		MHz	Note 3
RF Limiting Range	9,10		70		dB	Note 7
Alignment Trim Ref.	18		-550		mV	Note 2
Phase Variation	27, 28 9, 10		15		Degrees pk-pk	T_{AMB} = 25°C f = 325MHz
Phase Tracking between Units	27, 28 9, 10		3			- 60dBm to + 10dBm
Video Offset ADJ Range	13	-0.5		+ 1	V	R_G = 1kΩ to 2.2kΩ R_T = 1.5kΩ
Log Slope Adjust Range	13		± 20		± %	R_G = 1kΩ to 2.2kΩ R_T = 1.5kΩ
Nominal Log Slope	13		20		mV/dB	R_G = 1.5kΩ R_T = 1.5kΩ

Note 1. Measured between -68dBm and + 7dBm over supply, temperature and frequency ranges after alignment using R_G.
Note 2. Nominal voltage on pin 8.
Note 3. Input power = -80dBm. Temperature = 25°C
Note 4. Frequency range over which specified linearity and dynamic range guaranteed.
Note 5 Measured with RF O/P BUFFER powered down - Pin 8 ISOLATED from 0V (GND). V_{EE} = -5.0V
Note 6 Measured with RF O/P BUFFER powered up - Pin 8 CONNECTED to 0V (GND). V_{EE} = -5.0V
Note 7 -60dBm to + 10dBm for ± 1dB change in O/P

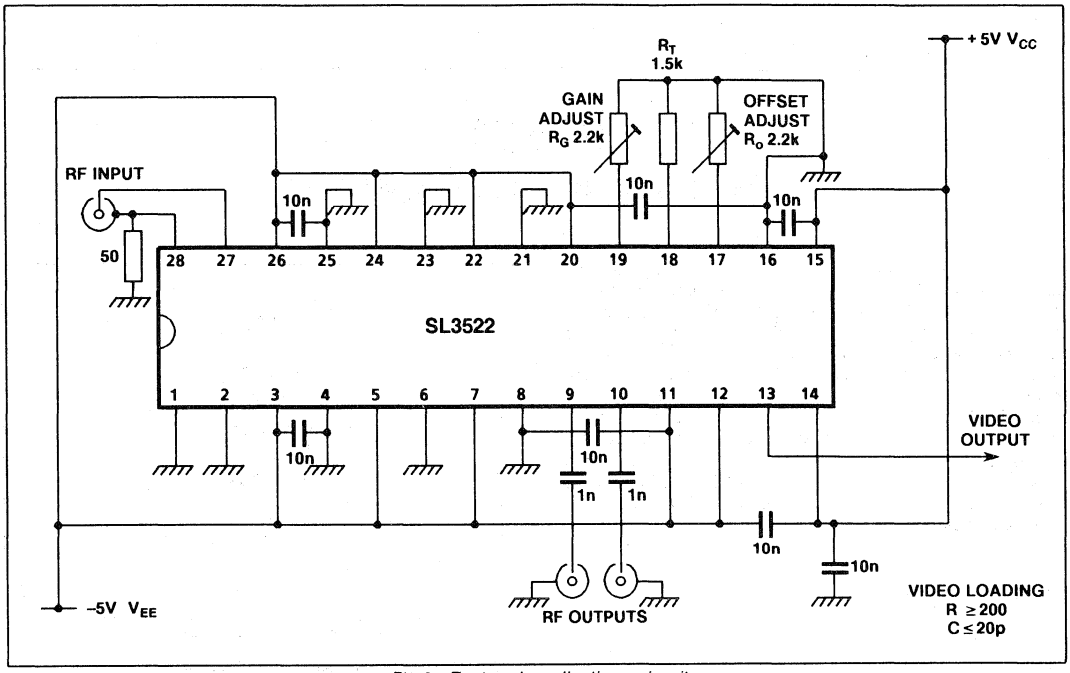


Fig.3 Test and applications circuit

APPLICATION NOTES

Like all high gain, high frequency circuits, some care is required in layout of the SL3522. However the use of on-chip decoupling leads to a high degree of stability, thus easing the requirements. Nevertheless, it is advised that the SL3522 be mounted on a ground plane, and the 10nF bypass capacitors be mounted close to the pins of the device. They should be surface mount RF quality low loss chip capacitors.

Layout should be such that capacitance on pin 18 (reference) is minimised. It is recommended that the resistors used are similar types, so that minimum parameter drift is introduced by differences in temperature coefficients.

Although the RF outputs have DC blocking capacitors shown, they may be operated with DC load to ground. However, a DC offset of about –400mV will be obtained. The output loads must be balanced, so that if only a single ended output is required, the other output must be provided with a similar load. Driving highly reactive SWR loads is not recommended for stability reasons.

Video Output

Although the video output impedance is low (about 10Ω), the available current is limited such that the load should not be less than 200Ω in parallel with no more than 20pF if the full video transient performance is to be obtained.

Gain and Offset Trimming

Gain and offset trimming are unilaterally independent. Adjustment of gain has an effect on offset, but not vice-versa. Because the gain and offset controls provide internal control dependent upon their difference from the trim reference resistor R_T, differing temperature coefficients in these resistors will lead to variations in gain and offset over the temperature range.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±6.0V
Storage temperature	-65°C to + 175°C
Junction temperature	+ 175°C
Thermal resistance:	
Die-to-case	15°C/W
Die-to-ambient	50°C/W
Applied DC voltage to RF input	±50mV
Applied RF power to RF input	+ 15dBm

Further Applications and Characterisation Data for this product may be found On pages 4-72 to 4-77.

SL521

140MHz WIDEBAND LOG AMPLIFIER

The SL521A, B and C are bipolar monolithic integrated circuit wideband amplifiers, intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 100MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL521 is typically 12dB (4 times). The SL521A, B and C differ mainly in the tolerance of voltage gain and upper cut-off frequency.

The device is also available as the SL521AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

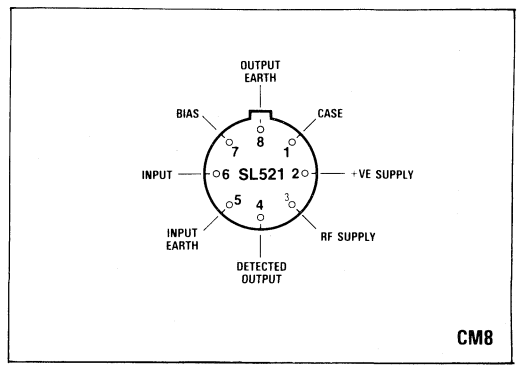


Fig.1 Pin connections - bottom view

FEATURES

- Well-Defined Gain
- 4dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 165MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

ORDERING INFORMATION

SL521 A CM
SL521 B CM
SL521 C CM
SL521 AB CM
SL521 BB CM
SL521 CB CM
SL521 AC CM
SL521 A BSS2 CM

ABSOLUTE MAXIMUM RATINGS (Non-simultaneous)

Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+9V

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity better than 1dB

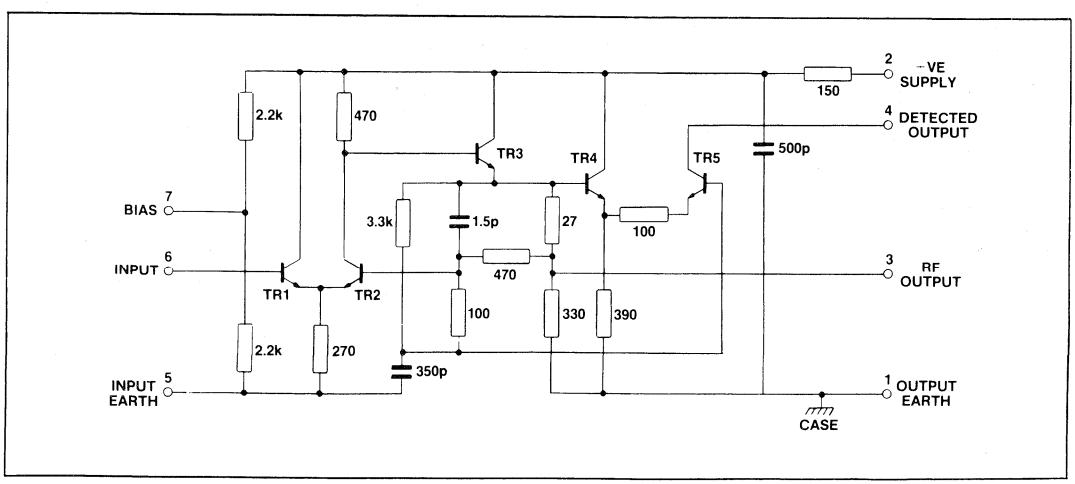


Fig.2 Circuit diagram SL521

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature = +22°C ± 2°C
Supply voltage = +6V
DC connection between input and bias pins.

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 30MHz	A	11.5		12.5	dB	10 ohms source, 8pF load
	B	11.3		12.7	dB	
	C	11.0		13.0	dB	
Voltage gain, f = 60MHz	A	11.3		12.7	dB	
	B	11.0		13.0	dB	
	C	10.7		13.3	dB	
Upper cut-off frequency (Fig. 3)	A	150	170		MHz	10 ohms source, 8pF load
	B	140	170		MHz	
	C	130	170		MHz	
Lower cut-off frequency (Fig. 3)	A B C		5	7	MHz	10 ohms source, 8pF load
Propagation delay	A B C		2		ns	
Maximum rectified video output current (Fig. 4 and 5)	A	1.00		1.10	mA	f = 60MHz, 0.5V rms input
	B	0.95		1.15	mA	
	C	0.90		1.20	mA	
Variation of gain with supply voltage	A B C		0.7		db/V	
Variation of maximum rectified output current with supply voltage	A B C		25		%/V	
Maximum input signal before overload	A B C	1.8	1.9		V rms	See note below
Noise figure (Fig. 6)			4	5.25	dB	f = 60MHz, Rs = 450 ohms
Supply current	A	12.5	15.0	18.0	mA	
	B	12.5	15.0	18.0	mA	
	C	11.5	15.0	19.0	mA	
Maxiumum RF output voltage			1.2		Vp-p	

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction to TR1 on peaks.

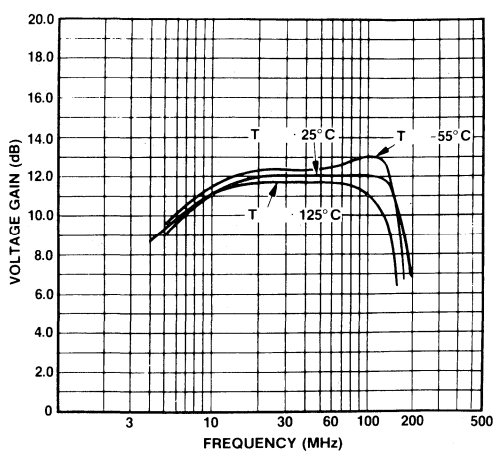


Fig.3 Voltage gain v. frequency (typical)

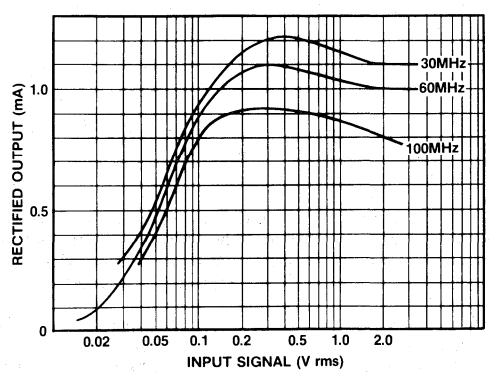


Fig.4 Rectified output current v. input signal (typical)

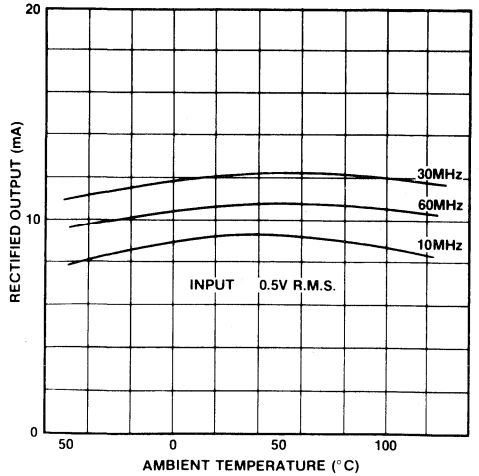


Fig.5 Maximum rectified output current v. temperature (typical)

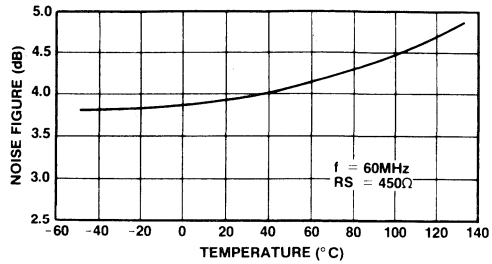


Fig.6 Noise figure v. temperature (typical)

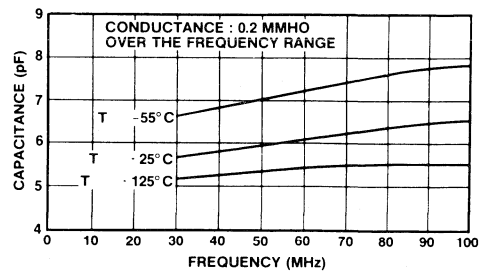


Fig.7 Input admittance with open-circuit output (typical)

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig.8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig.9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required. Alternative arrangements may be derived, based on the parasitic parameters given.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common ground lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

The 500pF supply decoupling capacitor has a resistance of, typically, 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see Absolute Maximum Ratings).

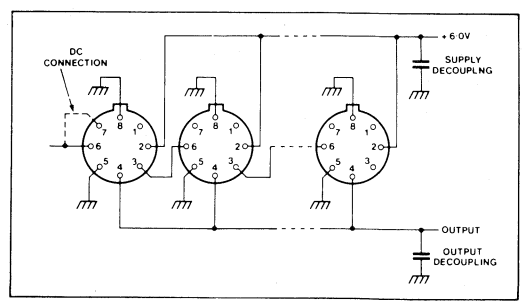


Fig.8 Direct coupled amplifiers

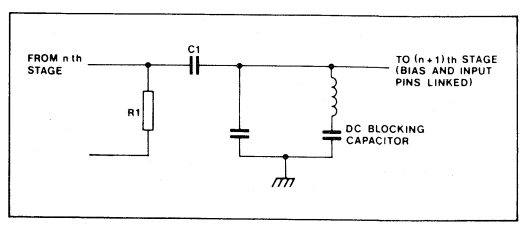


Fig.9 Suitable interstage tuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required; the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guesswork.

$$\frac{\widetilde{I_4}}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals).

$$\frac{V_6}{V_4} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6 \text{ mmhos (f = 10MHz)}$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 6 joined to pin 7 and fed from 300Ω source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}\left[\frac{V_6}{V_2}\right]_a\left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6dB/octave

SL523

100MHz DUAL WIDEBAND LOG AMPLIFIER

The SL523B and C are wideband amplifiers for use in successive detection logarithmic IF strips operating at centre frequencies between 10 and 100MHz. They are pin-compatible with the SL521 series of logarithmic amplifiers and comprise two amplifiers, internally connected in cascade. Small signal voltage gain is 24dB and an internal detector with an accurate logarithmic characteristic over a 20dB range produces a maximum output of 2.1mA. A strip of SL523s can be directly coupled and decoupling is provided on each amplifier. RF limiting occurs at an input voltage of 25mV RMS but the device will withstand input voltages up to 1.8V RMS without damage.

The SL523HB is supplied in matched sets of eight devices. The gain at 60MHz of the devices in the set is matched to 0.75dB. In all other respects the device is identical to an SL523B. This selection enables very precise log strips to be produced. Supplied only to Plessey Class B screening including burn-in.

The device is also available as the SL523AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- Small Size/Weight
- Lower Power Consumption
- Readily Cascadable
- Accurate Logarithmic Detector Characteristic

ABSOLUTE MAXIMUM RATINGS

(Non simultaneous)

Storage temperature range	-55°C to +175°C
Operating temperature range	-55°C to +125°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	+9V

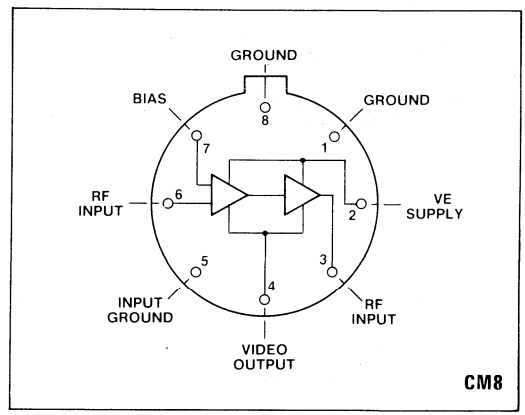


Fig.1 Pin connections (view from beneath)

QUICK REFERENCE DATA

- Small Signal Voltage Gain: 24dB
- Detector Output Current: 2.1mA
- Noise Figure: 4dB
- Frequency Range: 10-100MHz
- Supply Voltage +6V
- Supply Current 30mA

ORDERING INFORMATION

SL523 AC CM
SL523 B CM
SL523 BB CM
SL523 C CM
SL523 CB CM
SL523 HB CM
5962-89803: DESC approved

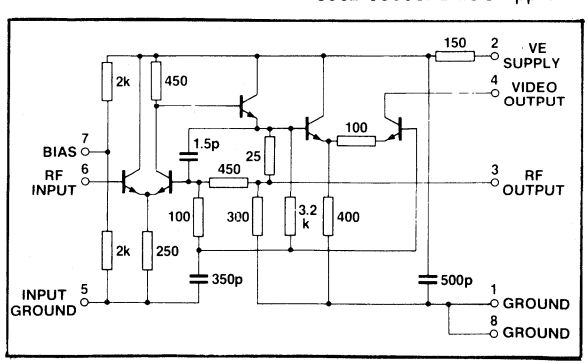


Fig.2 Circuit diagram (one amplifier)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Ambient temperature = 22°C ± 2°C; Source impedance = 10Ω; Supply voltage = +6V; Load impedance = 8pF; Frequency = 60MHz; DC connection between Pins 6 and 7

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Small signal voltage gain	B,HB	22.6	24	25.4	dB	Frequency = 30MHz
	C	22	24	26	dB	
Small signal voltage gain	B,HB	22	24	26	dB	Frequency = 60MHz
	C	21.4	24	26.6	dB	
Gain variation (set of 8)	HB		0.5	0.75	dB	Frequency = 60MHz
Upper cut-off frequency	B,C & HB	120	150		MHz	
Lower cut-off frequency	B,C & HB		10	15	MHz	
Propagation delay	B,C & HB		4		ns	
Maximum rectified video	B,HB	1.9	2.1	2.3	mA	V_{IN} = 0.5V RMS
output current	C	1.8	2.1	2.4	mA	
Maximum input signal before overload	B,C & HB	1.8	1.9		V RMS	
Noise figure			4	5.25	dB	Source impedance 450Ω
Supply current	B,HB	25	30	36	mA	
	C	23	30	38	mA	
Maximum RF output voltage	B,C & HB		1.2		V p-p	

OPERATING NOTES

The amplifier is designed to be directly coupled (see Fig.5).

The fourth stage in an untuned cascade will give full output on the broad band noise generated by the first stage.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The network chosen must give unity voltage gain at resonance to avoid distorting the log law. The typical value for input impedance is 500Ω in parallel with 5pF and the output impedance is typically 30Ω.

Although a 1nF supply line decoupling capacitor is included in the can an extra capacitor is required when the amplifiers are cascaded. Minimum values for this capacitor are: 2 stages - 3nF, 3 or more stages - 30nF.

In cascades of 3 or more stages care must be taken to avoid oscillations caused either by inductance common to the input and output earths of the strip or by feedback along the common video line. The use of a continuous earth plane will avoid earth inductance problems and a common base amplifier in the video line isolating the first two stages as shown in Fig.6 will eliminate feedback on the video line.

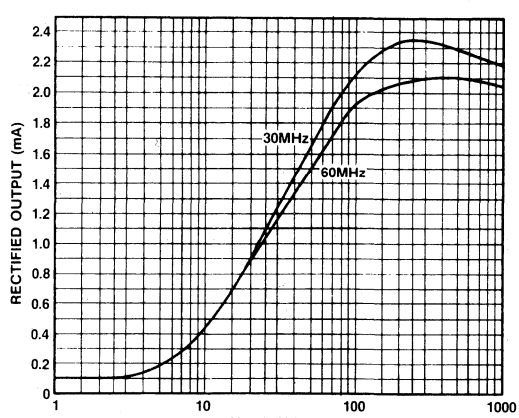


Fig.3 Rectified output current v. input signal (typical)

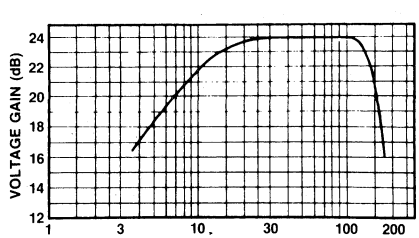


Fig.4 Voltage gain v. frequency (typical)

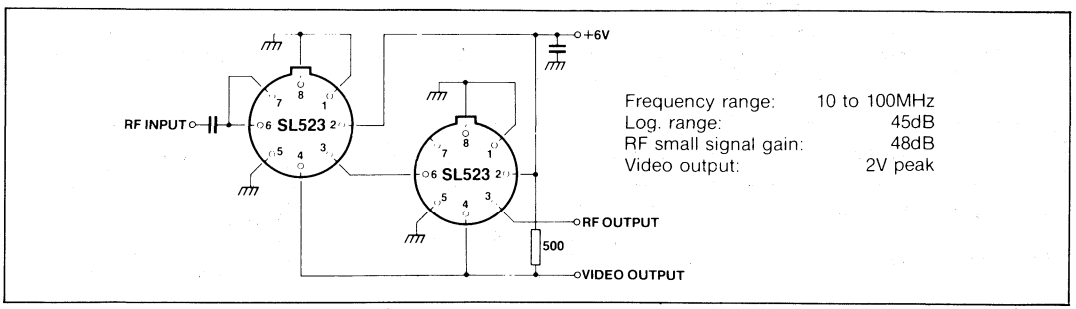


Fig.5 Simple log. IF strip

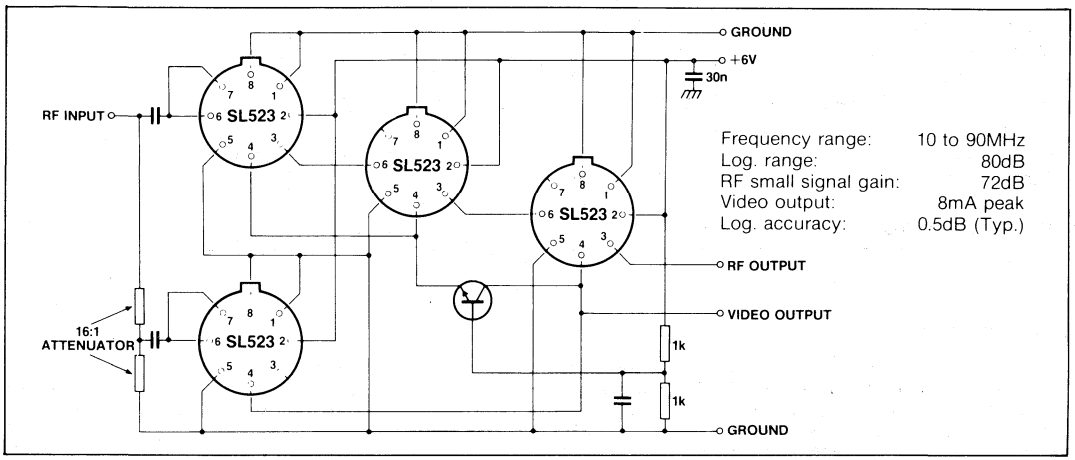


Fig.6 Wide dynamic range log. IF strip

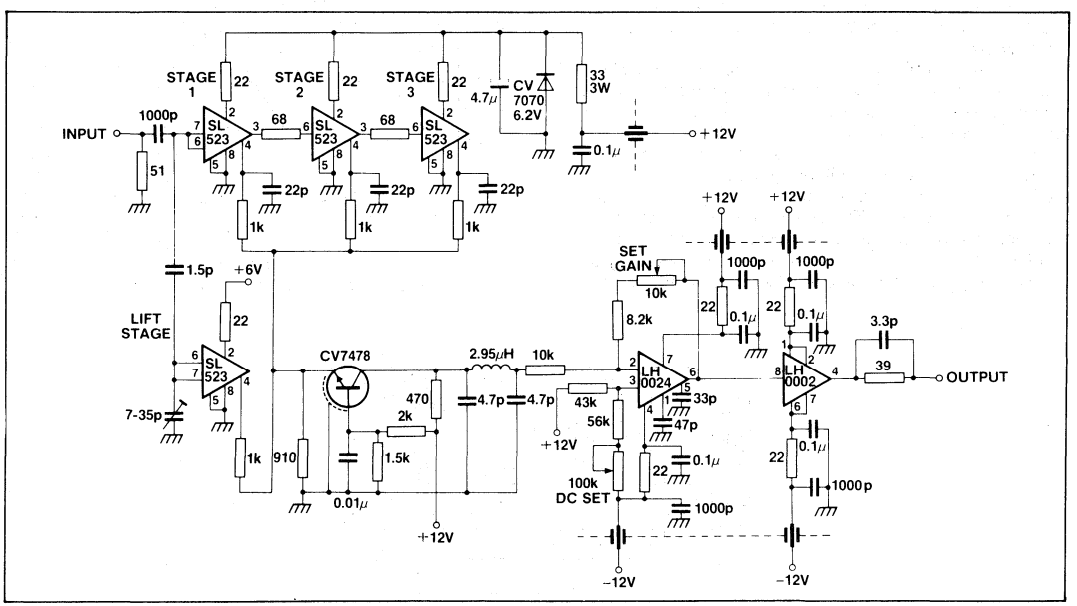


Fig.7 Wideband logarithmic amplifier

TYPICAL PERFORMANCE

Unselected SL523B devices were tested in a wideband logarithmic amplifier, described in RSRE Memo. No. 3027 and shown in Fig.7.

The amplifier consists of six logarithmic stages and two 'lift' stages, giving an overall dynamic range of greater than 80dB. The response and error curves were plotted on an RHG Log Test Set and bandwidth measurements were made with a Telonic Sweeper and Tektronix oscilloscope.

Fig.8 shows the dynamic range error curve and frequency response obtained. The stage gains of the SL523 devices used were as shown in Table 1.

Stages	fo (MHz)	Gain (dB)	Max. Deviation (dB)
1	60	24.123	
2	60	24.089	0.235
3	60	23.888	
Lift	60	24.086	

Table 1 Stage gains of SL523 used in performance tests

The input v. output characteristic (Fig.8a) is calibrated at 10dB/cm in the X axis and 1V/cm in the Y axis. 80dB of dynamic range was attained.

The error characteristic (Fig.8b) is calibrated at 10dB/cm in the X axis and 1dB/cm in the Y axis; this shows the error between the log. input v. output characterisitc and a mean straight line and shows that a dynamic range of 80dB was obtained with an accuracy of ±0.5dB.

As a comparison, the log amplifier of Fig.7 was constructed with randomly selected SL521Bs (two SL521Bs replacing each SL523B). Again, a dynamic response of 80dB was obtained (Fig.9a) with an accuracy of ±0.75dB (Fig.9b).

Bandwidth curves are shown in Figs.8c and 9c, where the amplitude scale is 2dB/cm, with frequency markers at 10MHz intervals from 20 to 100MHz. Using SL523Bs (Fig.8c), the frequency response at 90MHz is 4dB down on maximum and there is a fall-off in response after 50MHz. Fig.9c shows that the frequency response of the amplifier falls off more gradually after 40MHz but again the response at 90MHz is 4dB down on maximum.

These tests show that the SL523 is a very successful dual-stage log amplifier element and, since it is pin-compatible with the SL521, enables retrofit to be carried out in existing log amplifiers. It will be of greatest benefit however, in the design of new log amplifiers, enabling very compact units to be realised with a much shorter summation line.

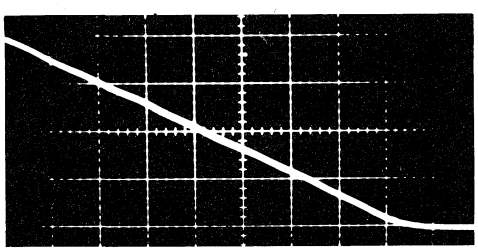


Fig.8a Input/output

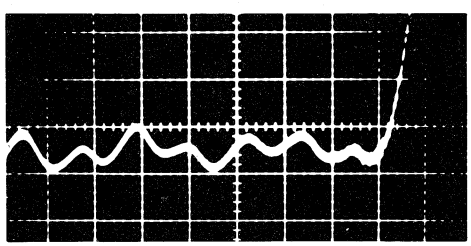


Fig.8b Error curve

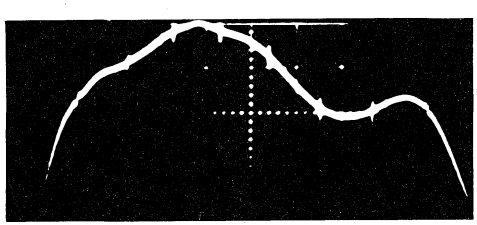


Fig.8c Frequency response, detected output

Fig.8 Characteristics of circuit shown in Fig.7 using SL523Bs

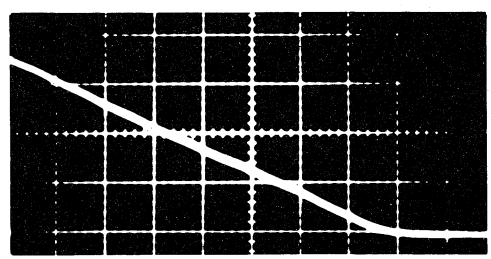


Fig.9a Input/output

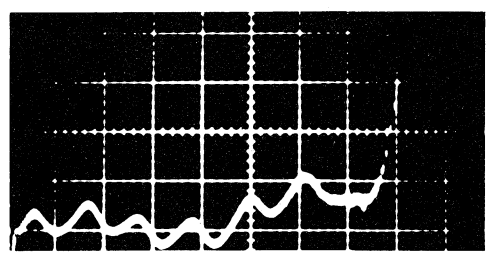


Fig.9b Error curve

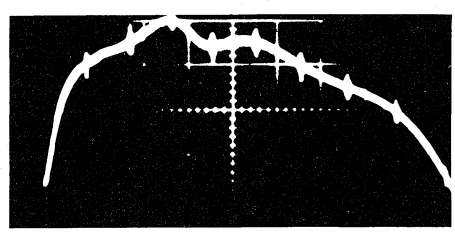


Fig.9c Frequency response, detected output

Fig.9 Characteristics of circuit shown in Fig.7 using SL521Bs

SL531

250MHz TRUE LOG IF AMPLIFIER

The SL531C is a wide band amplifier designed for use in logarithmic IF amplifiers of the true log type. The input and log output of a true log amplifier are at the same frequency i.e. detection does not occur. In successive detection log amplifiers (using SL521, SL1521 types) the log output is detected.

The small signal gain is 10dB and bandwidth is over 500MHz. At high signal levels the gain of a single stage drops to unity. A cascade of such stages give a close approximation to a log characteristic at centre frequencies between 10 and 200MHz.

An important feature of the device is that the phase shift is nearly constant with signal level. Thus any phase information on the input signal is preserved through the strip.

The device is also available as the SL531AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- Low Phase Shift vs Amplitude
- On-Chip Supply Decoupling
- Low External Components Count

APPLICATIONS

True Log Strips with: —

- Log Range 70 dB
- Centre frequencies 10 — 200 MHz
- Phase Shift ± 0.5 degrees / 10 dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+12 volts
Storage temperature range	-55 °C to +150 °C
Operating temperature range	-55 °C to +125 °C
	See operating notes
Max junction temperature	150 °C
Junction — ambient thermal resistance	220 °C/Watt
Junction — case thermal resistance	80 °C/Watt

CIRCUIT DESCRIPTION

The SL531 transfer characteristic has two regions. For small input signals it has a nominal gain of 10 dB, at large signals the gain falls to unity (see Fig 7). This is achieved by operating a limiting amplifier and a unity gain amplifier in parallel (see Fig 3). Tr1 and Tr4 comprise the long tailed pair limiting amplifier, the tail current being supplied by Tr5, see Fig 2. Tr2 and Tr3 form the unity gain amplifier the gain of which is defined by the emitter resistors. The outputs of both stages are summed in the 300 ohm resistor and Tr7 acts as an emitter follower output buffer. Important features are the amplitude and phase linearity of the unity gain stage which is achieved by the use of 5GHz transistors with carefully optimised geometries.

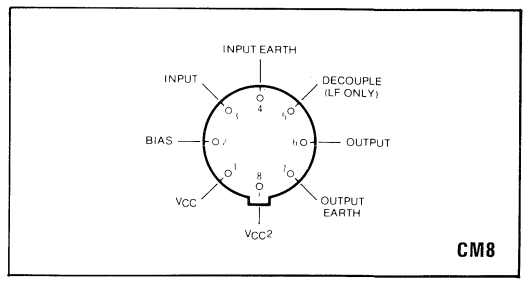


Fig. 1 Pin connections

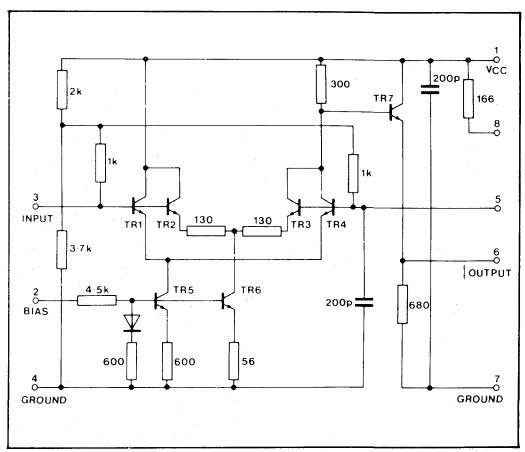


Fig. 2 Circuit diagram

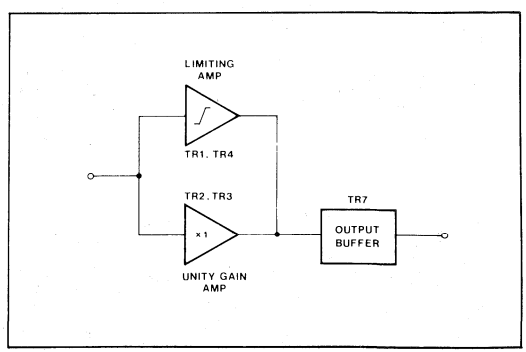


Fig. 3 Block diagram

ORDERING INFORMATION

SL531 AC CM
SL531 C CM
SL531 CB CM

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Test circuit Fig (4)
Frequency 60 MHz
Supply voltage 9 volts
Ambient temperature 22± 2°C

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Small signal voltage gain	8	10	12	dB	Vin = −30 dBm
High level slope gain	−1	0	+1	dB	
Upper cut off frequency	250	500		MHz	
Lower cut off frequency		3	10	MHz	−3dB w.r.t. ± 60 MHz
Supply current		17	25	mA	
Phase change with input amplitude		1.1	3	degrees	-Vin = 30 dBm to + 10 dBm
Input impedance	2.5pF parallel with 1kΩ				f = 10 - 200MHz
Output impedance	15Ω series with 25nH				

OPERATING NOTES

1. Supply Voltage Options

An on chip resistor is provided which can be used to drop the supply voltage instead of the external 180 ohms shown in the test circuit. The extra dissipation in this resistor reduces the maximum ambient operating temperature to 100°C. It is also possible to use a 6 volt supply connected directly to pins 1 and 2. Problems with feedback on the supply line etc may occur in this connection and RF chokes may be required in the supply line between stages.

2. Layout Precautions

The internal decoupling capacitors help prevent high frequency instability, however normal high frequency layout precautions are still necessary. Coupling capacitors should be physically small and be connected with short leads. It is most important that the ground connections are made with short leads to a continuous ground plane.

3. Low Frequency Response

The LF response is determined by the on chip capacitors. It can be extended by extra external decoupling on pins 5 and 1.

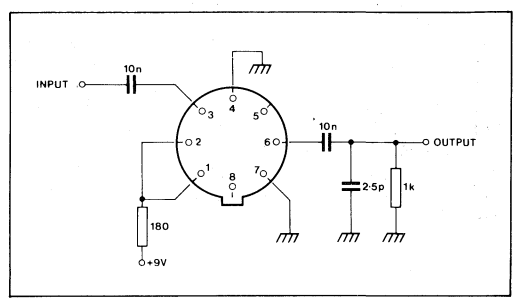


Fig. 4 Test circuit

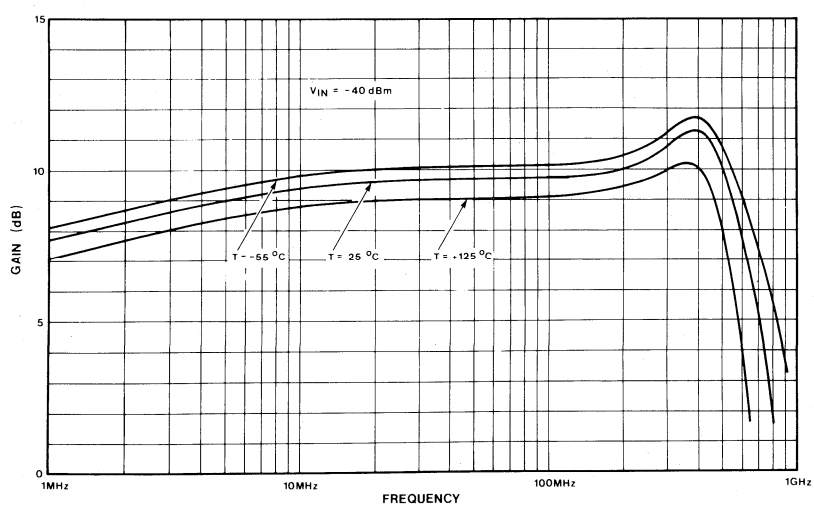


Fig. 5 Small signal frequency response

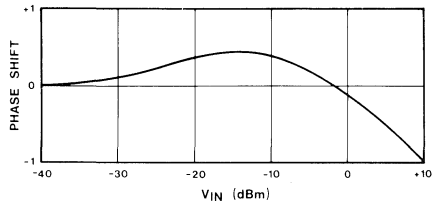


Fig. 6 Phase v. input

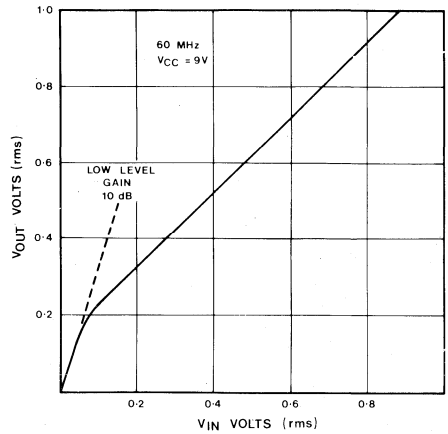


Fig. 7 Transfer characteristics linear plot

TYPICAL APPLICATION — 6 STAGE LOG STIP

Input log range 0dBm to −70dBm
Low level gain 60dB (−70dBm in)
Output dynamic range 20dB
Phase shift (over log range) ±3°
Frequency range 10 — 200MHz

The circuit shown in Fig 9 is designed to illustrate the use of the SL531 in a complete strip. The supply voltage is fed to each stage via an external 180Ω resistor to allow operation to 125°C ambient. If the ambient can be limited to + 100°C then the internal resistor can be used to reduce the external component count. Interstage coupling is very simple with just a capacitor to isolate bias levels being necessary. No connection is necessary to pin 5 unless operation below 10MHz is required. It is important to provide extra decoupling on pin 1 of the first stage to prevent positive feedback occuring down the supply line. An SL560 is used as a unity gain buffer, the output of the log strip being attenuated before the SL560 to give a nominal 0dBm output into 50Ω.

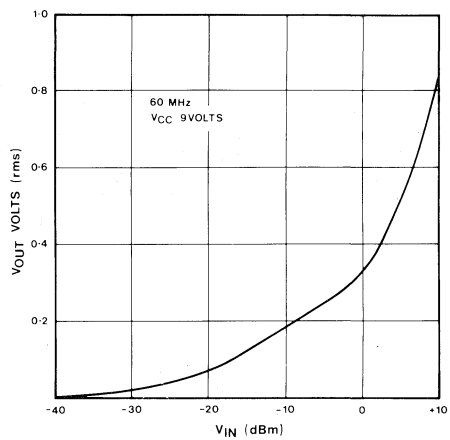


Fig. 8 Transfer characteristics logarithmic input scale

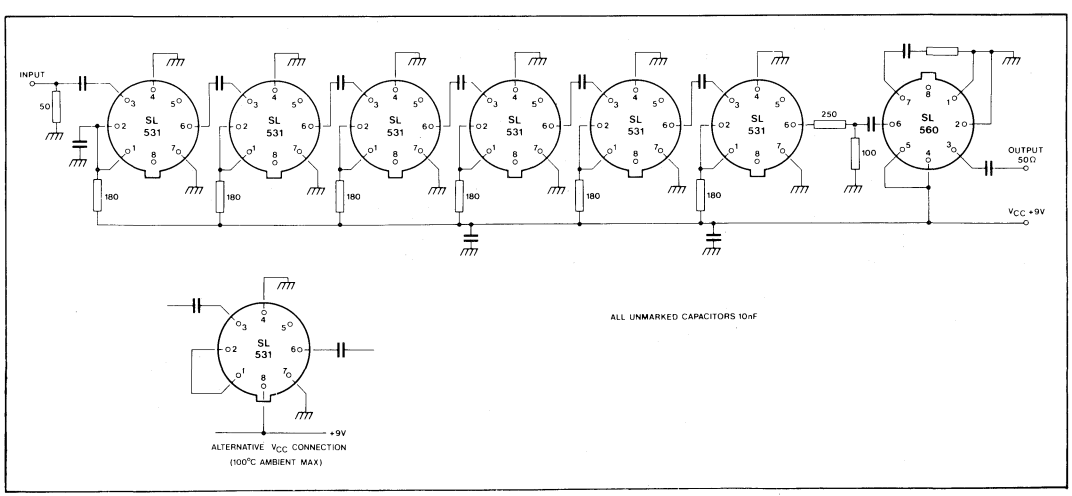


Fig. 9 Circuit diagram 6 stage strip

SL532

LOW PHASE SHIFT LIMITER

The SL532C is a monolithic integrated circuit designed for use in wideband limiting IF strips. It offers a bandwidth of over 400MHz and very low phase shift with amplitude. The small signal gain is 12dB and the limited output is 1V peak to peak. The use of a 5GHz IC process has produced a circuit which gives less than 1° phase shift when overdriven by 12dB. The amplifier has internal decoupling capacitors to ease the construction of cascaded strips and the number of external components required has been minimised.

The device is also available as the SL532AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

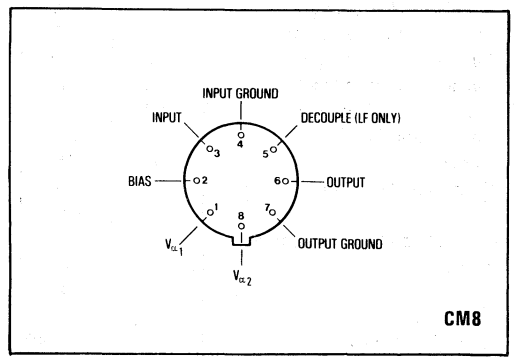


Fig.1 Pin connections

FEATURES

- Low Phase Shift v. Amplitude
- Wide Bandwidth
- Low External Component Count

APPLICATIONS

- Phase Recovery Strips in Radar and ECM Systems (e.g. Doppler)
- Limiting Amps for SAW Pulse Compression Systems
- Phase Monopulse Radars
- Phased Array Radars
- Low Noise Oscillators

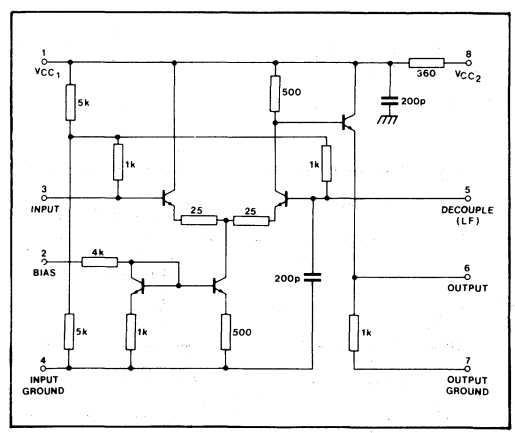


Fig.2 Circuit diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+15V
Storage temperature range	-55°C to +150°C
Operating temperature range	-55°C to +125°C

CIRCUIT DESCRIPTION

The SL532 uses a long-tailed pair limiting amplifier which combines low phase shift with a symmetrical limiting characteristic. This is followed by a simple emitter follower output stage. Each stage of a strip is capable of driving to full output a succeeding SL532 but a buffer amplifier is needed to drive lower impedance loads. No external decoupling capacitors are normally required but for use below 10MHz extra decoupling can be added on pins 1 and 5. Bias for the long-tailed pair is provided by connecting the bias (pin 2) to the decoupled supply (pin 1).

ORDERING INFORMATION

SL532 AC CM
SL532 C CM
SL532 CB CM

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature (ambient) 25°C ± 2°C
Frequency 60MHz : R_L = 1kΩ/<5pF : V_{IN} = -30dBm
V_{CC} = +9.0V : R_S = 50Ω

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	12.8	14	dB	
Small signal voltage gain		12.5		dB	f = 150MHz
-1dB compression point		-10		dBm	
Limited output voltage	1.0	1.15	1.4	V p-p	V_{IN} = +10dBm
Limited output voltage		1.10		V p-p	f = 150MHz
Upper cut-off frequency	250			MHz	-3dB w.r.t. 60MHz
Lower cut-off frequency			10	MHz	May be extended by decoupling pin 5
Supply current	6	8.5	11	mA	No signal
Phase variation with signal level		±1	±3	Degrees	-30dBm to +10dBm
		±1.5		Degrees	-30dBm to 0dBm. f = 150MHz
Absolute phase shift input to		-21		Degrees	f = 60MHz
output		-34		Degrees	f = 100MHz
		-43		Degrees	f = 150MHz
		-69		Degrees	f = 200MHz
Input impedance		1kΩ/2.5pF			
Output impedance		30Ω			
Noise figure		7		dB	400Ω source impedance. f = 60MHz
Gain variation with temperature		±2		dB	-40°C to 85°C
Phase variation with temperature		±0.5		Degrees	-40°C to +85°C at any level between -30dBm to +10dBm
Limited output voltage variation with temperature		±0.05		V p-p	V_{IN} = +10dBm -40°C to +85°C

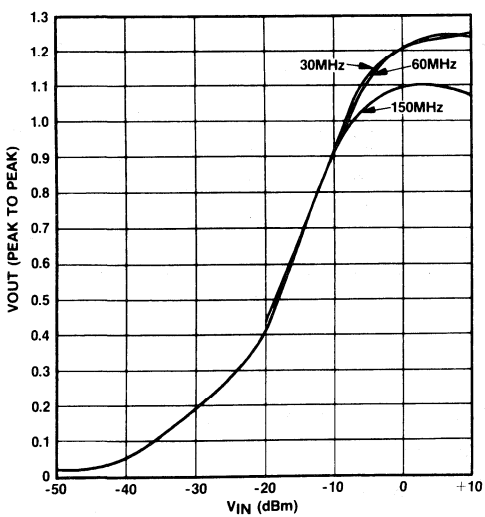


Fig.3 Transfer characteristic of a single stage

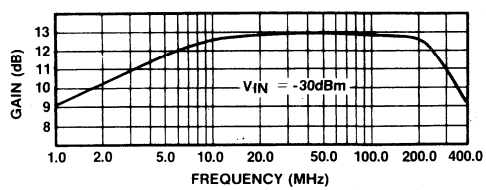


Fig.4 Gain/frequency curve of a typical device

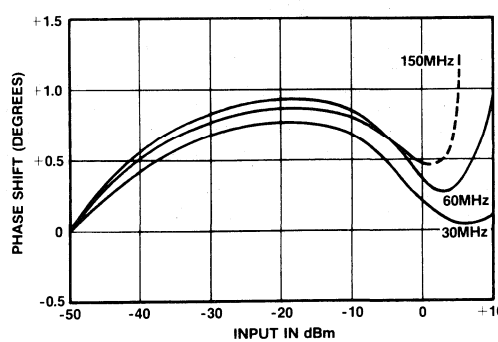
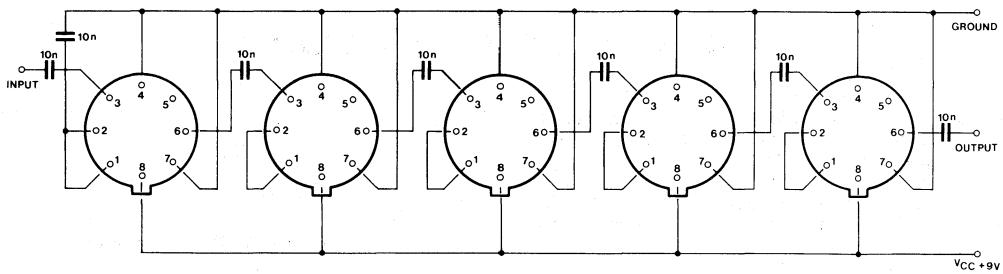


Fig.5 Phase change with input level

TYPICAL APPLICATION

Five stage strip

Input signal for full limiting	300μV rms −57dBm
Limited output	1V p-p
Phase shift (V_{IN} −57 → +10dBm)	±3° typ.



The recommended output buffer amplifier to drive 50Ω loads is the SL560C

Fig.6 Five stage IF strip

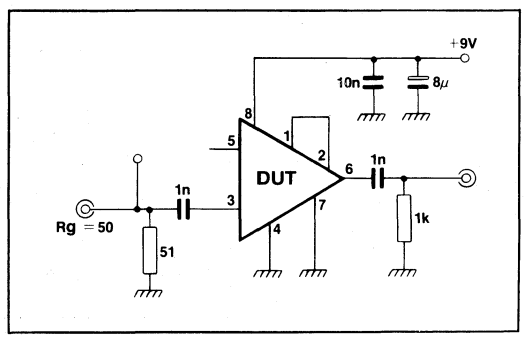


Fig.7 SL532 test circuit

SL1521

300MHz WIDEBAND LOG AMPLIFIER

The SL1521A and C are wideband amplifiers intended for use in successive detection logarithmic IF strips operating at centre frequencies of up to 200MHz. It is a plug in replacement for the SL521 series of RF amplifiers. The mid-band voltage gain of the SL1521 is typically 12dB. The SL1521A and C differ mainly in the tolerance of voltage gain.

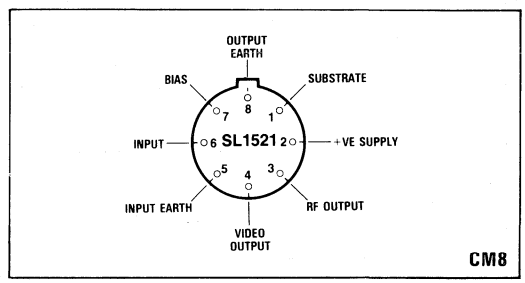


Fig.1 Pin connections

APPLICATIONS

- Radar IF Strips
- Wideband Amplification

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Operating temperature	−55°C to +125°C
Maximum chip operating temperature	150°C
Chip to ambient thermal resistance	250°C/W

Test circuits: see Fig.8

ORDERING INFORMATION

SL1521 A CM
SL1521 AB CM
SL1521 C CM
SL1521 CB CM

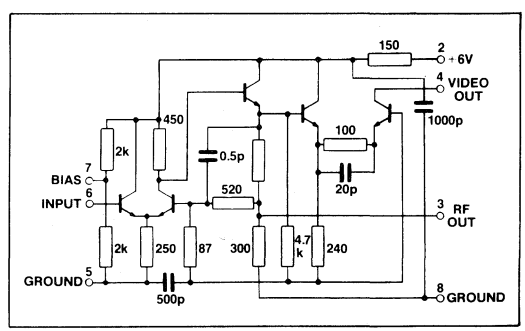


Fig.2 Circuit diagram

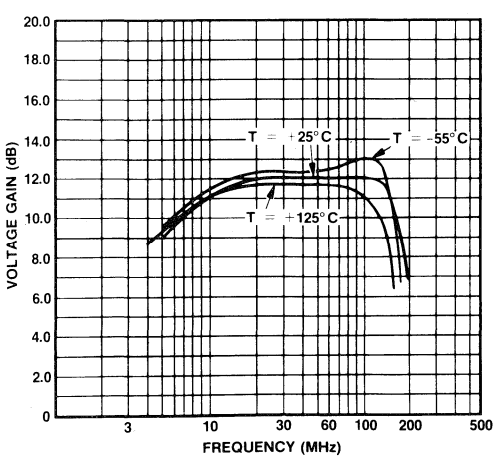


Fig.3 Voltage gain v. frequency

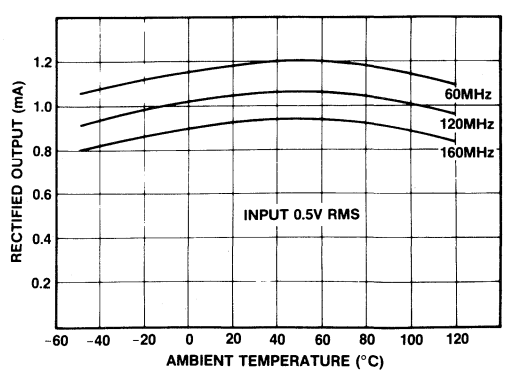


Fig.4 Maximum rectified output current v. temperature

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature = +22°C ± 2°C
Supply voltage = +5.2V
DC connection between input and bias pins.

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 120MHz	SL1521A	11.5		12.5	dB	3mV rms input, 50 ohms source, 8pF load + 500Ω
	SL1521C	10.8		13.1	dB	
Voltage gain, f = 160MHz	SL1521A	11.2		12.8	dB	
	SL1521C	10.6		13.4	dB	
Upper cut-off frequency	SL1521A	250	285		MHz	50 ohms source
	SL1521C		285		MHz	
Lower cut-off frequency	All types		6	10	MHz	50 ohms source
Propagation delay	All types		0.6		ns	
Maximum rectified video output current	SL1521A	0.95		1.05	mA	f = 120MHz, 0.5V rms input, 8pF load, 500 ohms in parallel
	SL1521C	0.90		1.20	mA	
Variation of gain with supply voltage	All types		1.0		dB/V	
Variation of maximum rectified output current with supply voltage	All types		30		%/V	
Maximum input signal before overload	All types		1.5		V rms	See note below
Noise figure			4.5	6.0	dB	f = 120MHz, source resistance optimised
Supply current	All types	10.0	15.0	20.0	mA	
Maximum RF output voltage	All types	1.0			V p-p	f = 120MHz

Operating Notes

The amplifiers are intended for use directly coupled, as shown in Fig.7.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 8. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

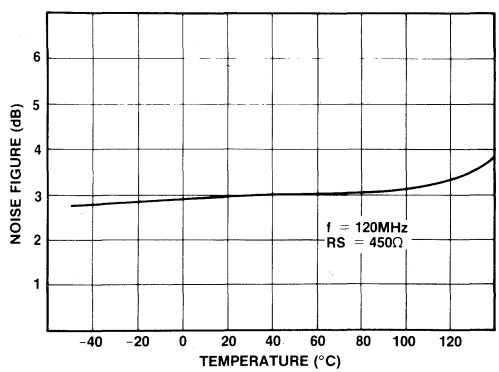


Fig.5 Typical noise figure v. temperature

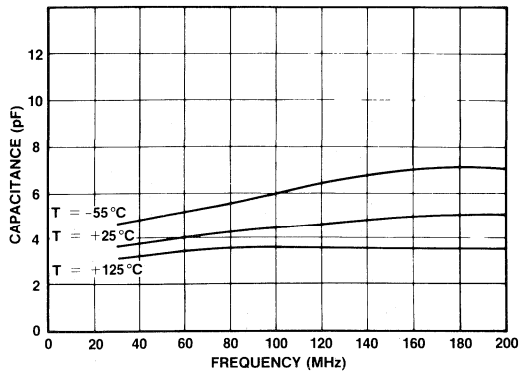


Fig.6 Input admittance with open-circuit output

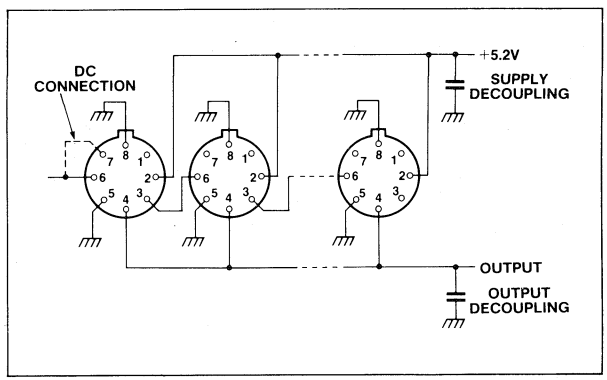


Fig.7 Direct coupled amplifier

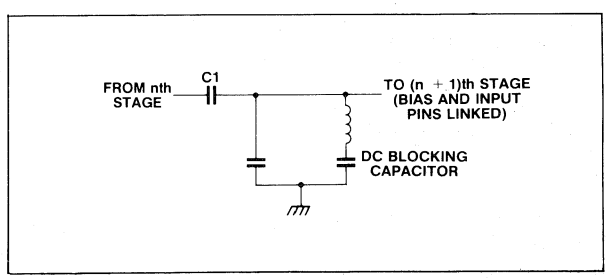


Fig.8 Suitable interstage tuned circuit

SL1523

300MHz DUAL WIDEBAND LOG AMPLIFIER

The SL1523C consists of two SL1521's in series, and is intended to reduce the package count and improve the packing density in logarithmic strips at frequencies up to 200 MHz.

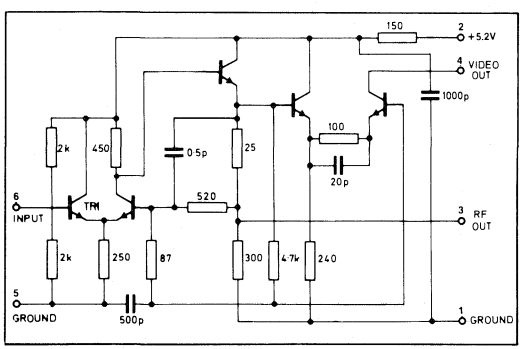


Fig. 2 SL1523 circuit diagram (each amp)

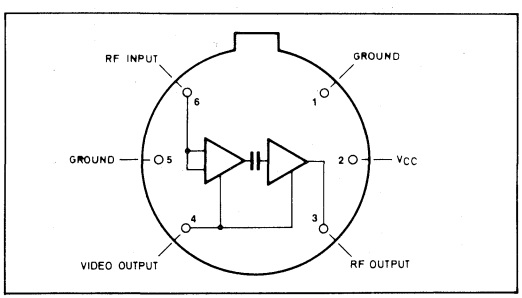


Fig. 3 SL1523 block diagram

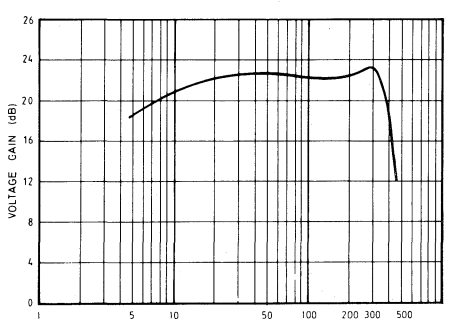


Fig. 4 Voltage gain v. frequency

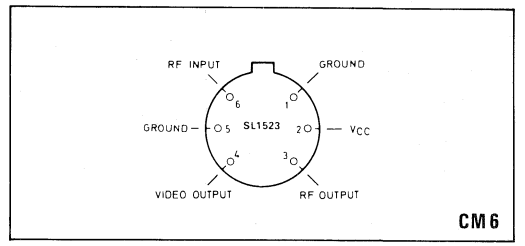


Fig. 1 Pin connections (bottom view)

Absolute Maximum Ratings (Non-Simultaneous)

The absolute maximum ratings are limiting values above which operating life may be shortened or satisfactory performance may be impaired.

Storage temperature range	—55°C to +175°C
Operating temperature	—55°C to +125°C
Chip operating temperature:	150°C
Chip-to-ambient thermal resistance	300°C/W
Chip-to-case thermal resistance	95° C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+ 9V

ORDERING INFORMATION

SL1523 C CM

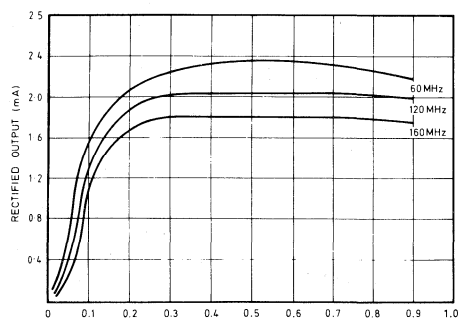


Fig. 5 Rectified output current v. input signal

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Temperature = 22°C ± 2°C
Supply voltage = + 5.2V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	21		27	dB	f = 120MHz, 3mV rms input, 50Ω source 4pF load + 50Ω
Voltage gain	20		27	dB	f = 160MHz, 3mV rms input, 50Ω source 4pF load + 500Ω
Upper cut-off frequency	175	200		MHz	50Ω source
Lower cut-off frequency		8	20	MHz	50Ω source
Propagation delay		1.2		ns	
Maximum rectified video output current	1.6		2.0	mA	f = 120MHz, 0.5V rms input, 4pF load
Variation of gain with supply voltage		2.0		dB/V	
Variation of maximum rectified output current with supply voltage		30		%/V	
Maximum input signal before overload		1.5		V rms	See note below
Noise figure		3		dB	f = 120MHz, source resistance optimised
Supply current	20	30	40	mA	
Maximum RF output voltage	1.0			V p-p	f = 120MHz

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction of TR1 on peaks.

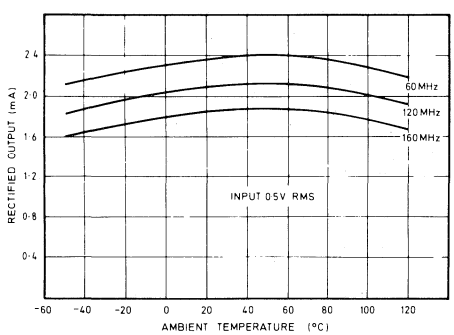


Fig.6 Maximum rectified output current v. temperature

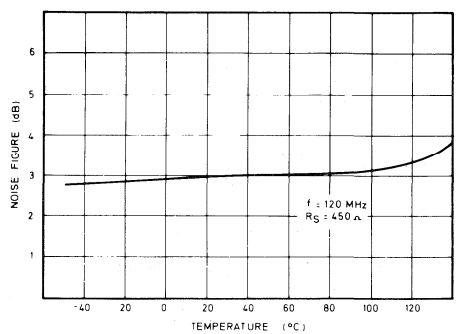


Fig.8 Input admittance with open circuit output

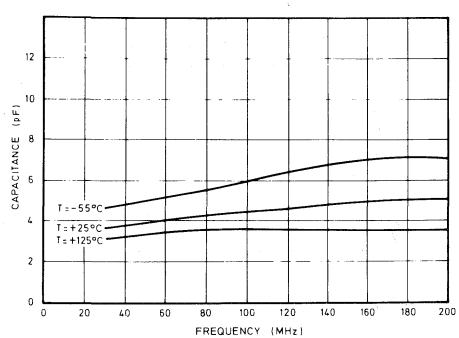


Fig.7 Typical noise figure v. temperature

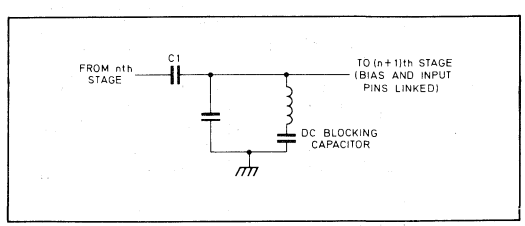


Fig.9 Suitable interstage tuned circuit

SL1613

WIDEBAND LOG IF STRIP AMPLIFIER

The SL1613 is a bipolar monolithic integrated circuit wideband amplifier intended for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 60MHz. The device provides amplification, limiting and rectification, is suitable for direct coupling and incorporates supply line decoupling. The mid-band voltage gain of the SL1613 is typically 12dB.

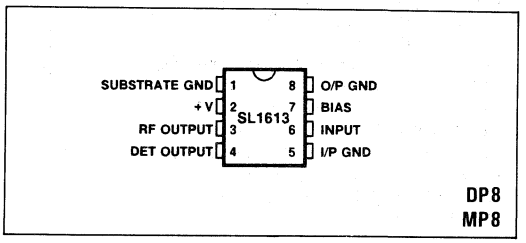


Fig. 1 Pin connections (top)

FEATURES

- Well Defined Gain
- 4.5dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 150MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity Better than 2dB
- Low Cost Radar
- Radio Telephone Field Strength Meters

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +125°C
Operating temperature range	−30°C to +85°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

ORDERING INFORMATION

SL1613 C DP
SL1613 C MP

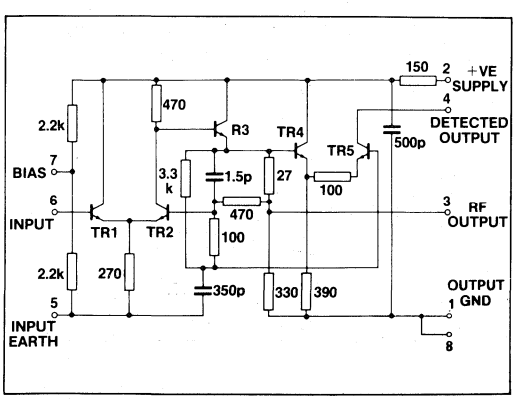


Fig. 2 Circuit diagram

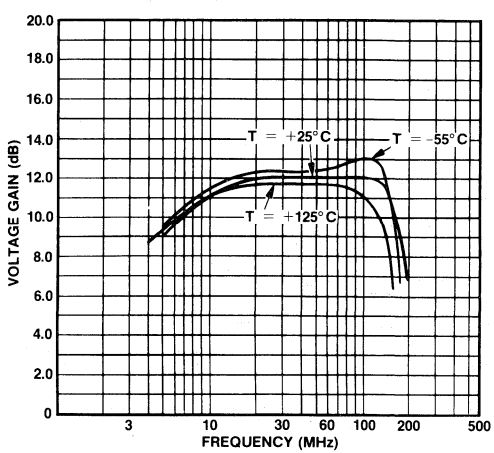


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_A = +22°C ±2°C
Supply voltage = +6V
DC connection between input and bias pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10	12	14	dB	f=30MHz, R_s=10Ω, C_L=8pF
Upper cut-off frequency (Fig. 3)		150		MHz	R_S=10Ω, C_L=8pF
Lower cut-off frequency (Fig. 3)		5		MHz	R_S=10Ω, C_L=8pF
Propagation delay		2		ns	
Max. rectified video output current (Figs. 4 and 5)	0.8	1	1.3	mA	f=60MHz, V_{in}=500mV rms
Variation of gain with supply voltage		0.7		dB/V	
Variation of maximum rectified output current with supply voltage		25		% / V	
Maximum input signal before overload		1.9		V rms	See Note 1
Noise figure (Fig. 6)		4.5		dB	f=60MHz, R_s=450Ω
Maximum RF output voltage		1.2		Vp-p	
Supply current		15	20	mA	

Note 1 Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction of TR1 on peak.

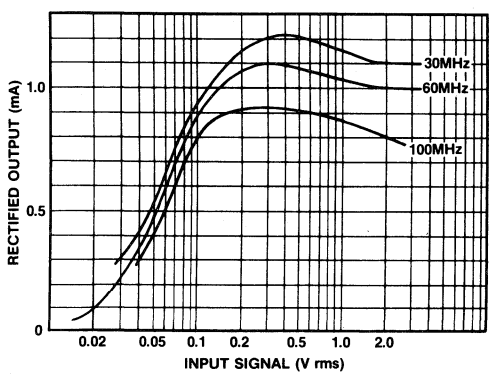


Fig. 4 Rectified output current v. input signal

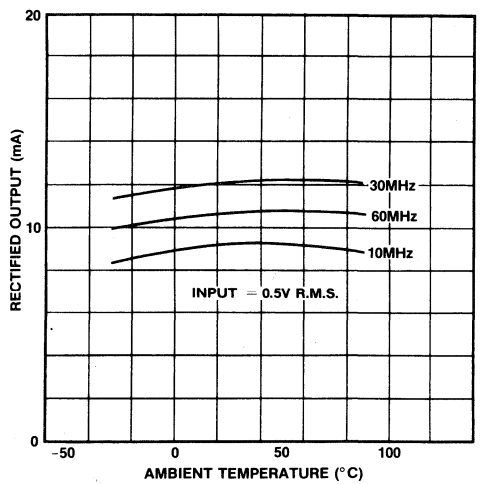


Fig. 5 Maximum rectified output current v. temperature

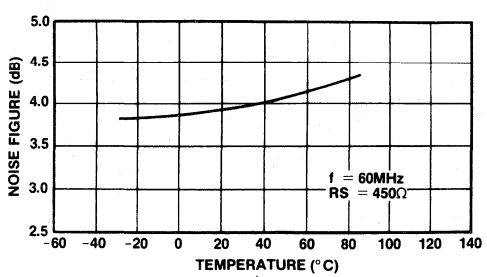


Fig. 6 Typical noise figure v. temperature

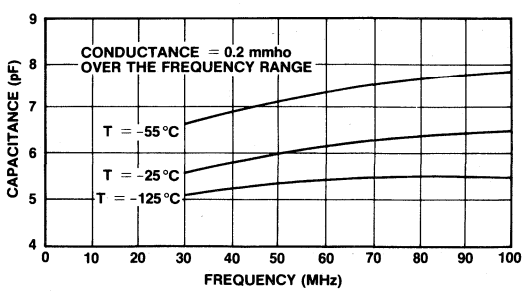


Fig. 7 Input admittance with open circuit output

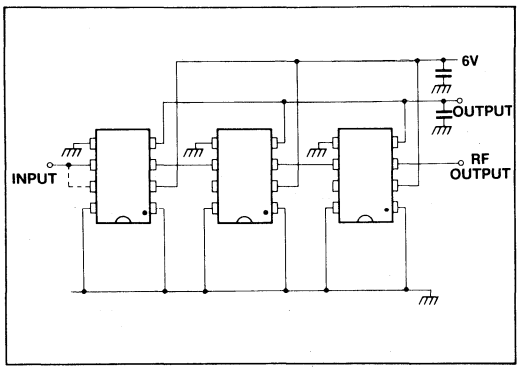


Fig. 8 Direct coupled amplifiers

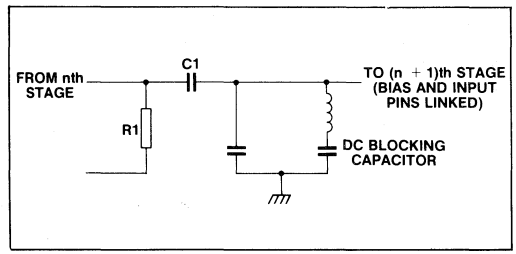


Fig. 9 Suitable interstage tuned circuit

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple parallel or series circuit cannot be used. This choice of network is also controlled by the need to avoid distorting the logarithmic law: the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A single capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two ground leads to avoid the introduction of common ground lead inductance between input and output circuits. the equipment designer should take care to aviod the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nf	10nF	3nF	1nF

The on-chip 500pF supply decoupling capacitor has a resistance of, typically 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V. (See Absolute Maximum Ratings).

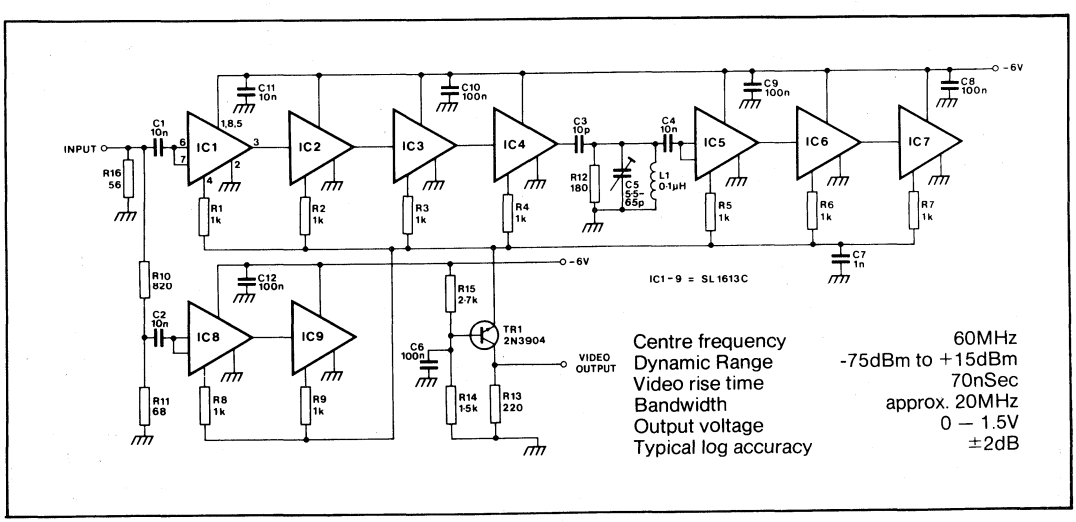


Fig. 10 Circuit diagram of low cost strip

SL1615

WIDEBAND LOG IF STRIP AMPLIFIER

The SL1615 is a bipolar monolithic integrated circuit wideband amplifier intended for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 60MHz. The device provides amplification, limiting and rectification, is suitable for direct coupling and incorporates supply line decoupling. The mid-band voltage gain of the SL1615 is typically 12dB.

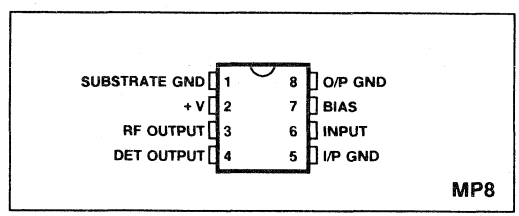


Fig.1. Pin connections - top view

FEATURES

- Well Defined Gain
- 4.5dB noise Figure
- High I/P Impedance
- Low O/P Impedance
- 150MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity Better than 2dB
- Low Cost Radar
- Radio Telephone Field Strength Meters

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range	–55°C to +125°C
Operating Temperature	–30°C to +85°C
Maximum Instantaneous Voltage at Video Output	+12V
Supply Voltage	9V

ORDERING INFORMATION

SL1615 NA MP

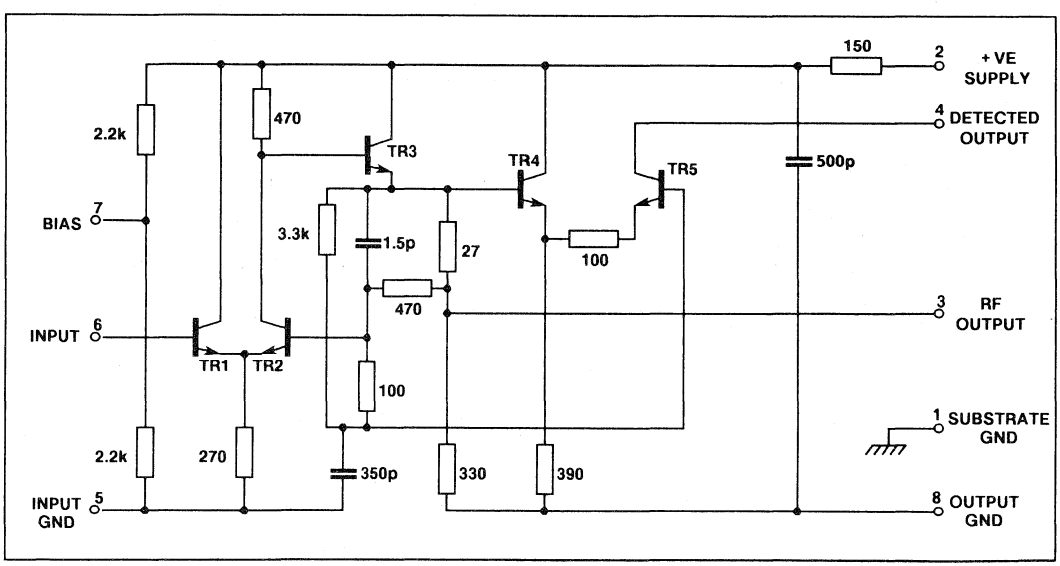


Fig.2. Circuit Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Temperature = +22°C ±2°C, Supply Voltage = +6V, DC Connection between Input and Bias Pins

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Voltage Gain, f=30MHz	11		13	dB	10Ω Source, 8pF Load
Voltage Gain, f=60MHz	10.7		13.3	dB	10Ω Source, 8pF Load
Upper Cut-off frequency (Fig.3)	130	170		MHz	10Ω Source, 8pF Load
Lower cut-off Frequency (Fig.3)		5	10	MHz	10Ω Source, 8pF Load
Propagation Delay		2		ns	
Maximum rectified Video Output Current (Fig. 4 and 5)	0.90		1.20	mA	f=60MHz, 0.5Vrms Input
Variation of Gain with Supply Voltage		0.7		db/V	
Variation of Maximum Rectified Output Current with Supply Voltage		25		%/V	
Maximum Input Signal before Overload	1.8	1.9		V rms	See Note Below
Noise Figure (Fig.6)		4		dB	f=60MHz, Rs=450Ω
Supply Current	11.5		19.0	mA	
Maximum RF Output Voltage		1.2		Vp-p	

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction to TR1 on peaks.

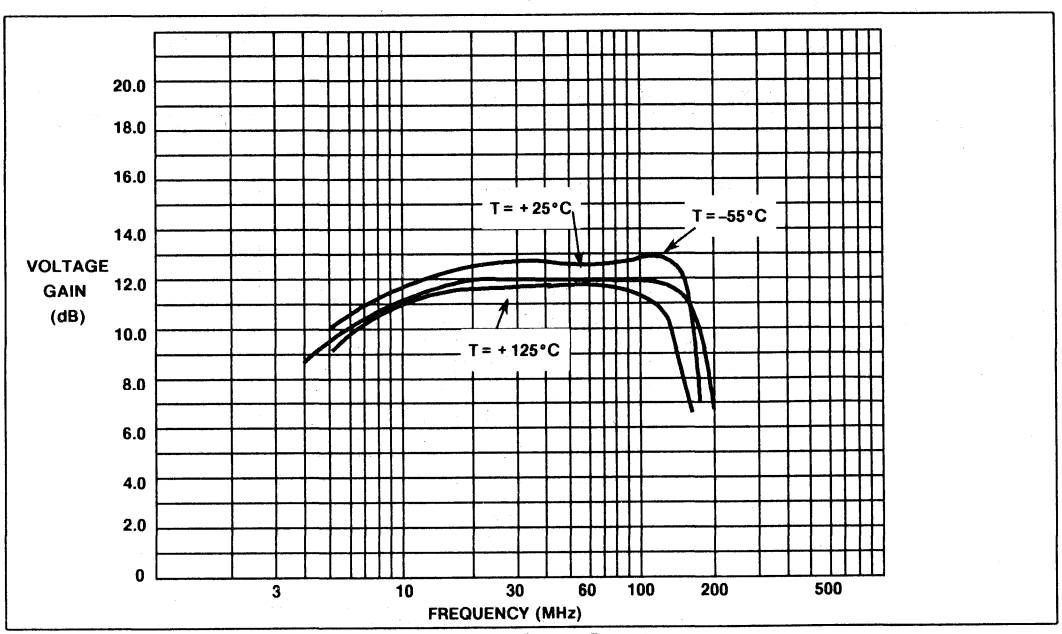


Fig.3. Voltage Gain v. Frequency

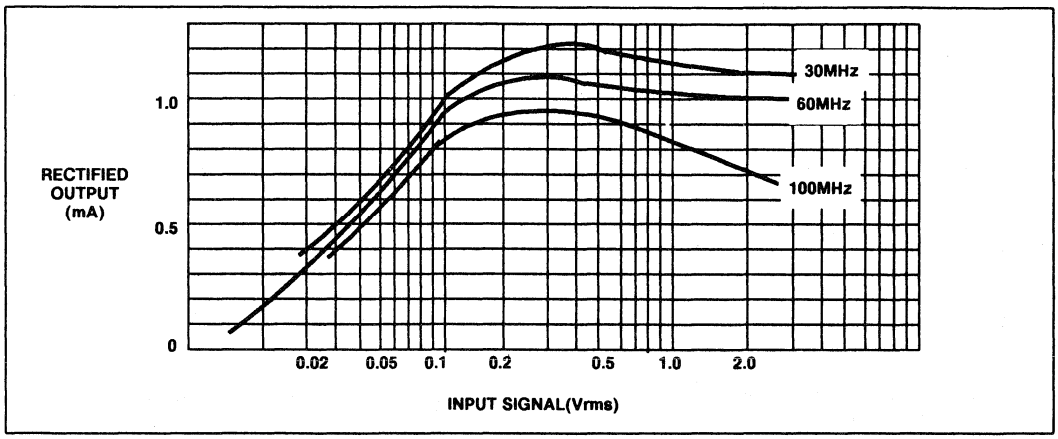


Fig.4. Rectified Output Current v. Input Signal

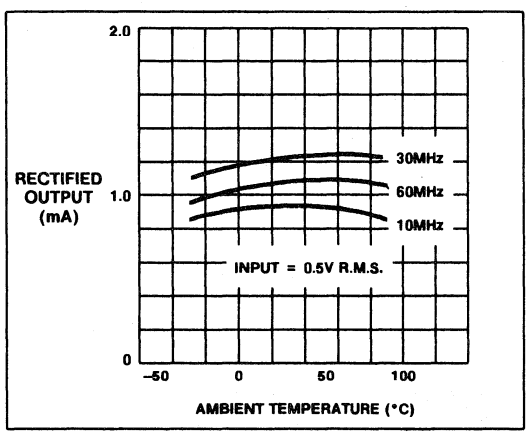


Fig.5. Maximum Rectified Output Current v. Temperature

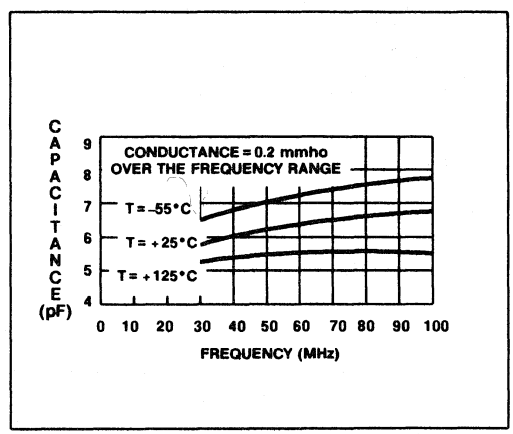


Fig.7. Input Admittance with Open Circuit Output

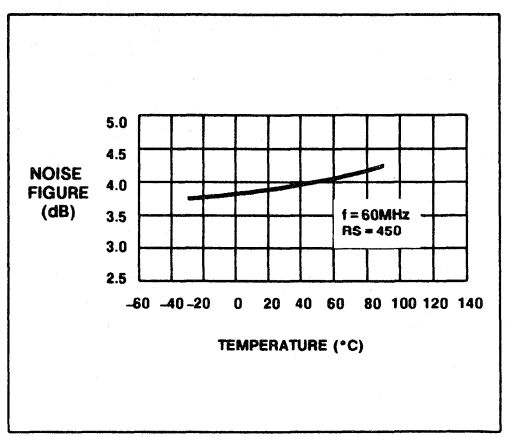


Fig.6. Typical Noise Figure v. Temperature

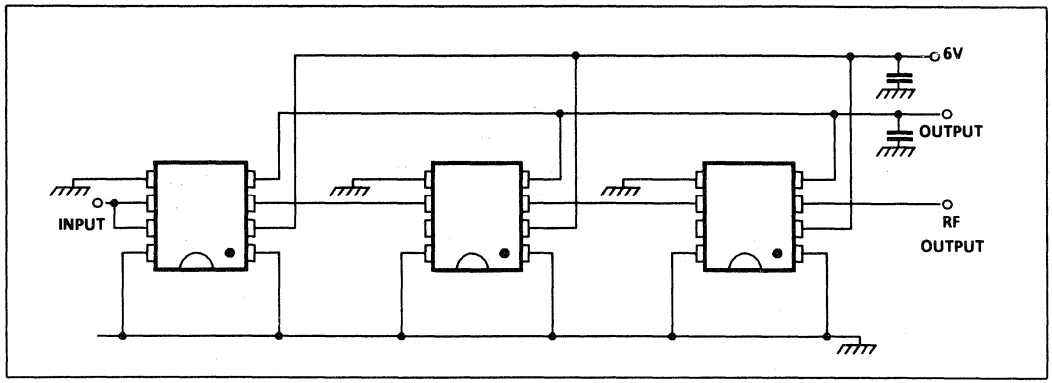


Fig.8 Direct Coupled Amplifiers

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple parallel or series circuit cannot be used. This choice of network is also controlled by the need to avoid distorting the logarithmic law: the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C3 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R12 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A single capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two ground leads to avoid the introduction of common ground lead inductance between input and output circuits. the equipment designer should take care to aviod the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The on-chip 500pF supply decoupling capacitor has a resistance of, typically 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V. (See Absolute Maximum Ratings).

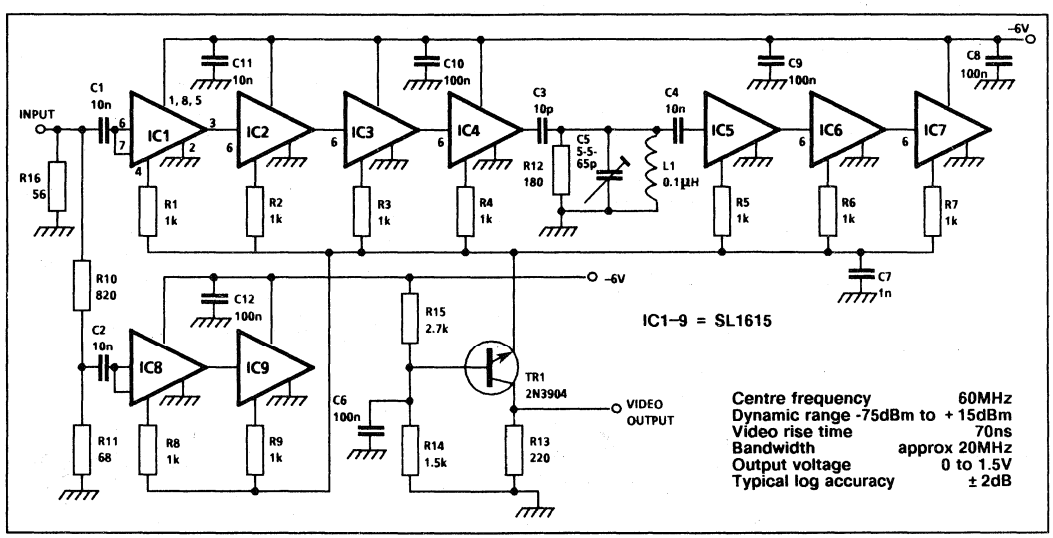


Fig.9 Circuit Diagram of Low Cost Strip

SL2521B

1.3GHz DUAL WIDEBAND LOGARITHMIC AMPLIFIER

(NOT RECOMMENDED FOR NEW DESIGNS – TO BE REPLACED BY SL2524)

The SL2521 is a revolutionary monolithic integrated circuit designed on an advanced 3 micron oxide isolated bipolar process. The amplifier is a successive detection type which provides linear gain and accurate logarithmic signal compression over a wide bandwidth.

When six stages (three SL2521s) are cascaded the strip can be used for IFs between 30-650MHz whilst achieving greater than 65dB dynamic range with a log accuracy of $<\pm 1.0$dB. The balanced limited output also offers accurate phase information with input amplitude. One log strip therefore offers limited IF output, phase and video information.

The device is also available as the SL2522BC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

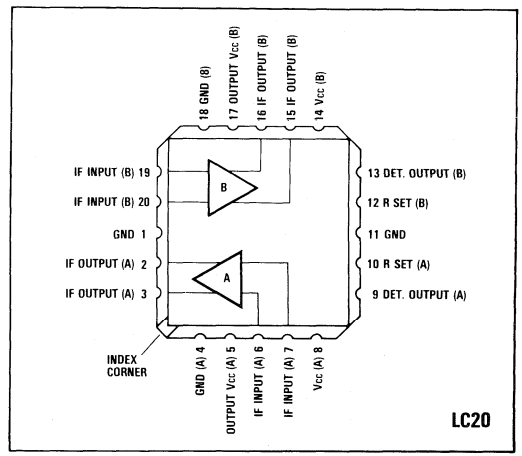


Fig.1 Pin connections - top view

FEATURES

- 1.3GHz Bandwidth (-3dB)
- Balanced IF Limiting
- 3ns Rise Times/5ns Fall Times (Six Stages)
- 20ns Pulse Handling (Six Stages)
- Temperature Stabilised
- Full Military Temperature Range/Surface Mountable

ORDERING INFORMATION

SL2521 B LC
Military version available:
SL2522 AC LC
SL2522 BC LC

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Applications

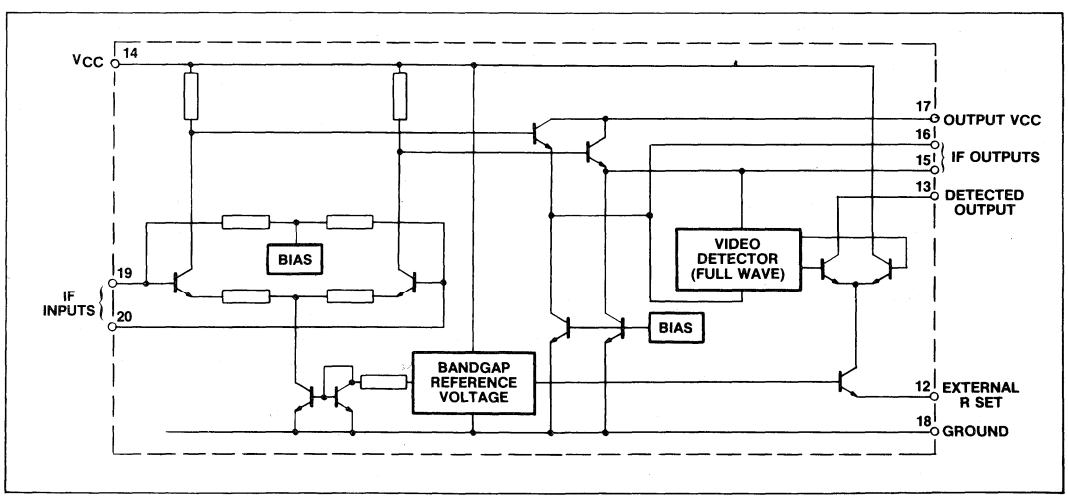


Fig.2 Circuit diagram (single stage B only)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Frequency = 200MHz, T_{amb} = -30°C to +85°C, Input voltage = -30dBm, V_{CC} = 6V ± 0.1V, Source Impedance = 50Ω, Test Circuit = Fig.3, R_{set} = 300Ω. Tested as a dual stage.

Characteristics	Value						Units	Conditions	Notes
	50Ω Load			1kΩ Load					
	Min.	Typ.	Max.	Min.	Typ.	Max.			
Small signal gain (dual stage, single ended)	9.2	10.7	12.2	14.8	16.5	18.3	dB	T_{amb} = -30°C frequency = 200MHz	2
	9.8	11.0	12.2	15.8	17.0	18.2	dB	T_{amb} = +25°C frequency = 200MHz	
	9.7	11.2	12.4	15.8	17.3	18.8	dB	T_{amb} = +85°C frequency = 200MHz	2
	9.9	11.5	13.2	16.1	18.1	20.1	dB	T_{amb} = -30°C frequency = 500MHz	2
	10.2	11.4	12.7	16.3	18.0	19.8	dB	T_{amb} = +25°C frequency = 500MHz	
	9.7	11.2	12.7	15.6	17.6	19.6	dB	T_{amb} = +85°C frequency = 500MHz	2
Detected output current (max)	3.05	3.25	3.45	3.20	3.45	3.70	mA	T_{amb} = -30°C, V_{in} = 0dBm, f = 200MHz	2
	3.15	3.3	3.45	3.30	3.5	3.70	mA	T_{amb} = +25°C, V_{in} = 0dBm, f = 200MHz	
	3.10	3.3	3.50	3.30	3.55	3.80	mA	T_{amb} = +85°C, V_{in} = 0dBm, f = 200MHz	2
	2.8	3	3.2	2.8	3	3.2	mA	T_{amb} = -30°C, V_{in} = 0dBm, f = 500MHz	2
	2.9	3.05	3.45	2.8	3	3.2	mA	T_{amb} = +25°C, V_{in} = 0dBm, f = 500MHz	
	2.85	3.03	3.65	2.8	3	3.2	mA	T_{amb} = +85°C, V_{in} = 0dBm, f = 500MHz	2
Detected output current (no signal)				0.9	1.1	1.3	mA	T_{amb} = -30°C	2
				0.95	1.1	1.25	mA	T_{amb} = +25°C	
				0.9	1.1	1.3	mA	T_{amb} = +85°C	2
Upper cut off frequency (RF)				900	1100		MHz	-3dB w.r.t. 200MHz, T_{amb} = +25°C	1
Lower cut off frequency (RF)					0.35	1	MHz		
Detector cut off frequency					700		MHz	50% O/P current w.r.t. 200MHz	
Limited IF O/P voltage				105	120	145	mV	I/P voltage = 0dBm, T_{amb} = +25°C	
Phase variation with input		±2	±6				Degree	Frequency = 70MHz, -55 to +3dBm	
level (normalised to -30dBm)		±2	±6				Degree	Frequency = 200MHz, -55 to +3dBm	
Limited O/P var with temp.		±12	±25				mV		
Noise figure		12			9		dB		
Max I/P before overload					15		dBm		
Input impedance					1		kΩ	1kΩ in parallel with 2pF	
Output impedance					40		Ω		
Supply current			90		75	90	mA		
Variation of max detected current with V_{CC}					5		%/V	T_{amb} = +25°C	
Variation of small signal gain with V_{CC}					0.5		dB/V	T_{amb} = +25°C	

NOTES
1. Parameter guaranteed but not tested.
2. Tested at 25°C only, but guaranteed at temperature.

GENERAL DESCRIPTION

The SL2521 is primarily intended for use in Radar and EW receivers. Six stages (3 chip carriers) can be cascaded to form a very wideband logarithmic amplifier offering >65dB of input dynamic range, with pulse handling of better than 25ns. (See Figs.4 and 5.)

A six stage strip also offers balanced IF limiting, linearity (log accuracy) of <±1.0dB, temperature stabilisation and programmable detector characteristics.

The detector has an external resistor set pin which allows the major characteristics of the detector to be programmed. With a six stage strip it is possible to vary the value of R_{set} on each detector and so improve the overall log error/linearity.

The detector is full wave and good slew rates are achieved with 2ns rise and 5ns fall times (no video filter). The video bandwidth for a six stage strip is typically 600MHz (-3dB).

The amplifier also offers balanced IF limiting, low phase shift versus input amplitude, and at an IF of 120MHz, less than 7° of phase change is achievable over the input level of -55dBm to +5dBm.

The IF and Video ports can be used simultaneously so offering phase, frequency and pulse (video) information. A slight loss of dynamic range (2dB) will be observed when the IF ports are used in conjunction with the video.

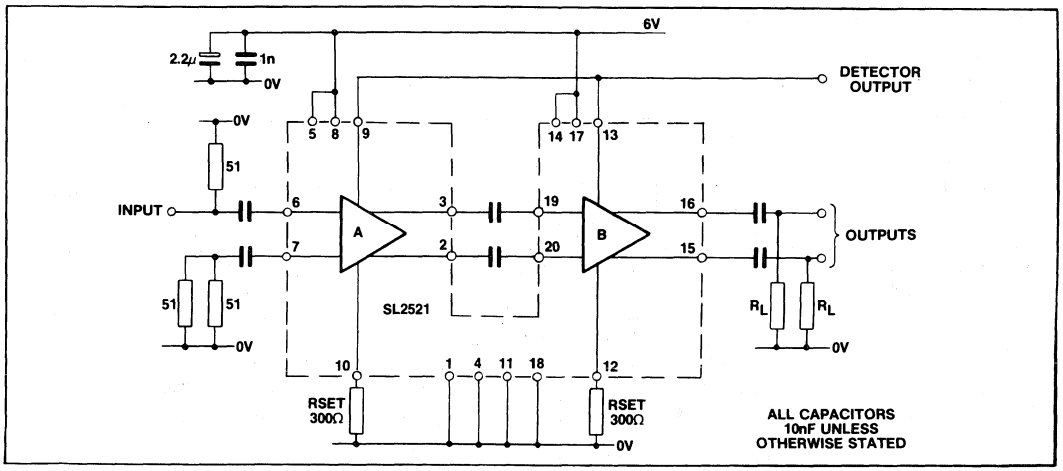


Fig.3 Test circuit

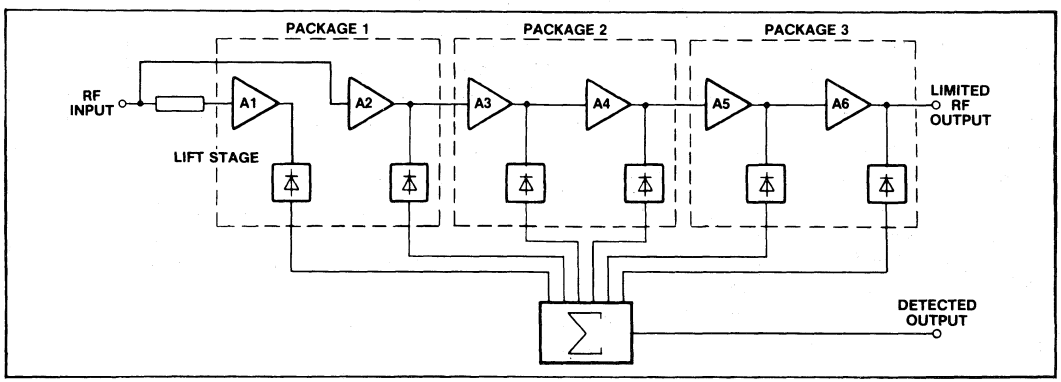


Fig.4 Schematic diagram showing configuration of SD amplifier

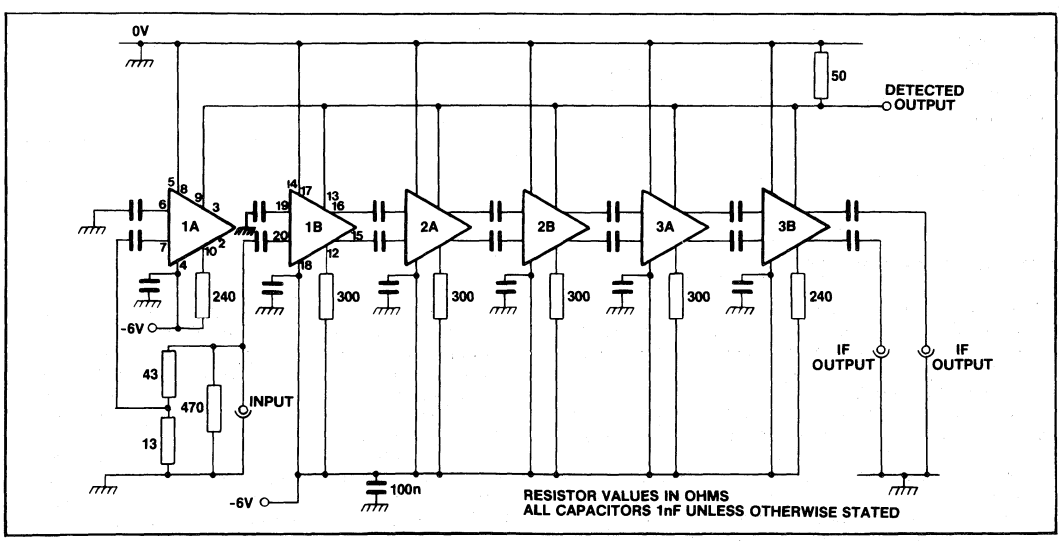


Fig. 5 Circuit diagram for 6-stage log strip (results shown in Figs. 18 to 35 were achieved with this circuit)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER (i.e. 1 SL2521)

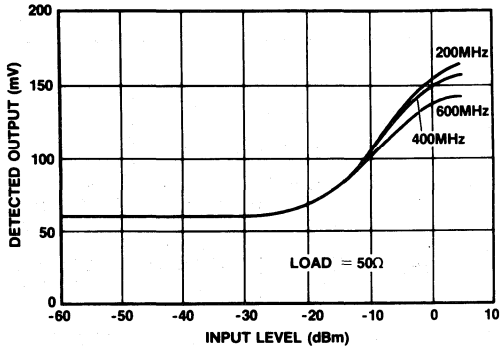


Fig.6 Detected O/P Vs input level at 200,400,600MHz for $R_L = 50\Omega$

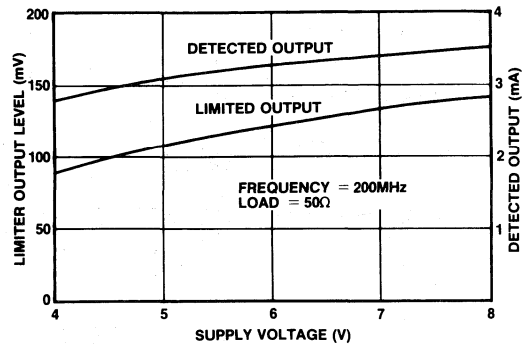


Fig.7 Output levels Vs supply voltage

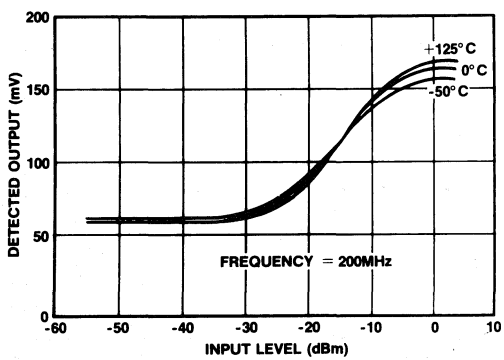


Fig.8 Detected output Vs input level and temperature

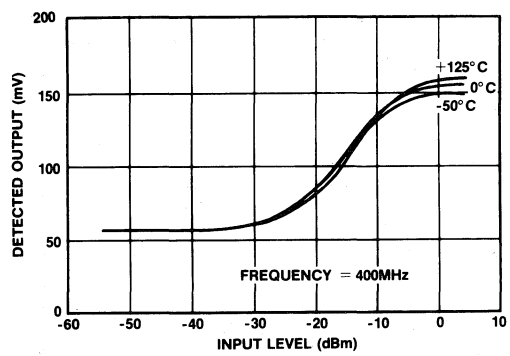


Fig.9 Detected output Vs input level and temperature

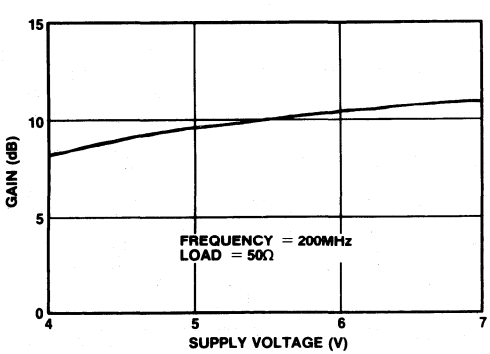


Fig.10 Gain Vs supply voltage

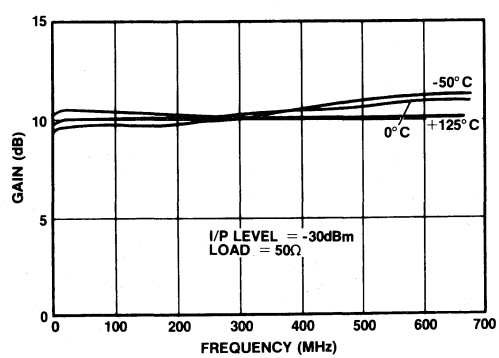


Fig.11 Gain Vs frequency of 2 amplifiers (1 SL2521)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER

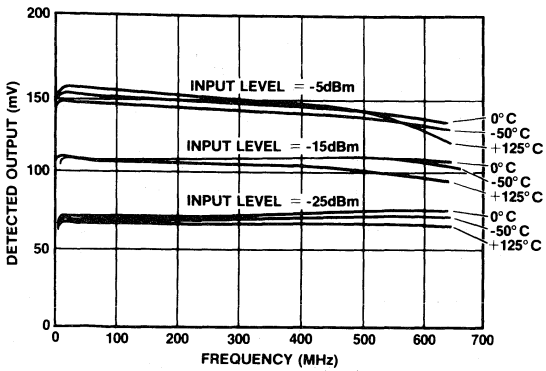


Fig.12 Detected output level Vs frequency and temperature

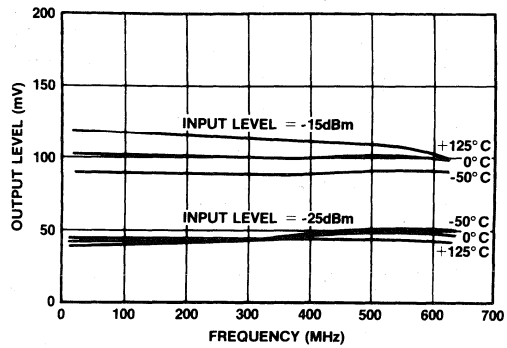


Fig.13 Limited output level Vs frequency and temperature

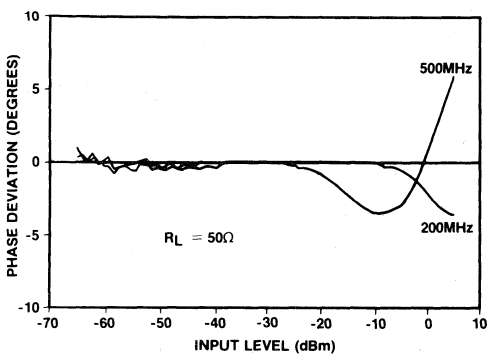


Fig.14 Normalised phase Vs input level at 200 and 500MHz for $R_L = 50\Omega$

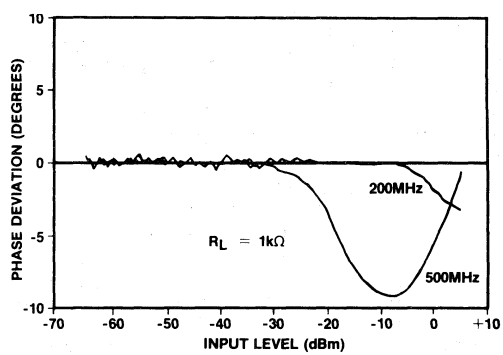


Fig.15 Normalised phase Vs input level at 200 and 500MHz for $R_L = 1k\Omega$

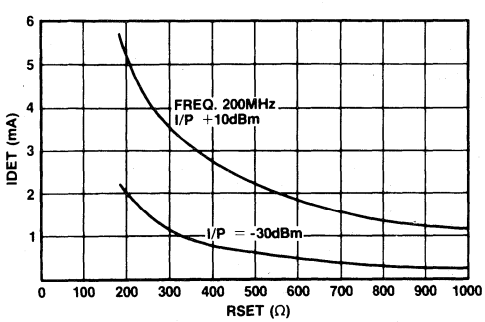


Fig.16 Detector current Vs R_{set} at 200MHz

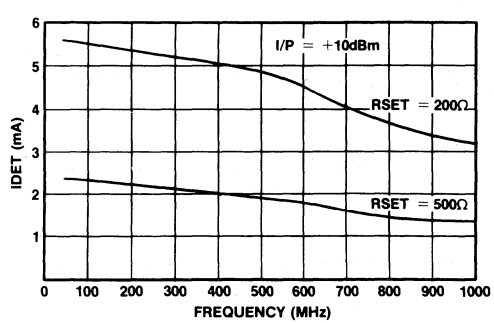


Fig.17 Detector current Vs frequency at $R_{set} = 200\Omega$ and 500Ω

TYPICAL CHARACTERISTICS FOR A SIX STAGE STRIP, USING THE VIDEO OUTPUT

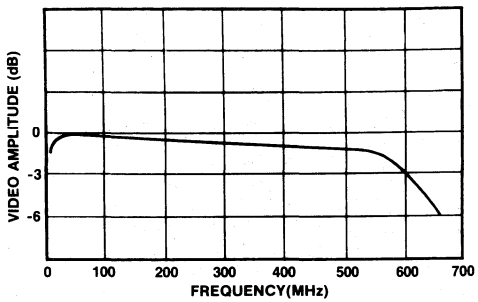


Fig.18 Video bandwidth (detector)

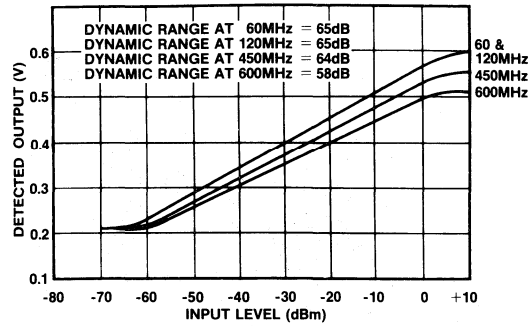


Fig.19 Video output Vs CW input at 60, 120, 450 and 600MHz at 25° C

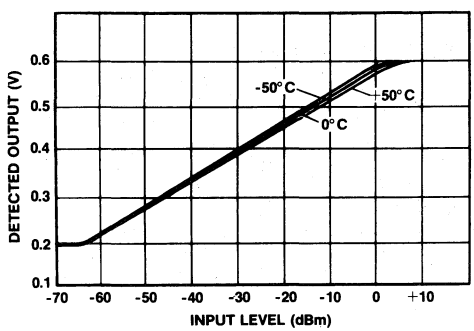


Fig.20 Detected output Vs input level and temperature at 60, 120MHz

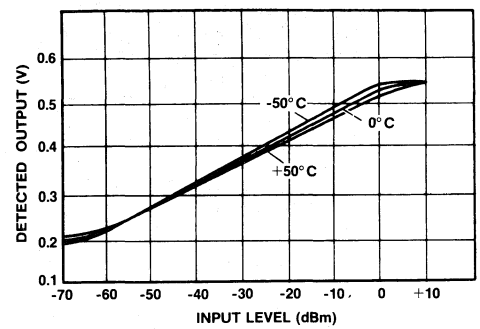


Fig.21 Detected output Vs input level and temperature at 450MHz

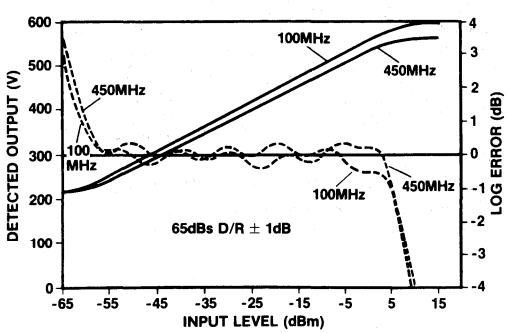


Fig.22 Detected O/P and log linearity at 450 and 100MHz

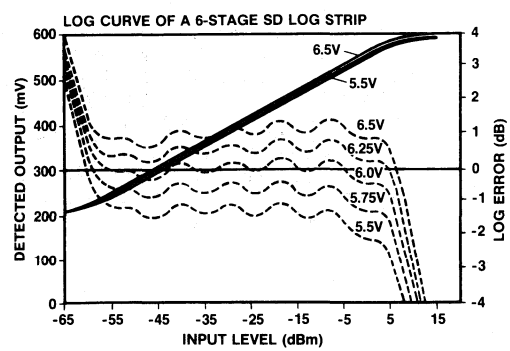


Fig.23 Logarithmic output Vs Vcc

SL2521: PULSE FIDELITY FOR A SIX STAGE STRIP

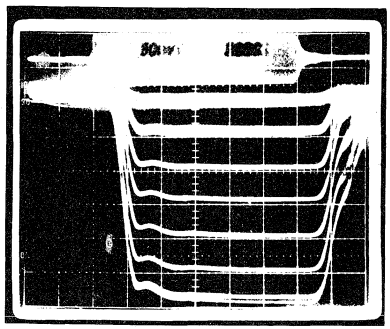


Fig.24 60ns I/P pulse. With low pass video filter. Horizontal = 10ns/div. Vertical = 50mV/div. Input level -70dBm to -10dBm

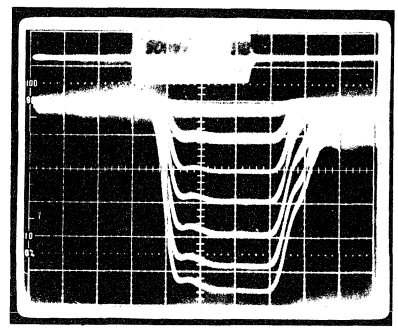


Fig.25 As Fig.25 with 35ns input pulse (Slight glitch on front edge is due to underdamping of video filter)

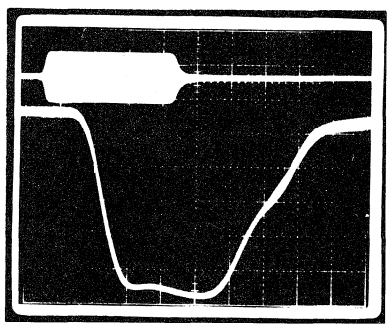


Fig.26 20ns input pulse. Showing input and output pulse with low pass video filter. Horizontal = 5ns/div. Vertical = 50mV/div; -10dBm input.

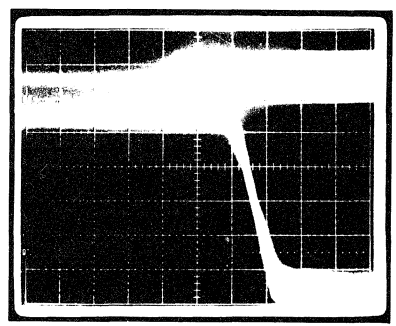


Fig.27 20ns input pulse. No video filter leading edge only. Horizontal = 2ns/div; -10dBm input level.

SL2521: LIMITING CHARACTERISTICS

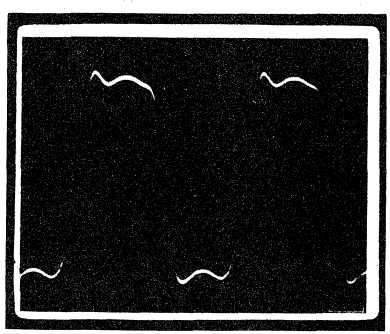


Fig.28 Hard limiting output at 200MHz with +10dBm input level

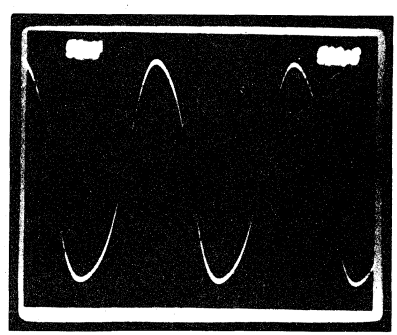


Fig.29 Hard limiting output at 500MHz with +10dBm input level

TYPICAL CHARACTERISTICS OF A SIX STAGE STRIP AS A LOW PHASE SHIFT WIDEBAND LIMITER

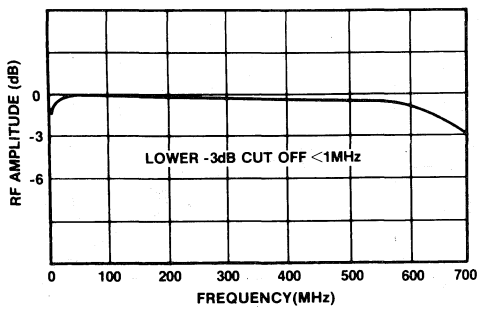


Fig.30 IF bandwidth measured from output 1. Output 2 terminated into 50Ω

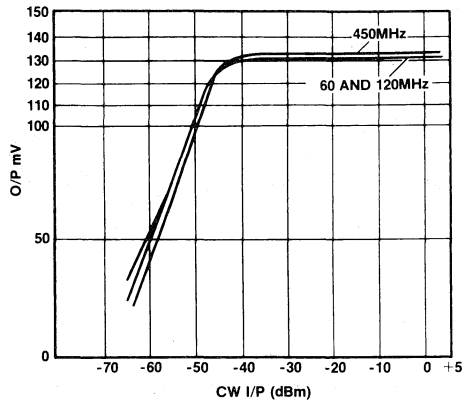


Fig.31 IF limiting characteristic at 60, 120 and 450MHz

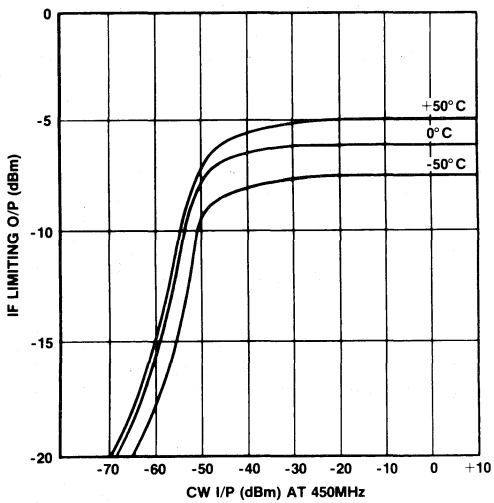


Fig.32 Limiting characteristic Vs temperature at 450MHz

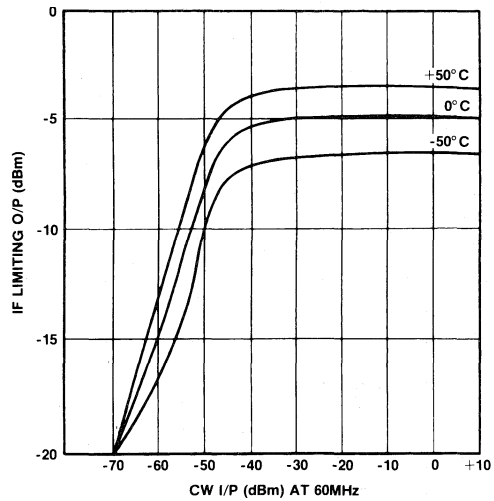


Fig.33 Limiting characteristic Vs temperature at 60MHz

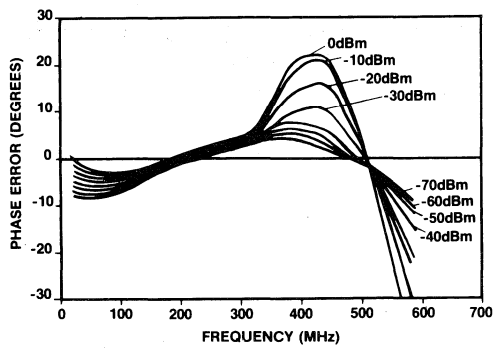


Fig.34 Departure from linear phase

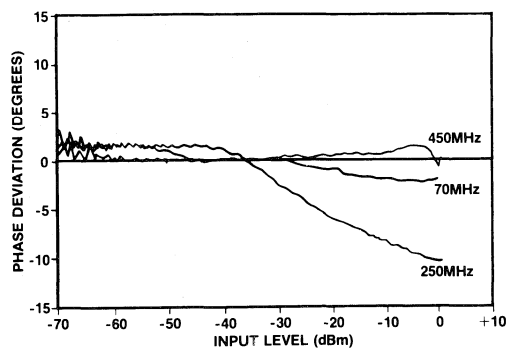


Fig.35 Normalised phase Vs input level

WIDEBAND LIMITER CHARACTERISTICS

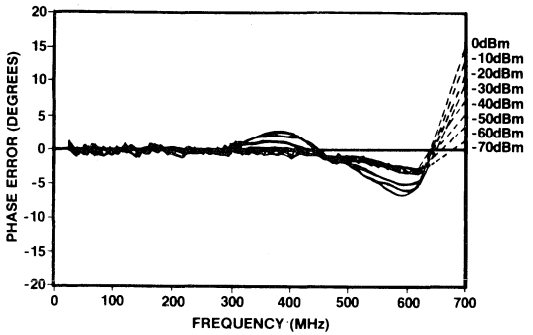


Fig.36 Phase tracking Vs frequency of two SD log strips (typical)

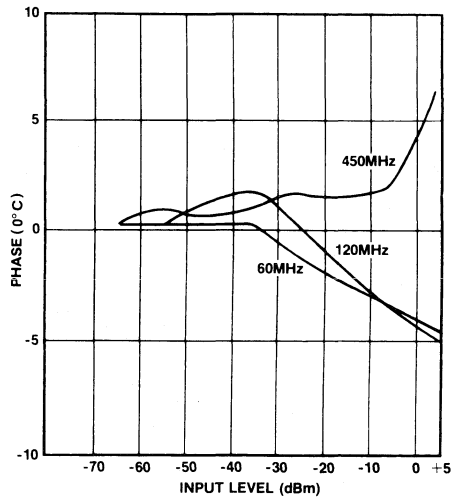


Fig.37 Phase change Vs input level at 60, 120 and 450MHz

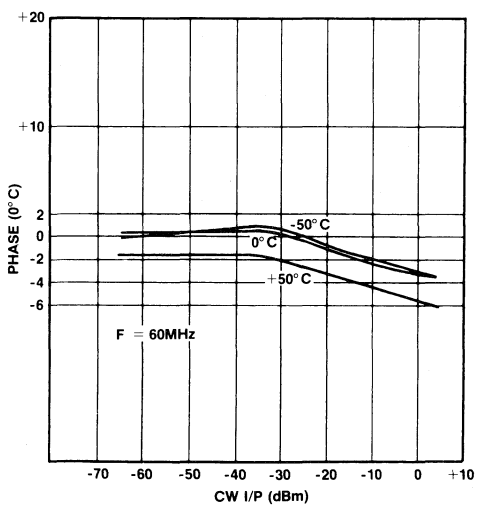


Fig.38 Phase change Vs temperature at 60MHz

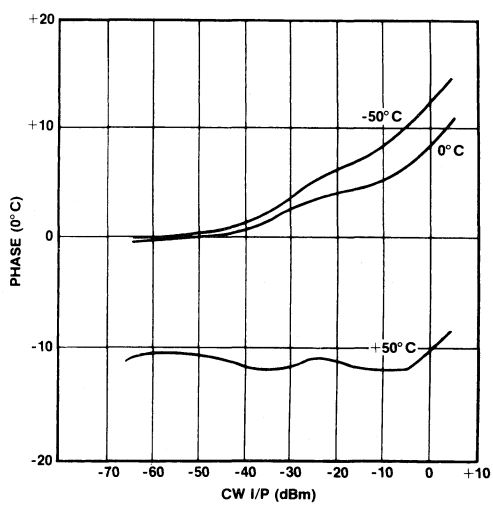


Fig.39 Phase change Vs temperature at 450MHz

IMPEDANCE OR ADMITTANCE CO-ORDINATES

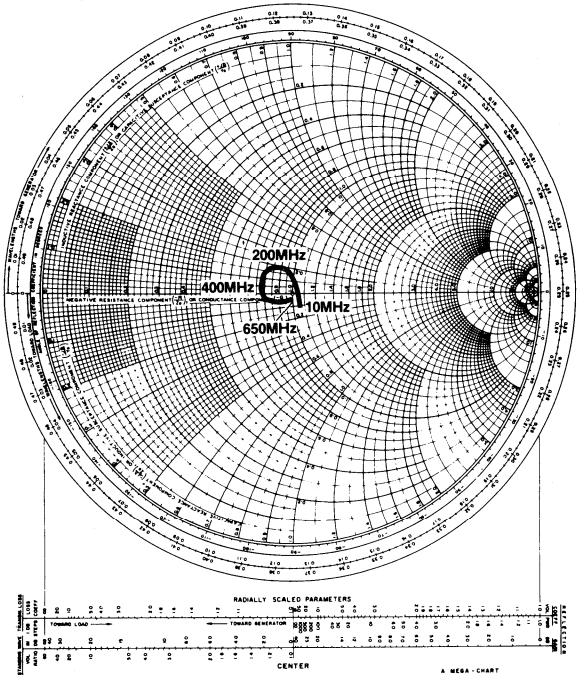


Fig.40 Output impedance (typical)

IMPEDANCE OR ADMITTANCE CO-ORDINATES

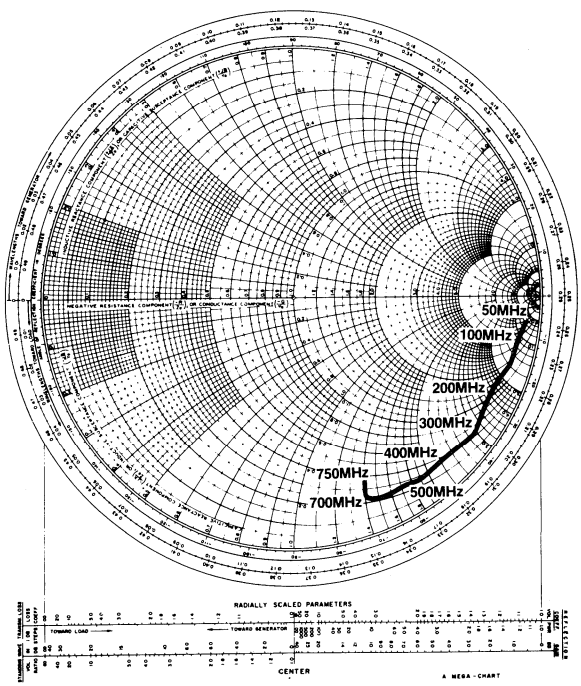


Fig.41 Input impedance (typical)

SL2521C

1.0GHz DUAL WIDEBAND LOGARITHMIC AMPLIFIER

(NOT RECOMMENDED FOR NEW DESIGNS - TO BE REPLACED BY SL2524)

The SL2521 is a revolutionary monolithic integrated circuit designed on an advanced 3 micron oxide isolated bipolar process. The amplifier is a successive detection type which provides linear gain and accurate logarithmic signal compression over a wide bandwidth.

When six stages (three SL2521s) are cascaded the strip can be used for IFs between 30-650MHz whilst achieving greater than 65dB dynamic range with a log accuracy of $<\pm 1.0$dB. The balanced limited output also offers accurate phase information with input amplitude. One log strip therefore offers limited IF output, phase and video information.

FEATURES

- 1.0GHz Bandwidth (-3dB)
- Balanced IF Limiting
- 3ns Rise Times/5ns Fall Times (Six Stages)
- 20ns Pulse Handling (Six Stages)
- Temperture Stabilised
- Surface Mountable

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Applications

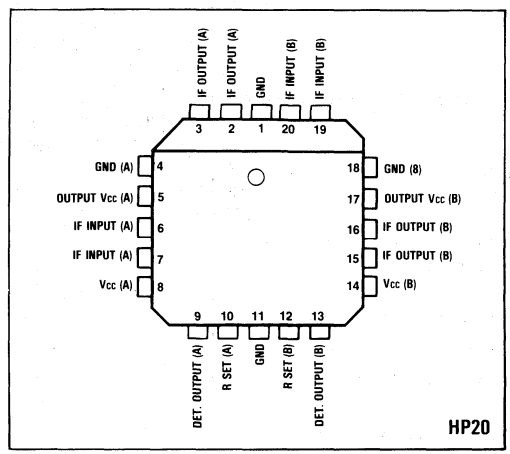


Fig.1 Pin connections - top view

ORDERING INFORMATION

SL2521 C HP
Military version available:
SL2522 AC LC
SL2522 BC LC

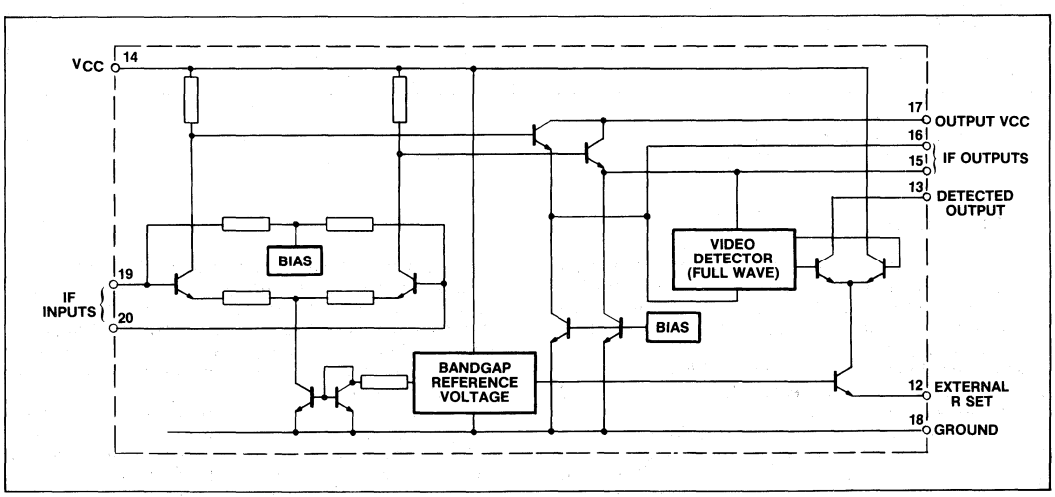


Fig.2 Circuit diagram (single stage B only)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Frequency = 200MHz, T_{amb} = -30°C to +85°C, Input voltage = -30dBm, V_{CC} = 6V ± 0.1V, Source Impedance = 50Ω, Test Circuit = Fig.3, R_{set} = 300Ω.

Characteristics	Value						Units	Conditions	Notes
	50Ω Load			1kΩ Load					
	Min.	Typ.	Max.	Min.	Typ.	Max.			
Small signal gain (dual stage, single ended)	8.7	10.7	12.7	14.3	16.5	19.2	dB	T_{amb} = -30°C frequency = 200MHz	2
	9.3	11.0	12.7	15.3	17.0	18.7	dB	T_{amb} = +25°C frequency = 200MHz	
	9.2	11.2	12.9	15.3	17.3	19.3	dB	T_{amb} = +85°C frequency = 200MHz	2
	9.4	11.5	13.7	15.6	18.1	20.6	dB	T_{amb} = -30°C frequency = 500MHz	2
	9.7	11.4	13.2	15.8	18.0	20.3	dB	T_{amb} = +25°C frequency = 500MHz	
	9.2	11.2	13.2	15.1	17.6	20.1	dB	T_{amb} = +85°C frequency = 500MHz	2
Detected output current (max)	2.95	3.25	3.55	3.10	3.45	3.8	mA	T_{amb} = -30°C, V_{in} = 0dBm, f = 200MHz	2
	3.05	3.3	3.55	3.2	3.5	3.8	mA	T_{amb} = +25°C, V_{in} = 0dBm, f = 200MHz	
	3.0	3.3	3.5	3.2	3.55	3.9	mA	T_{amb} = +85°C, V_{in} = 0dBm, f = 200MHz	2
	2.7	3	3.3	2.7	3	3.3	mA	T_{amb} = -30°C, V_{in} = 0dBm, f = 500MHz	2
	2.8	3.05	3.55	2.7	3	3.3	mA	T_{amb} = +25°C, V_{in} = 0dBm, f = 500MHz	
	2.75	3.03	3.75	2.7	3	3.3	mA	T_{amb} = +85°C, V_{in} = 0dBm, f = 500MHz	2
Detected output current (no signal)				0.8	1.2	1.4	mA	T_{amb} = -30°C	2
				0.85	1.2	1.35	mA	T_{amb} = +25°C	
				0.8	1.2	1.4	mA	T_{amb} = +85°C	2
Upper cut off frequency (RF)					1000		MHz	-3dB w.r.t. 200MHz, T_{amb} = +25°C	1
Lower cut off frequency (RF)					0.35	2	MHz		
Detector cut off frequency					600		MHz	50% O/P current w.r.t. 200MHz	
Limited IF O/P voltage				90	120	160	mV	I/P voltage = 0dBm, T_{amb} = +25°C	
Phase variation with input level (normalised to -30dBm)		±2					Degree	Frequency = 70MHz, -55 to +3dBm	
		±4					Degree	Frequency = 200MHz, -55 to +3dBm	
Limited O/P var with temp.		±12					mV		
Noise figure		12			9		dB		
Max I/P before overload					15		dBm		
Input impedance					1		kΩ	1kΩ in parallel with 2pF	
Output impedance					40		Ω		
Supply current			90		75	90	mA		
Variation of max detected current with V_{CC}					5		%/V	T_{amb} = +25°C	
Variation of small signal gain with V_{CC}					0.5		dB/V	T_{amb} = +25°C	

NOTES
1. Parameter guaranteed but not tested.
2. Tested at 25°C only, but guaranteed at temperature.

GENERAL DESCRIPTION

The SL2521 is primarily intended for use in Radar and EW receivers. Six stages (3 chip carriers) can be cascaded to form a very wideband logarithmic amplifier offering >65dB of input dynamic range, with pulse handling of better than 25ns. (See Figs.4 and 5.)

A six stage strip also offers balanced IF limiting, linearity (log accuracy) of <±1.0dB, temperature stabilisation and programmable detector characteristics.

The detector has an external resistor set pin which allows the major characteristics of the detector to be programmed. With a six stage strip it is possible to vary the value of R_{set} on each detector and so improve the overall log error/linearity.

The detector is full wave and good slew rates are achieved with 2ns rise and 5ns fall times (no video filter). The video bandwidth for a six stage strip is typically 600MHz (-3dB).

The amplifier also offers balanced IF limiting, low phase shift versus input amplitude, and at an IF of 120MHz, less than 7° of phase change is achievable over the input level of -55dBm to +5dBm.

The IF and Video ports can be used simultaneously so offering phase, frequency and pulse (video) information. A slight loss of dynamic range (2dB) will be observed when the IF ports are used in conjunction with the video.

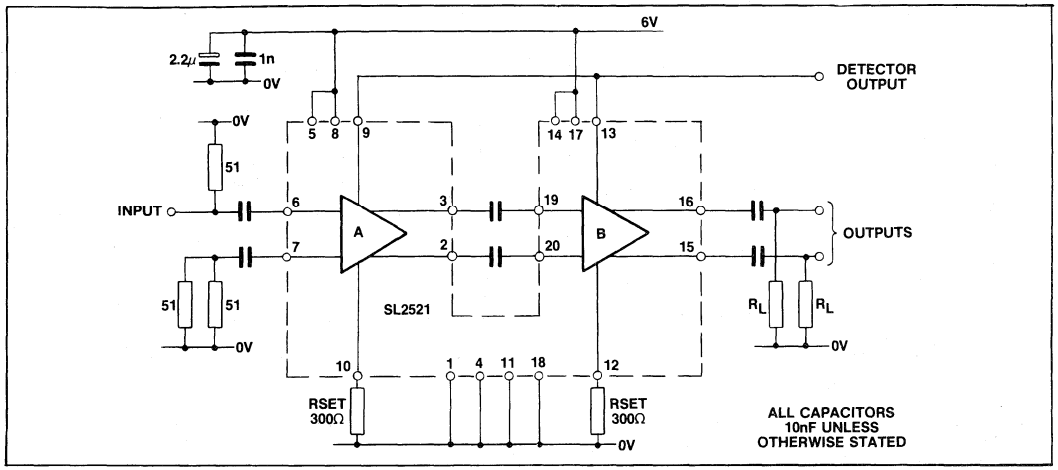


Fig.3 Test circuit

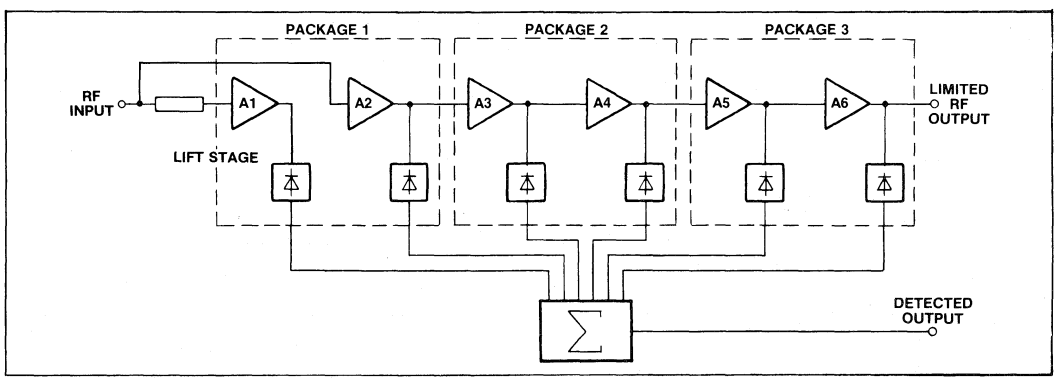


Fig.4 Schematic diagram showing configuration of SD amplifier

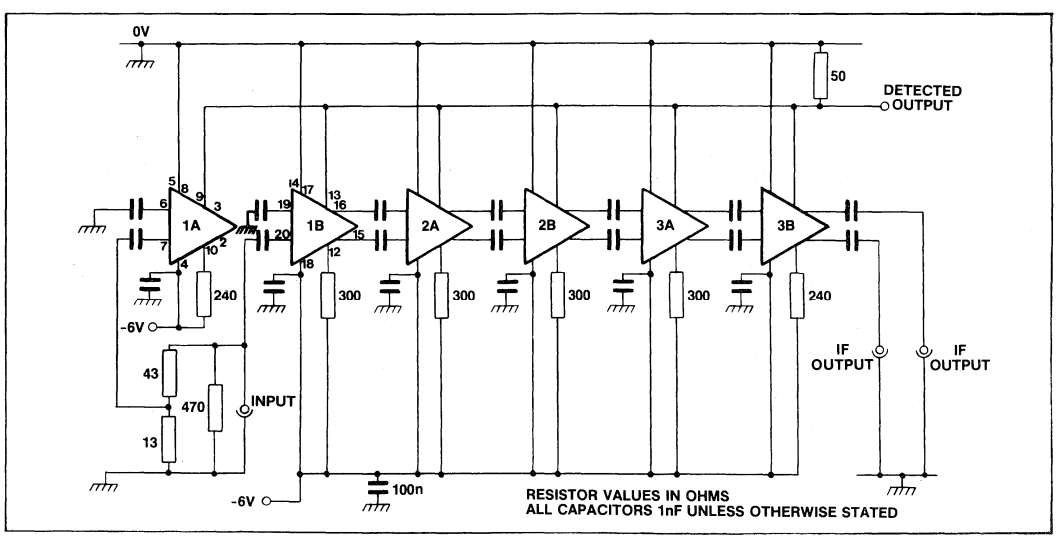


Fig. 5 Circuit diagram for 6-stage log strip (results shown in Figs. 18 to 35 were achieved with this circuit)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER (i.e. 1 SL2521)

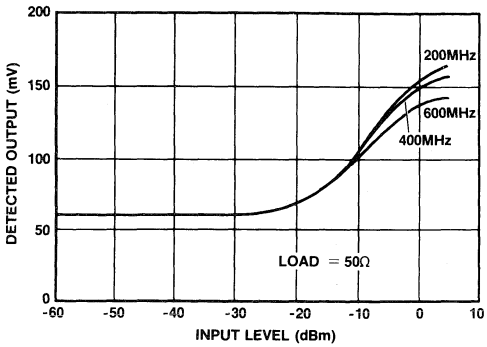


Fig.6 Detected O/P Vs input level at 200,400,600MHz for $R_L = 50\Omega$

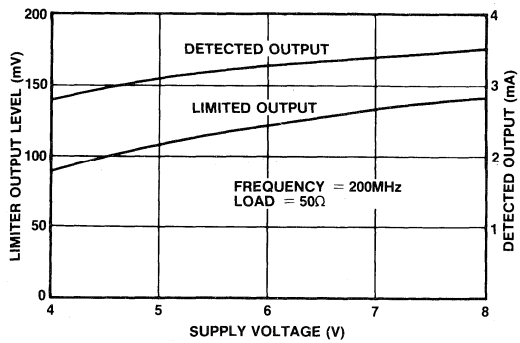


Fig.7 Output levels Vs supply voltage

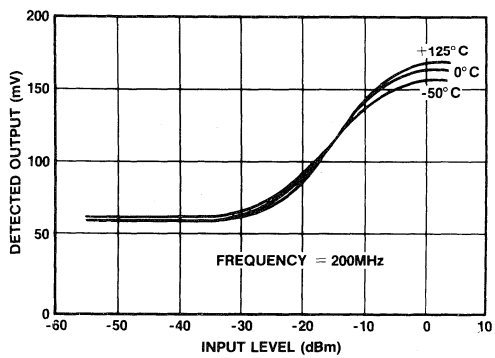


Fig.8 Detected output Vs input level and temperature

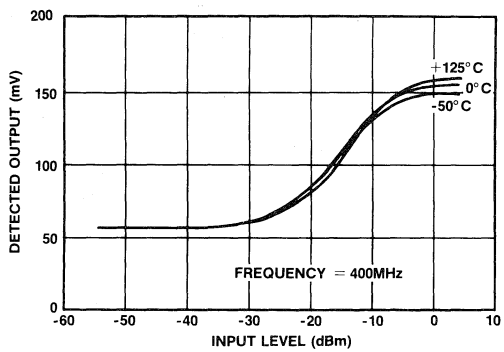


Fig.9 Detected output Vs input level and temperature

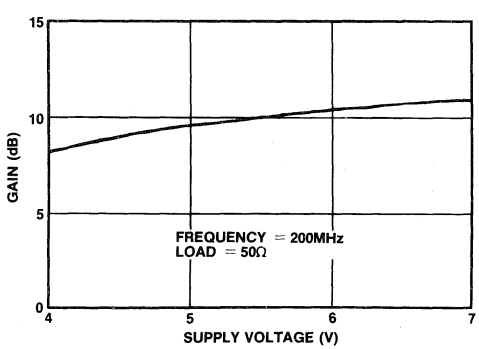


Fig.10 Gain Vs supply voltage

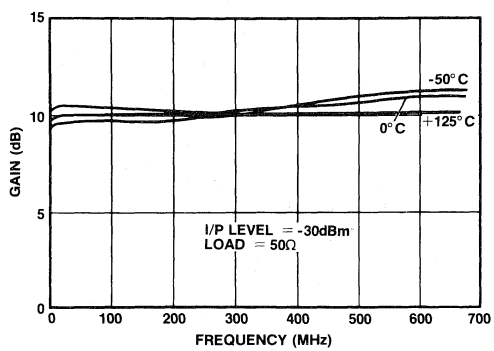


Fig.11 Gain Vs frequency of 2 amplifiers (1 SL2521)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER

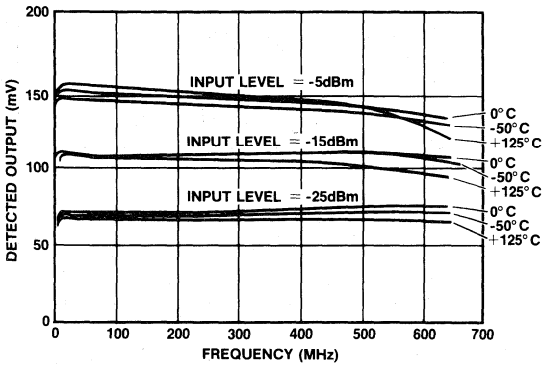


Fig.12 Detected output level Vs frequency and temperature

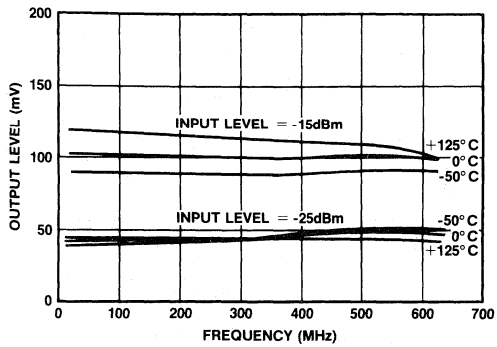


Fig.13 Limited output level Vs frequency and temperature

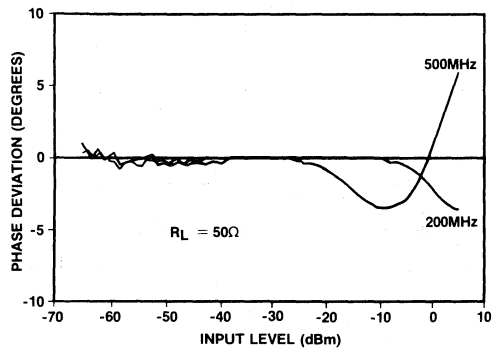


Fig.14 Normalised phase Vs input level at 200 and 500MHz for $R_L = 50\Omega$

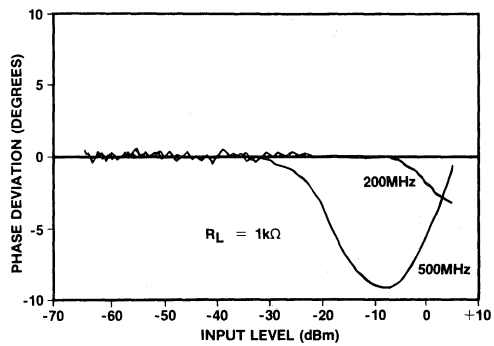


Fig.15 Normalised phase Vs input level at 200 and 500MHz for $R_L = 1k\Omega$

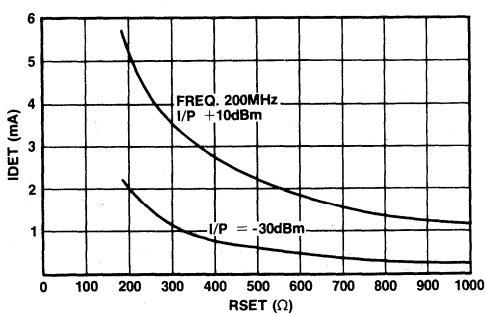


Fig.16 Detector current Vs R_{set} at 200MHz

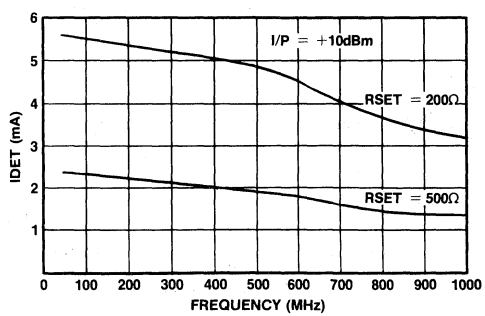


Fig.17 Detector current Vs frequency at $R_{set} = 200\Omega$ and 500Ω

TYPICAL CHARACTERISTICS FOR A SIX STAGE STRIP, USING THE VIDEO OUTPUT

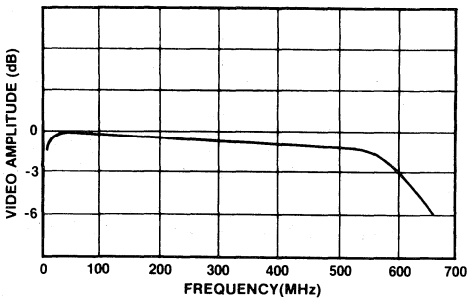


Fig.18 Video bandwidth (detector)

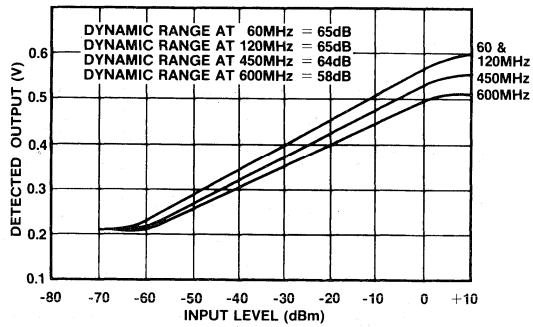


Fig.19 Video output Vs CW input at 60, 120, 450 and 600MHz at 25° C

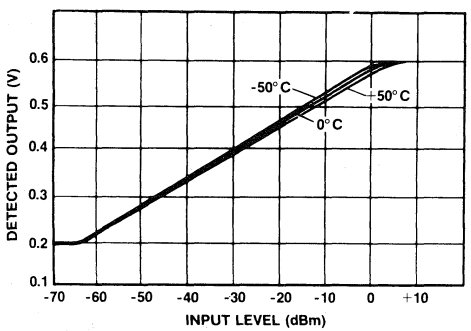


Fig.20 Detected output Vs input level and temperature at 60, 120MHz

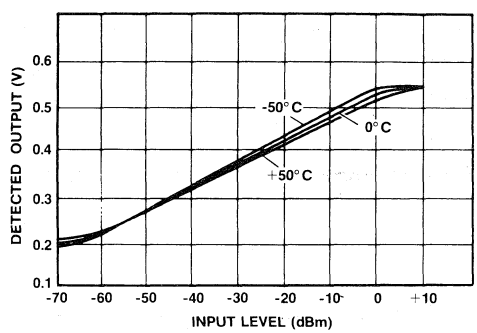


Fig.21 Detected output Vs input level and temperature at 450MHz

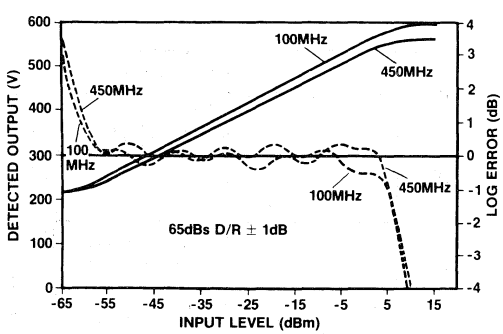


Fig.22 Detected O/P and log linearity at 450 and 100MHz

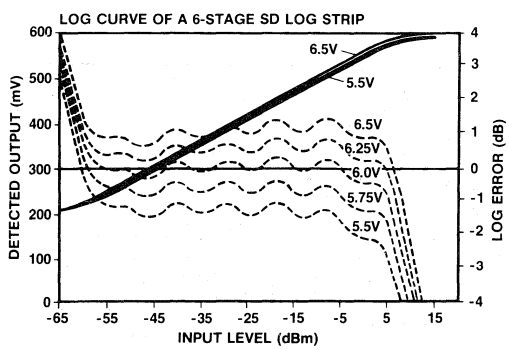


Fig.23 Logarithmic output Vs V_{CC}

SL2521: PULSE FIDELITY FOR A SIX STAGE STRIP

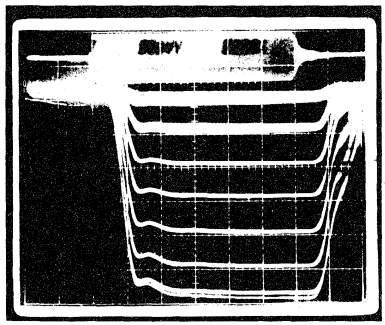


Fig.24 60ns I/P pulse. With low pass video filter. Horizontal = 10ns/div. Vertical = 50mV/div. Input level -70dBm to -10dBm

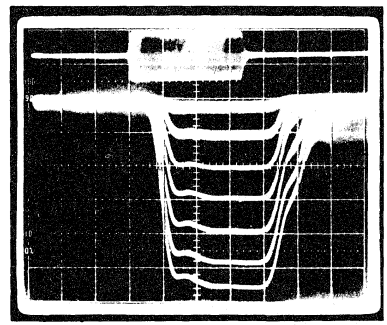


Fig.25 As Fig.25 with 35ns input pulse (Slight glitch on front edge is due to underdamping of video filter)

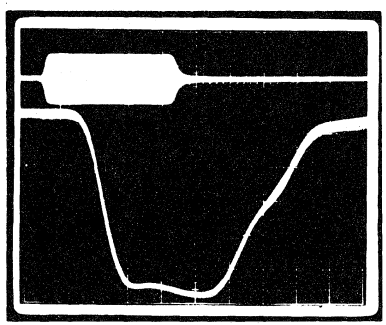


Fig.26 20ns input pulse. Showing input and output pulse with low pass video filter. Horizontal = 5ns/div. Vertical = 50mV/div; -10dBm input.

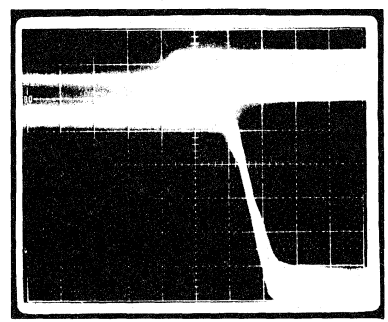


Fig.27 20ns input pulse. No video filter leading edge only. Horizontal = 2ns/div; -10dBm input level.

SL2521: LIMITING CHARACTERISTICS

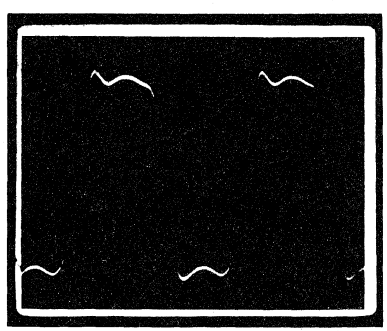


Fig.28 Hard limiting output at 200MHz with +10dBm input level

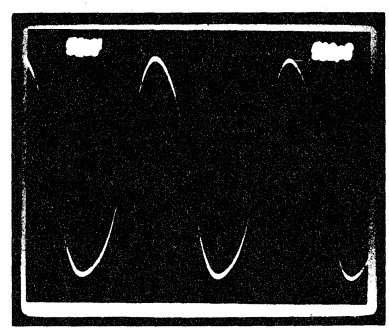


Fig.29 Hard limiting output at 500MHz with +10dBm input level

TYPICAL CHARACTERISTICS OF A SIX STAGE STRIP AS A LOW PHASE SHIFT WIDEBAND LIMITER

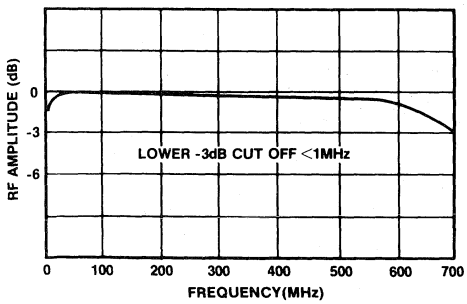


Fig.30 IF bandwidth measured from output 1. Output 2 terminated into 50Ω

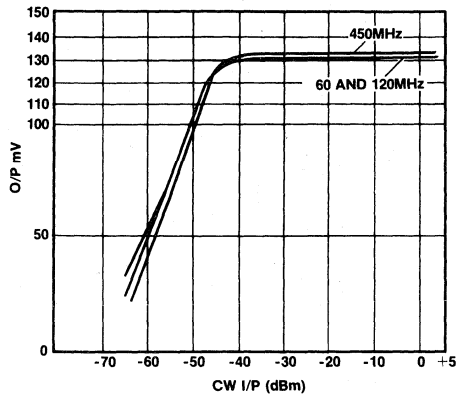


Fig.31 IF limiting characteristic at 60, 120 and 450MHz

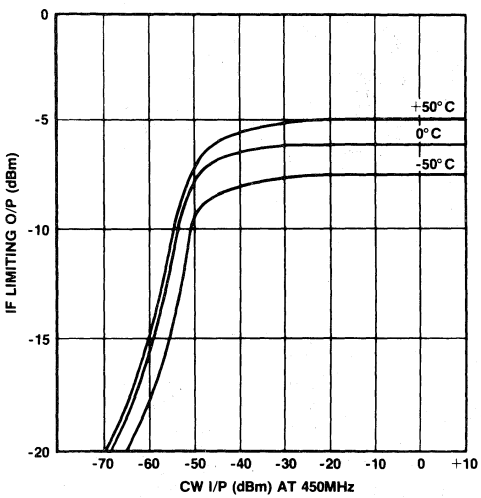


Fig.32 Limiting characteristic Vs temperature at 450MHz

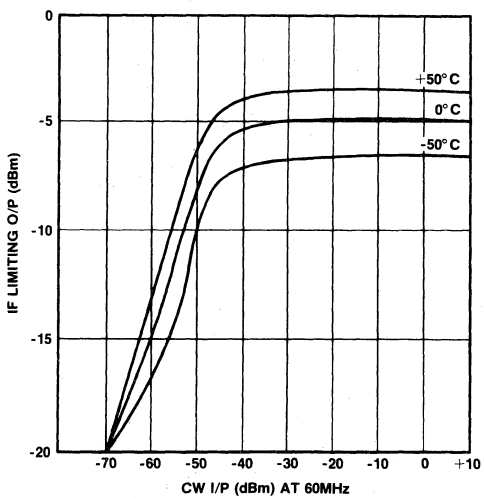


Fig.33 Limiting characteristic Vs temperature at 60MHz

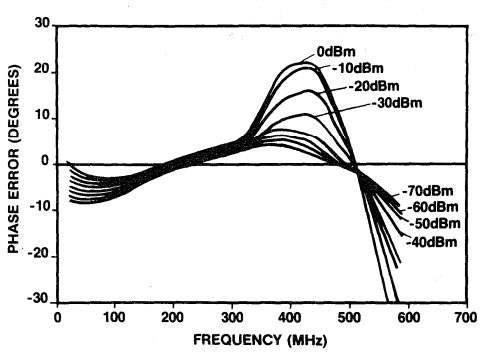


Fig.34 Departure from linear phase

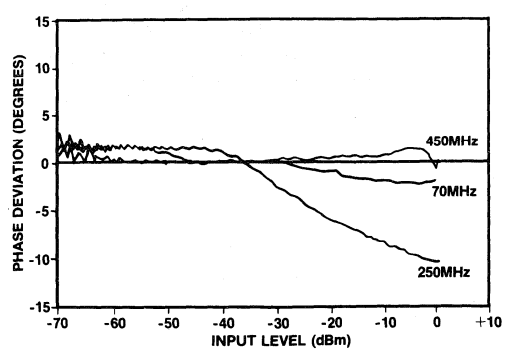


Fig.35 Normalised phase Vs input level

WIDEBAND LIMITER CHARACTERISTICS

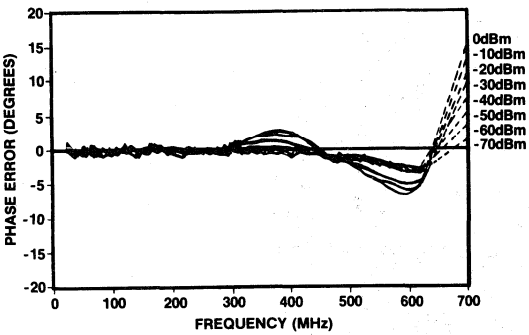


Fig.36 Phase tracking Vs frequency of two SD log strips (typical)

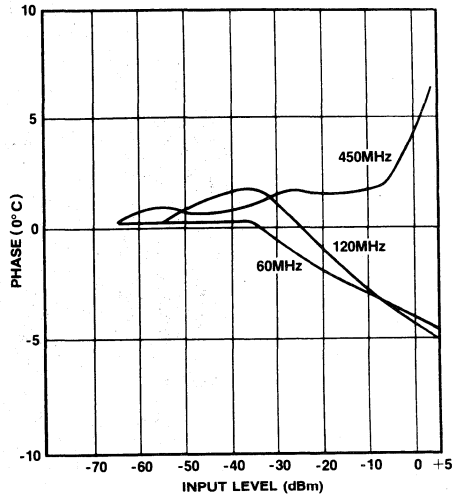


Fig.37 Phase change Vs input level at 60, 120 and 450MHz

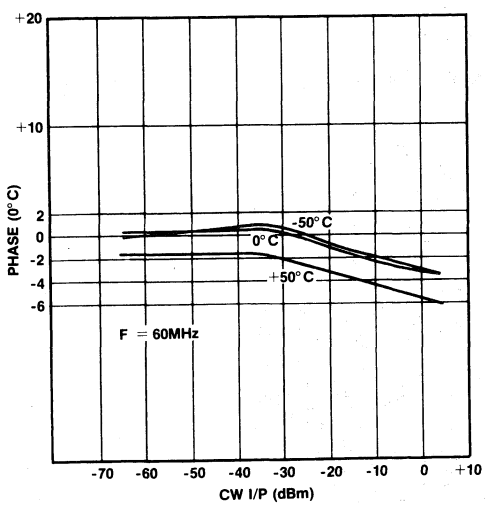


Fig.38 Phase change Vs temperature at 60MHz

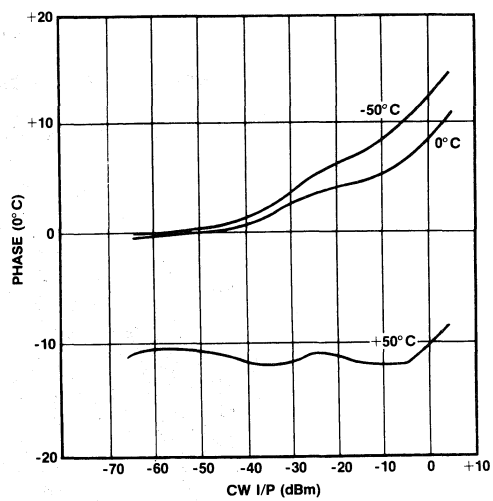


Fig.39 Phase change Vs temperature at 450MHz

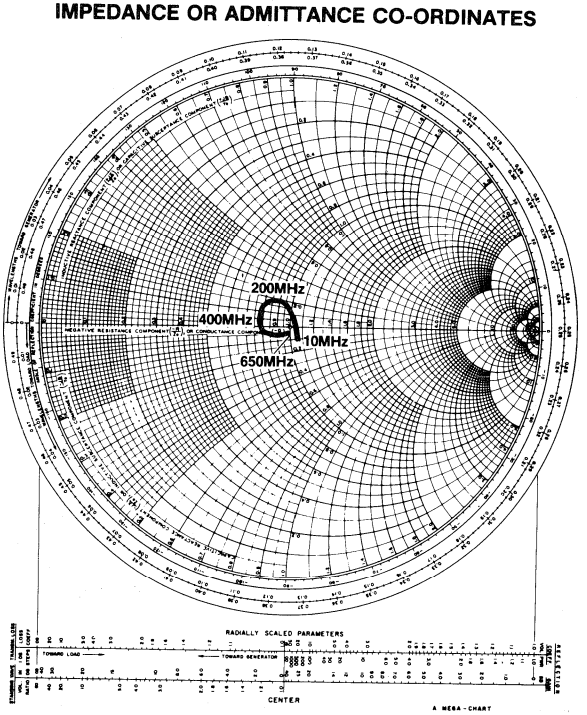


Fig.40 Output impedance (typical)

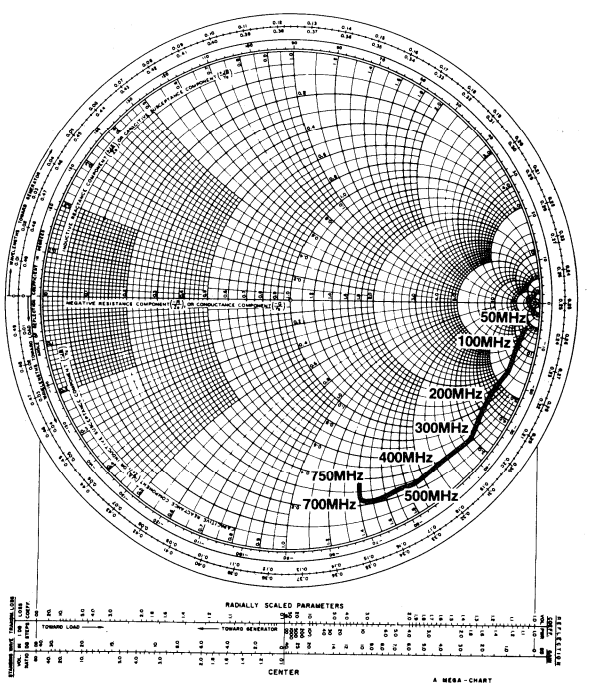


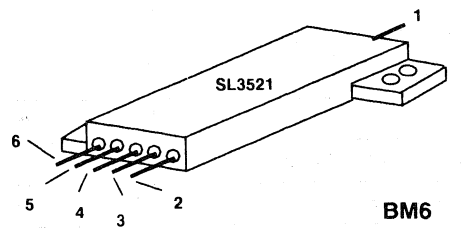
Fig.41 Input impedance (typical)

SL3521

75dB RANGE LOGARITHMIC AMPLIFIER

(Supersedes May 1990 Edition)

The SL3521 is a successive detection logarithmic amplifier, capable of operating from 100MHz to 650MHz. It consists of a monolithic chip mounted on a hybrid substrate. Bypassing capacitors and thick film resistors are also included. An attractive feature is its extremely small size - less than 0.04cu.ins. (0.7x0.36x0.16ins). The wide bandwidth, low power consumption, and high accuracy plus the inherent reliability of monolithic integrated circuits, make the SL3521 an attractive part for modern Radar and Electronic Warfare equipment.



Pin	Function
1	RF INPUT
2	OFFSET ADJUST
3	-5V V_{EE}
4	GROUND
5	+5V V_{CC}
6	VIDEO OUTPUT

Fig.1 Pin Connections

FEATURES

- Small Size: 0.04 cu ins (less mounting tabs)
- Low Power: 0.9 W max.
- Frequency Range: 100 - 650MHz
- High Accuracy: <0.75dB Error
- High Output Voltage: 2V
- Extremely High Stability with Temperature
- High Reliability because of Low Component Count
- -55 to 125°C Operating Temperature Range

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Radar

ORDERING INFORMATION

SL3521 A BM
SL3521 AC BM

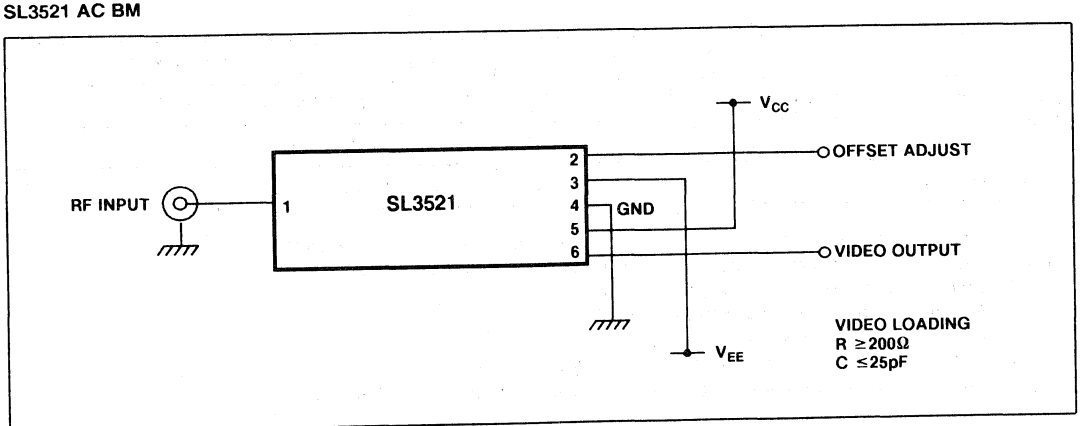


Fig.2 Test and application circuit (top view)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

V_{CC} = +5V ± 10%, V_{EE} = -5V ± 10% , $T_{mounting\ base}$ = -55°C to +125°C

Characteristic	Pin	Value			Units	Notes
		Min	Typ	Max		
Frequency Range	1	200		450	MHz	Note 7
Noise Bandwidth		150		500	MHz	-3dB
Input Level				+15	dBm	Without Damage
Noise Figure	1			10	dB	Note 3
Tangential Sensitivity		-76			dBm	
Video Output Range	2			2	Volts DC	
Video Slope	2	19		21	mV/dB	Note 1.
Video Bandwidth	2	30	40		MHz	Critically Damped Transient Response
Rise Time	2		22	25	ns	Settled to within +/-0.7%
RiseTime	2		14		ns	10% to 90% (60dB step)
Linearity	2	- 0.75		+ 0.75	dB	Deviation from best fit straight line Note 1.
Video Output Impedance	2			10	Ω	
Video Load Impedance	2	190			Ω	Max Cap = 25pF
Input VSWR	1	1		2		50Ω System
Positive Supply Current I_{CC} Negative Supply Current I_{EE}	3 5		25 150	35 175	mA mA	) at nominal) Supply Voltage
Conducted Emissions on Supply leads	3 5			- 60	dBm	0dBm RF input
Video Offset Adjustment Range	6	-0.5		+0.5	Volts	I/P = -70dBm Note 2.
Offset Adjust Output Impedance	2		1.4		kΩ	Note 4
Offset Adjust Voltage	2		-550		mV	Note 5
Offset Adjust gain	2		5		V6/V2	Note 6

Note 1. Measured between -65dBm and +5 over supply, temperature and frequency ranges
Note 2. Video offset is externally adjusted : after adjustment it is stable to ±20mV
Note 3. Derived from tangential sensitivity measurement
Note 4. Nominal impedance between offset ADJ and GND
Note 5. Nominal bias on offset adjust
Note 6. Voltage gain between video output and offset adjust
Note 7. Frequency range over which log accuracy and dynamic range is guaranteed

The SL3521 is a very easy device to use, requiring only to be attached to a suitable mounting face and supplies which may be applied in any order. However, a few points should be noted:-

1. The capacitive load of 25pF on the video output should not be exceeded: to do so may restrict video bandwidth.

2. The input pin must be at 0 Volts i.e. DC isolated.

3. Offset adjustment may be made by applying a voltage to the offset pin. This Voltage will be in the range -0.45V to -0.55V and should not be such as to increase the output offset to more than ±0.5V: to do so may impair the dynamic range. The impedance to ground is of the order of 1500Ω. Because of the gain between offset input and output, the offset supply must be well filtered.

4. Devices may be supplied adjusted for a customer specified DC output for a -70dBm RF input. Please contact your local Plessey Sales Office for details.

5. Internal supply bypassing is incorporated, giving some 40dB of rejection for frequencies above 100kHz. For extra rejection of low frequency ripple, extra filtering should be provided.

6. The junction-to-case thermal resistance is approximately 11 °C/W.

ABSOLUTE MAXIMUM RATINGS

(Non-simultaneous)

Supplies:	+20% of Nominal
Chip temperature:	+150°C
Storage temperature	-65°C to +150°C
Input DC Voltage:	±0.05V
Input RF Power:	15dBm

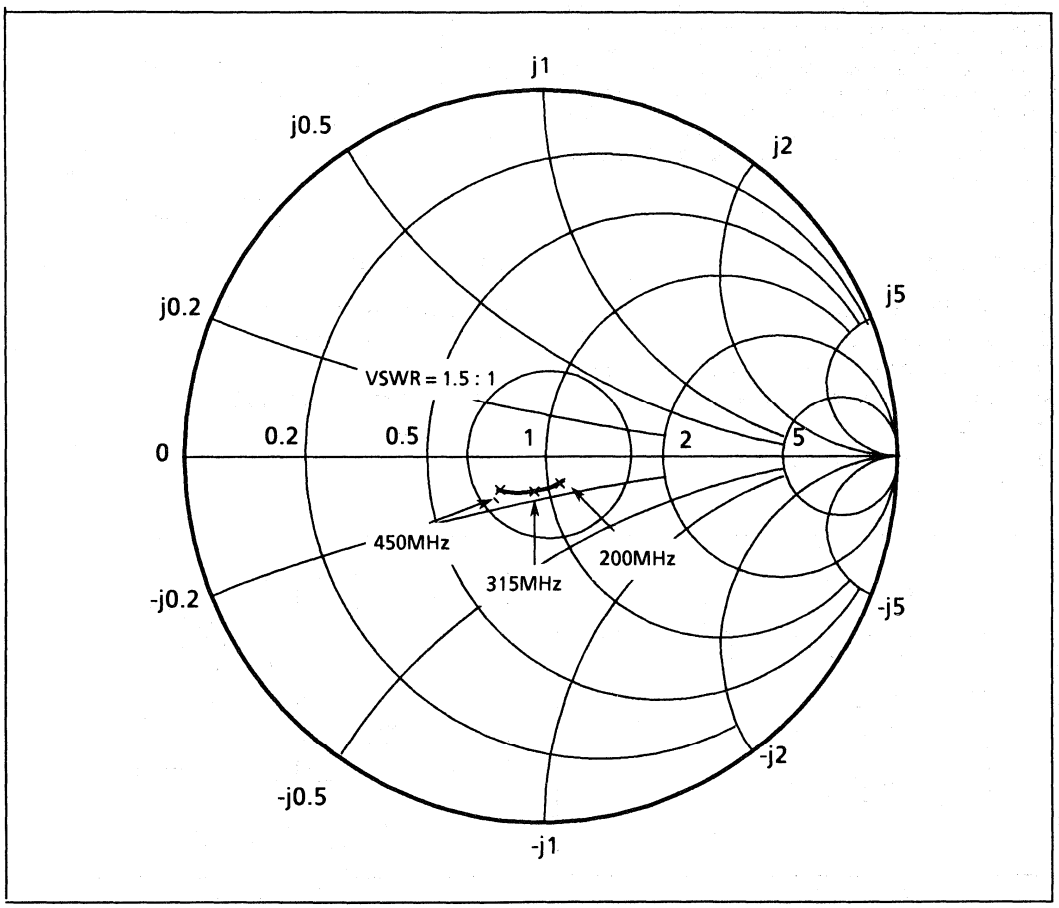


Fig.3 S11 - SL3521 - 50Ω system

SL550

LOW NOISE WIDEBAND AMPLIFIER WITH EXTERNAL GAIN CONTROL

The SL550 is a silicon integrated circuit designed for use as a general-purpose wideband linear amplifier with remote gain control. At a frequency of 60MHz, the SL550G noise figure is 1.8dB (typ.) from a 200 ohm source, giving good noise performance directly from a microwave mixer. The SL550 has an external gain control facility which can be used to obtain a swept gain function and makes the amplifier ideal for use either in a linear IF strip or as a low noise preamplifier in a logarithmic strip.

External gain control is performed in the feedback loop of the main amplifier which is buffered on the input and output, hence the noise figure and output voltage swing are only slightly degraded as the gain is reduced. The external gain control characteristic is specified with an accuracy of ±1dB, enabling a well-defined gain versus time law to be obtained.

The input transistor can be connected in common emitter or common base and the quiescent current of the output emitter follower can be increased to enable low impedance load to be driven.

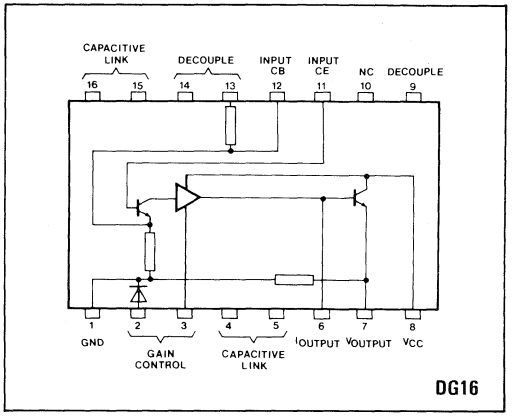


Fig. 1 Pin connections (top view)

FEATURES

- 200 MHz Bandwidth
- Low Noise Figure
- Well-Defined Gain Control Characteristic
- 25dB Gain Control Range
- 40dB Gain
- Output Voltage 0.8Vp-p (Typ.)

APPLICATIONS

- Low Noise Preamplifiers
- Swept Gain Radar IFs

ORDERING INFORMATION

SL550 G DG
SL550 GB DG

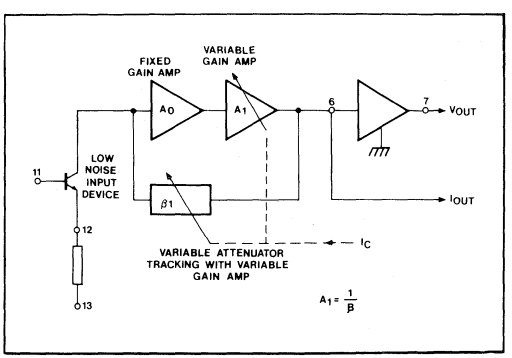


Fig. 2 Functional diagram

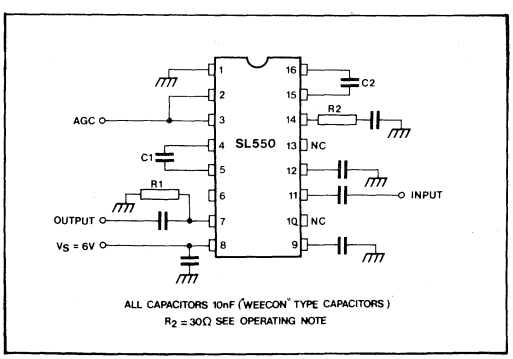


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
f = 30MHz, V_S = +6V, R_L = 200Ω, I_C = 0, R_1 = 750Ω, T_{amb} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	39	42	44	dB	
Gain control characteristic		See Note 1			
Gain reduction at mid-point		10		dB	I_C = 0.24mA
Max. gain reduction	20	25		dB	I_C = 2.0mA
Noise figure		2.0	2.7	dB	R_S = 200Ω
		3.5		dB	R_S = 50Ω
Output voltage		0.15		Vrms	R_1 = ∞
		0.3		Vrms	R_1 = 750Ω
Supply current		11	13	mA	R_1 = ∞
		15		mA	R_1 = 750Ω
Gain variation with supply voltage		0.2		dB/V	V_S = 6V to 9V
Upper cut-off frequency (-3dB w.r.t. 30MHz)		125		MHz	
Gain variation with temperature (see Note 2)		±3		dB	T_{AMB} = -40°C to +85°C

NOTES
1. The external gain control characteristic is specified in terms of the gain reduction obtained when the control current (I_C) is increased from zero to the specified current.
2. This can be reduced by using an alternative input configuration (see operating note: 'Wide Temperature Range').

OPERATING NOTES

Input Impedance

The input capacitance, which is typically 12pF at 60MHz, is independent of frequency. The input resistance, which is approximately 1.5k at 10MHz, decreases with frequency and is typically 500 ohms at 60MHz.

Control Input

Gain control is normally achieved by a current into pin 2. Between pin 2 and ground is a forward biased diode and so the voltage on pin 2 will vary between 600 mV at I_C = 1μA to 800 mV at I_C = 2 mA. The amplifier gain is varied by applying a voltage in this range to pin 3. To avoid problems associated with the sensitivity of the control voltage and with operation over a wide temperature range the diode should be used to convert a control current to a voltage which is applied to pin 3 by linking pins 2 and 3.

Minimum Supply Current

If the full output swing is not required, or if high impedance loads are being driven, the current consumption can be reduced by omitting R_1 (Fig. 3). The function of R_1 is to increase the quiescent current of the output emitter follower.

High Output Impedance

A high impedance current output can be obtained by taking the output from pin 6 (leaving pin 7 open-circuit). Maximum output current is 2 mA peak and the output impedance is 350Ω.

Wide Temperature Range

The gain variation with temperature can be reduced at the expense of noise figure by including an internal 30Ω resistor in the emitter of the input transistor. This is achieved by decoupling pin 13 and leaving pin 12 open-circuit. Gain variation is reduced from ±3dB to ±1dB over the temperature range -40°C to +85°C (Figs. 6 and 7).

Low Input Impedance

A low input impedance (≃25Ω) can be obtained by connecting the input transistor in common base. This is achieved by decoupling pin 11 and applying the input to pin 12 (pin 13 open-circuit).

High Frequency Stability

Care must be taken to keep all capacitor leads short and a ground plane should be used to prevent any earth inductance common between the input and output circuits. The 30Ω resistor (pin 14) shown in the test circuit eliminates high frequency instabilities due to the stray capacitances and inductances which are unavoidable in a plug-in test system. If the amplifier is soldered directly into a printed circuit board then the 30Ω resistor can be reduced or omitted completely.

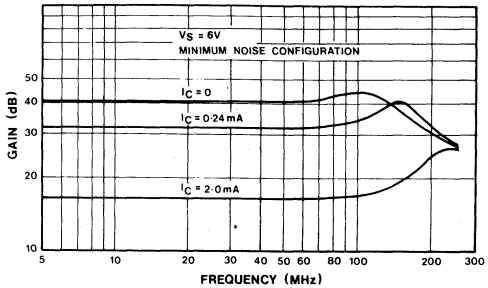


Fig. 4 Frequency response

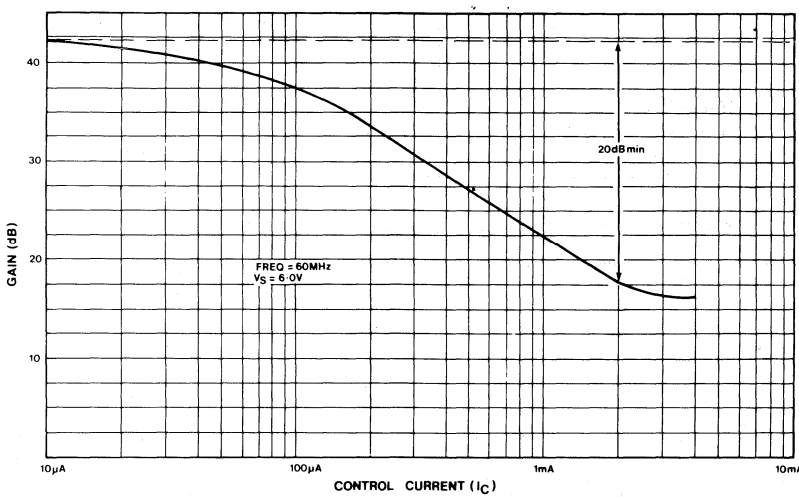


Fig. 5 Gain control characteristic

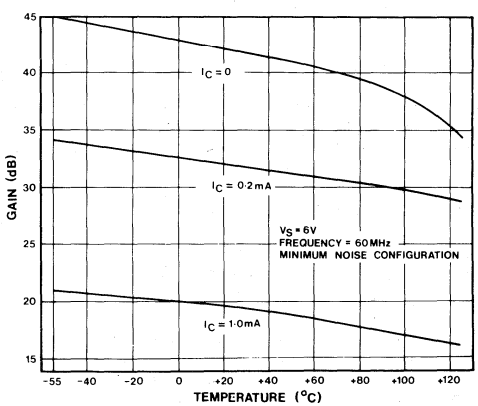


Fig. 6 Voltage gain v. temperature (pin 12 decoupled, standard circuit configuration)

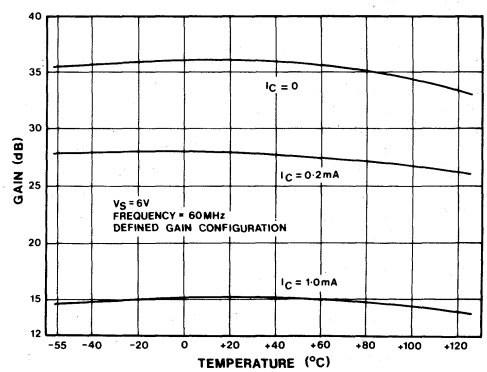


Fig. 7 Voltage gain v. temperature (pin 13 decoupled for improved gain variation with temperature – see operating notes)

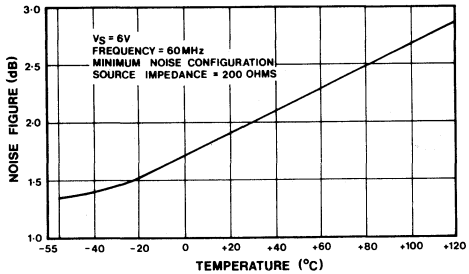


Fig. 8 Typical noise figure

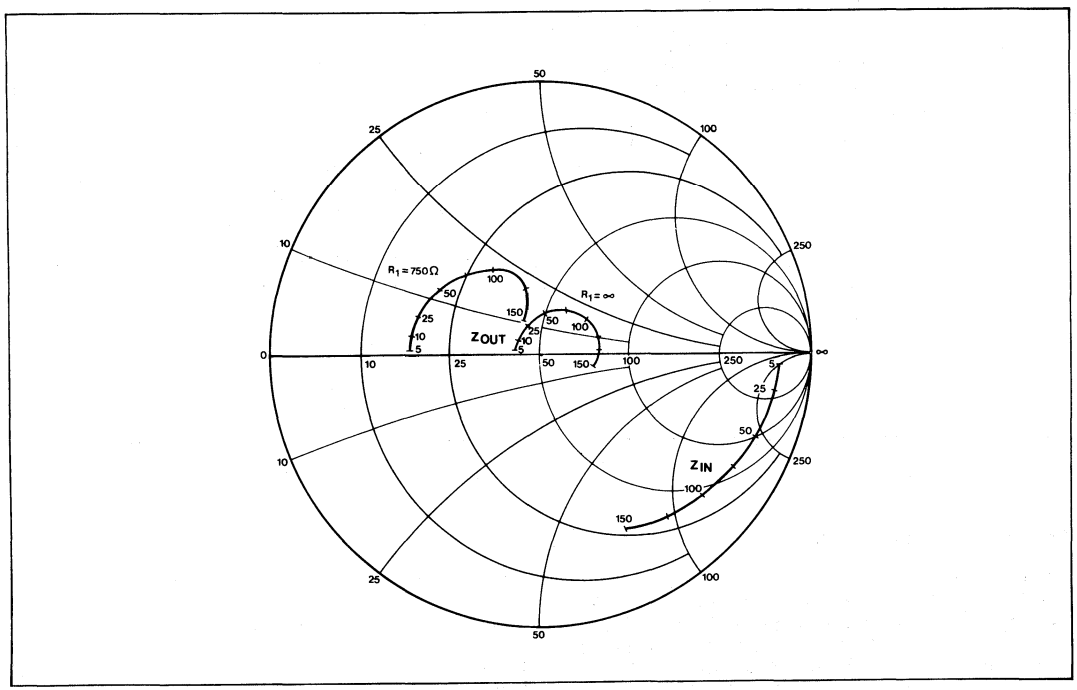


Fig.9 Input and output impedances (Vs = 6V)

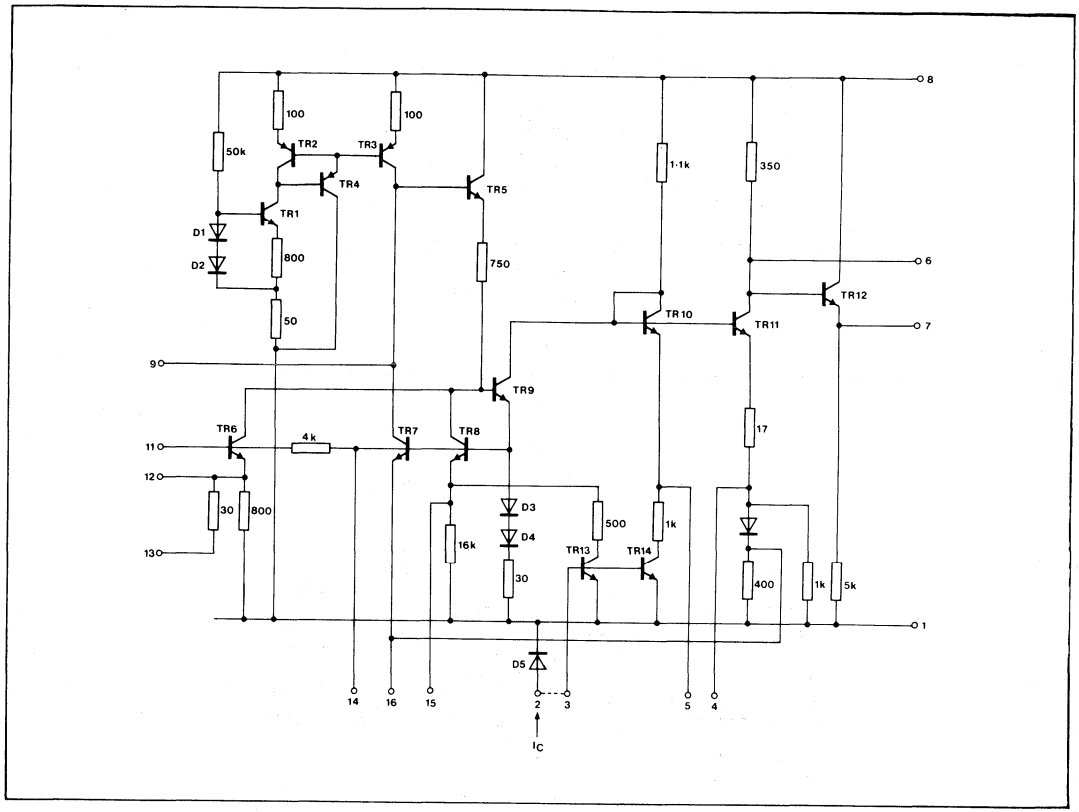


Fig.10 Circuit diagram

APPLICATION NOTES

A wideband high gain configuration using two SL550s connected in series is shown in Fig. 11. The first stage is connected in common emitter configuration, whilst the second stage is a common base circuit. Stable gains of up to 65 dB can be achieved by the proper choice of R1 and R2. The bandwidth is 5 to 130 MHz, with a noise figure only marginally greater than the 2.0 dB specified for a single stage circuit.

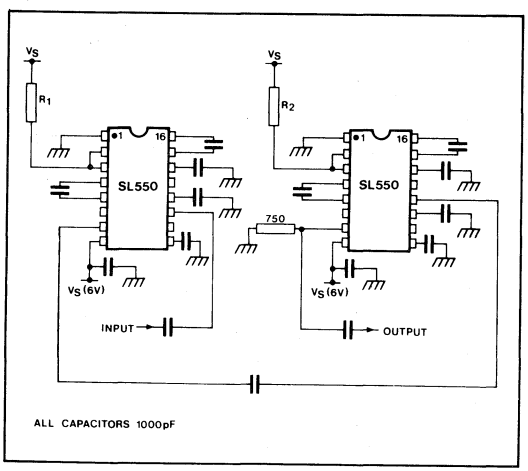


Fig. 11 A two-stage wide-band amplifier

A voltage gain control which is linear with control voltage can be obtained using the circuit shown in Fig. 12. The input is a voltage ramp which is negative going with respect to ground. The output drives the control current pins 2 and 3 directly (see Fig. 13). If two SL550s in the strip are controlled as shown in Fig. 14, with a linear ramp input to the linearising circuit, a fourth power law (power gain v. time) will be obtained over a 50 dB dynamic range.

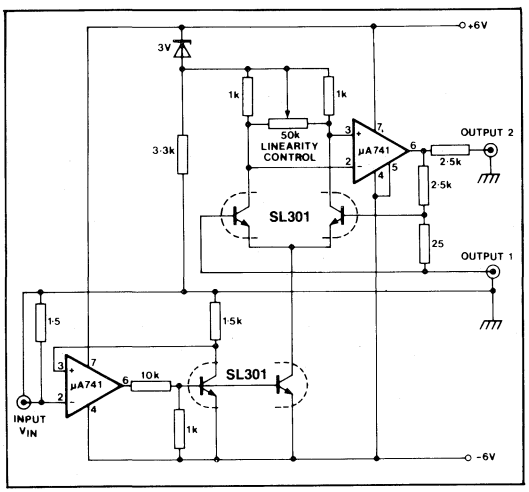


Fig. 12 Gain control linearising circuit

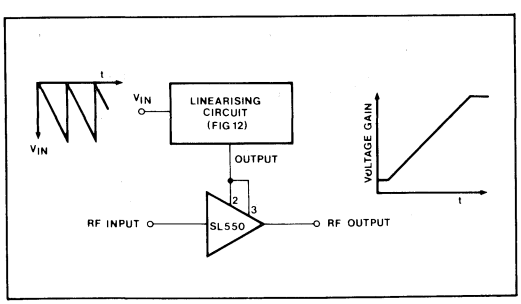


Fig. 13 Linear swept gain circuit

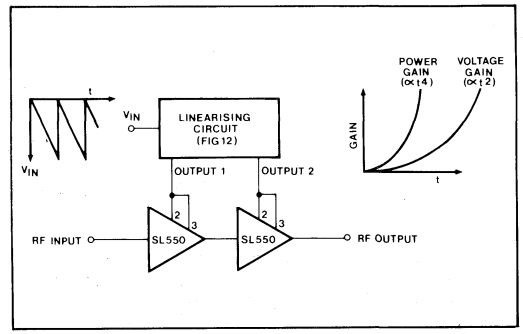


Fig. 14 Square law swept gain circuit

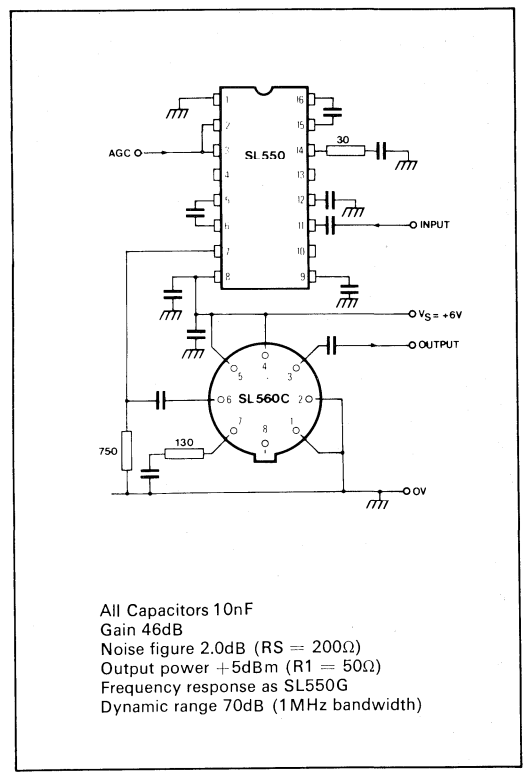


Fig. 15 Applications example of wide dynamic range: 50Ω load amplifier with AGC using SL500 series integrated circuit.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Ambient operating temp.	−40°C to +125°C
Max. continuous supply Voltage wrt pin 1	+9V
Max. continuous AGC current	
pin 2	10mA
pin 3	1mA

SL560

300MHz LOW NOISE AMPLIFIER

This monolithic integrated circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL560C is a general purpose low noise, high frequency gain block.

The device is also available as the SL560AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- Gain up to 40dB
- Noise Figure less than 2dB (Rs 200 ohm)
- Bandwidth 300MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Systems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wide Dynamic Range IF Amplifiers
- Aerial Preamplifiers for VHF TV and FM Radio

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pin 4)	+15V
Storage temperature	-55°C to 150°C (CM) -55°C to 125°C (DP)
Junction temperature	150°C (CM) 125°C (DP)
Thermal resistance	
Junction-case	60°C/W (CM)
Junction ambient	220°C/W (CM) 230°C/W (DP)
Maximum power dissipation	See Fig.15
Operating temperature range	-55°C to +125°C (CM) at 100mW -55°C to +100°C (DP) at 100mW

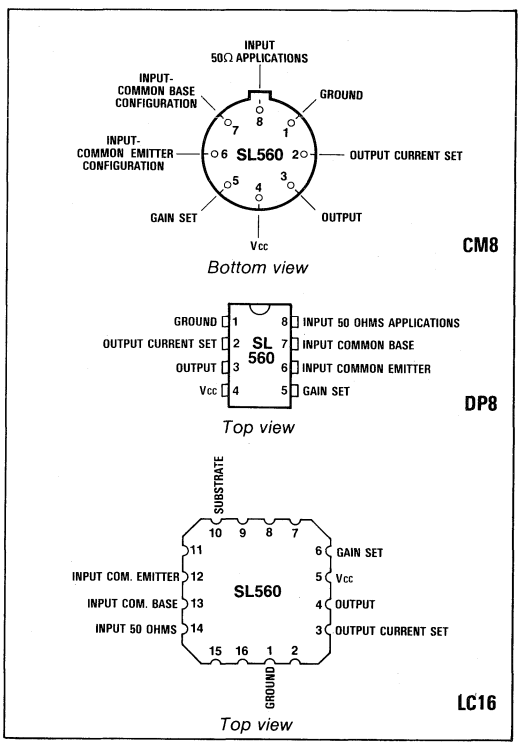


Fig.1 Pin connections

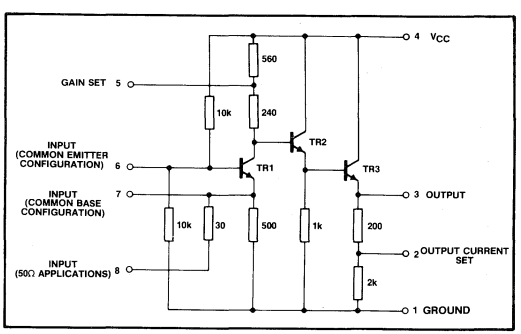


Fig.2 SL560C circuit diagram

ORDERING INFORMATION

SL560 AC CM
SL560 C CM
SL560 C DP
SL560 C LC
SL560 CB CM
SL560 C BSS2 NA CM

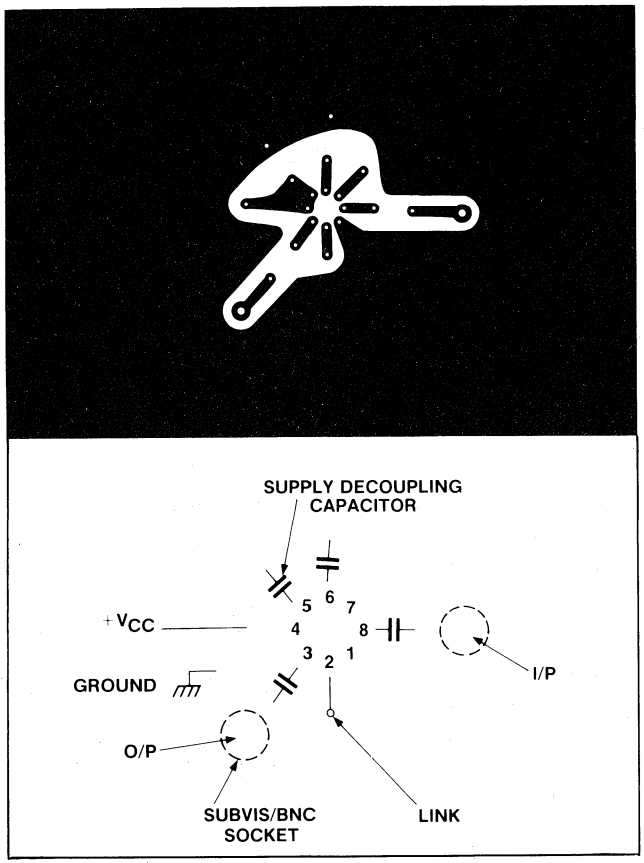


Fig.3 PC layout for 50Ω line driver (see Fig.6)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Frequency = 30MHz; V_{CC} = 6V; R_S = R_L = 50Ω; T_{amb} = 25°C; Test Circuit: Fig.6

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	14	17	dB	
Gain flatness		±1.5		dB	10MHz - 220MHz
Upper cut-off frequency		250		MHz	
Output swing	+5	+7		dBm	V_{CC} 6V } See Fig.5
		+11		dBm	V_{CC} = 9V }
Noise figure (common emitter)		1.8		dB	R_S = 200Ω
		3.5		dB	R_S = 50Ω
Supply current		20	30	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance ($R_{bb'}$) of 17Ω (for low noise operation) with a small physical size - giving a transition frequency, f_T, in excess of 1GHz.

The input transistor (TR1) is normally operated in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector is buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2dB noise figure (R_S = 200Ω) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 75MHz (see Figs. 8 and 9) or, using feedback 14dB with a bandwidth of 300MHz (see Figs. 10 and 11).

Because the transistors used in the SL560C exhibit a high value of f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be as short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

Further applications information is available in the 'Broadband Amplifier Applications' booklet.

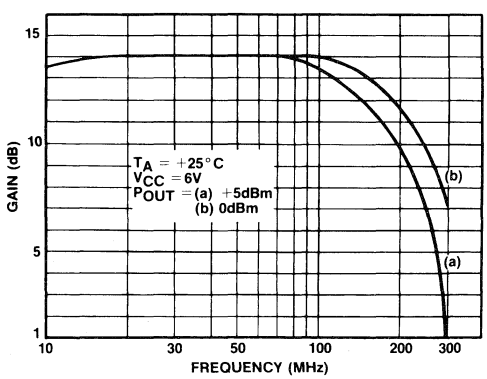


Fig.4 Frequency response, small signal gain is of a typical device

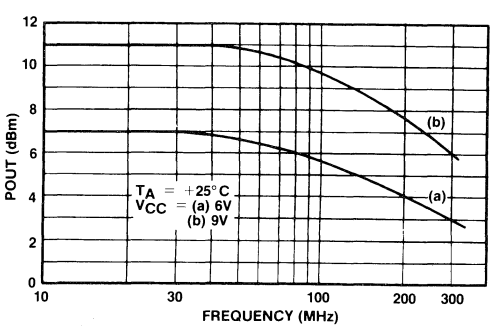


Fig.5 Frequency response, output capability (loci of maximum output power with frequency, for 1dB gain compression (typical)

TYPICAL APPLICATIONS

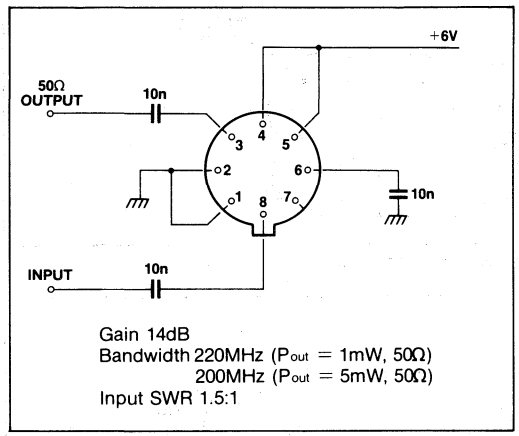


Fig.6 50Ω line driver. The response of this configuration is shown in Fig.4.

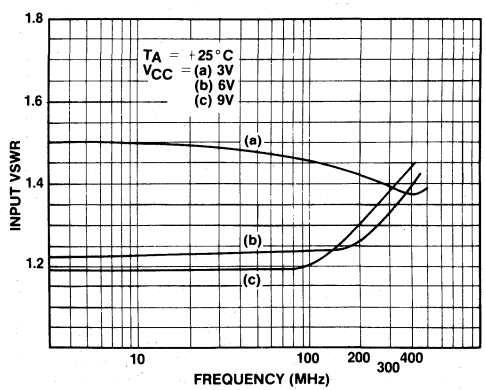


Fig.7 Input standing wave ratio plot of circuit shown in Fig.6 (typical)

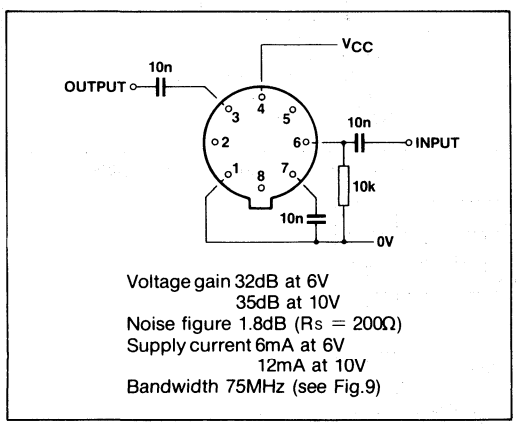


Fig.8 Low noise preamplifier

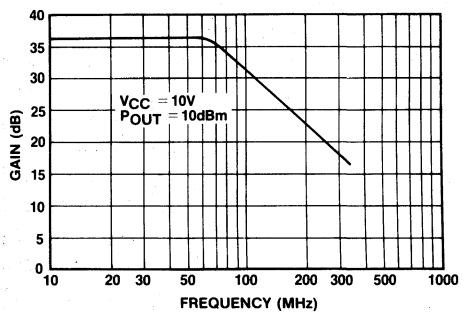


Fig.9 Frequency response of circuit shown in Fig.8 (typical)

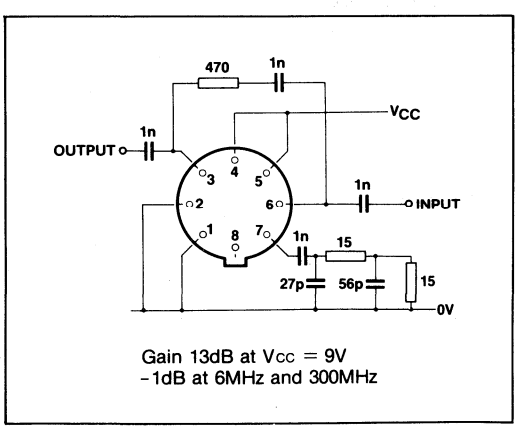


Fig.10 Wide bandwidth amplifier

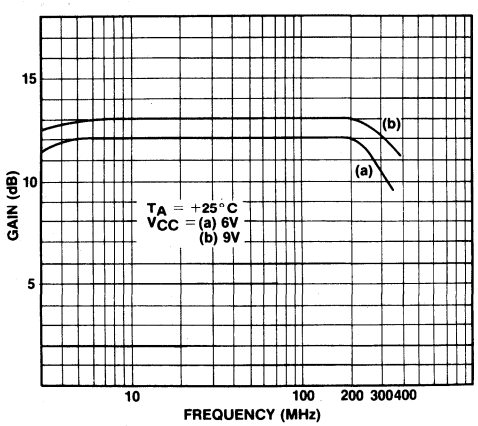


Fig.11 Frequency response of circuit shown in Fig.10 (typical)

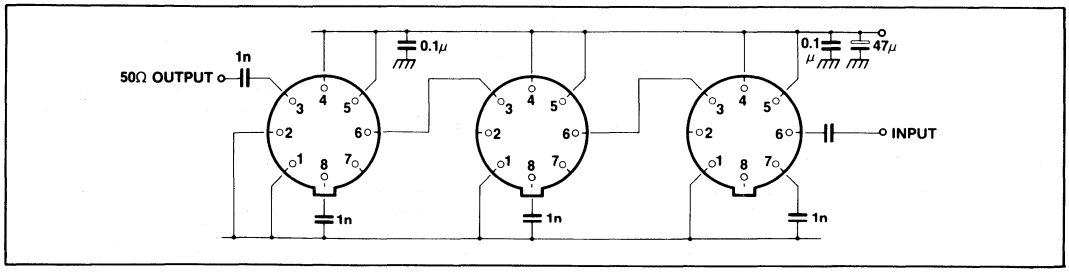


Fig.12 Three-stage directly-coupled high gain low noise amplifier

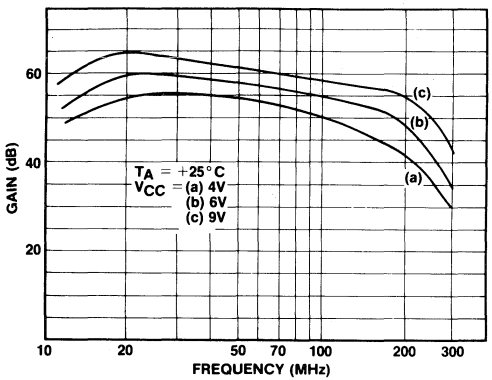


Fig.13 Frequency response of circuit shown in Fig.12 (typical)

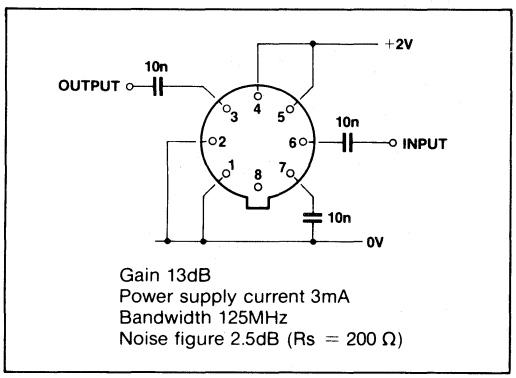


Fig.14 Low power consumption amplifier

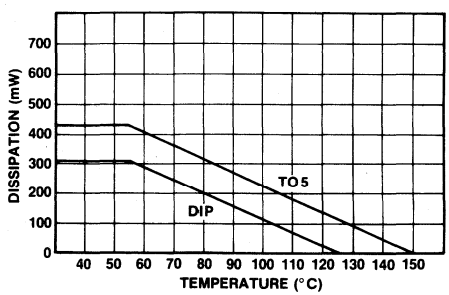


Fig.15 Ambient operating temperature v. degrees centigrade (typical)

SL952

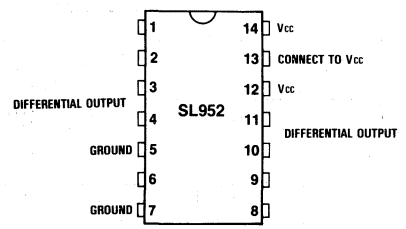
UHF LIMITING AMPLIFIER

The SL952 is a single chip limiting amplifier for use up to 1GHz. It features differential inputs and outputs and is suitable for use as a prescaler driver, limiting amplifier etc.

The device operates from a single 5V supply with a minimal number of external components and is encapsulated in either a 14 lead DIL package or a 16 lead chip carrier.

FEATURES

- Low Cost
- High Gain
- Minimal External Component Count
- Good Limiting Characteristics
- 1GHz Response
- 5V Supply



NOTE: Ground all other unused pins. **DP14**

Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Vcc	+10V
Ambient temperature	0°C to +65°C
Storage temperature	-55°C to +125°C

ORDERING INFORMATION

SL952 NA DP
SL952 NA DG
SL952 CB DG

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Vcc = +5V, T_{amb} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4.75	5.00	5.50	V	
Supply current		70	90	mA	
DC output level		3.2		V	
Output offset		100	600	mV	
Maximum differential output swing	600			mV p-p	950MHz
Differential voltage gain	30	35		dB	100MHz
Differential voltage gain	30	35		dB	500MHz
Differential voltage gain	15	26		dB	950MHz
Gain variation with supply		1		dB	Between 4.75V and 5.25V
Reverse isolation		30		dB	500MHz
1dB gain compression point		37		dBm	Input 10-900MHz
Input impedance		310Ω// 1.8pF			500MHz

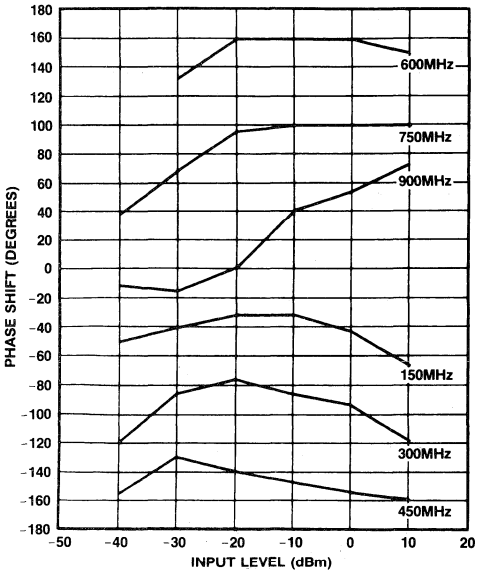


Fig.2 Phase shift/amplitude at various frequencies (input and output terminated at 50Ω

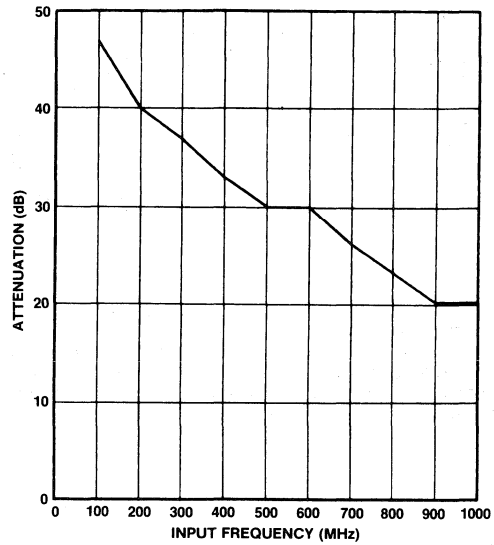


Fig.3 Input/output characteristic, 10-900MHz

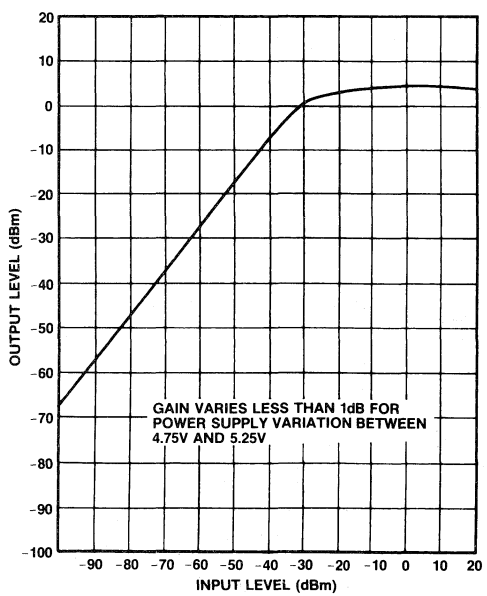


Fig.4 Reverse isolation v. input frequency

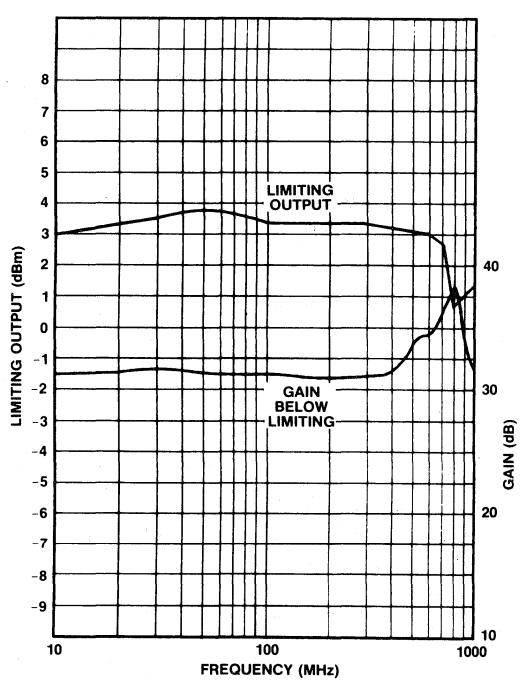


Fig.5 Limiting output v. frequency input -15dBm and gain below limiting v. frequency input -50dBm

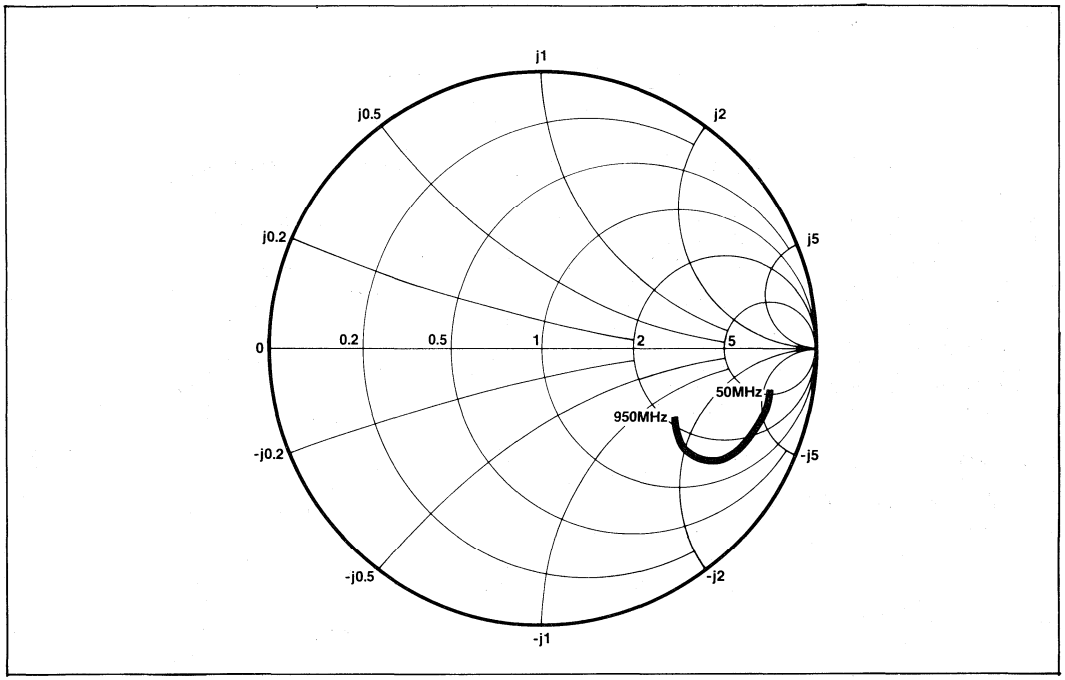


Fig.6 Input impedance (S_{11})

SL541

HIGH SLEW RATE OPERATIONAL AMPLIFIER

The SL541 is a monolithic amplifier designed for optimum pulse response and applications requiring high slew rate with fast settling time to high accuracy. The high open loop gain is stable with temperature, allowing the desired closed loop gain to be achieved using standard operational amplifier techniques. The device has been designed for optimum response at a gain of 20dB when no compensation is required. The SL541B has a guaranteed input offset voltage of ±5mV maximum and replaces the SL541C.

The SL541B is tested in two circuit applications (A and B).

FEATURES

- High Slew Rate: 175V/μs
- Fast Settling Time: 1% in 50ns
- Open Loop Gain: 70dB (SL541B)
- Wide Bandwidth: DC to 100MHz at 10dB Gain
- Very Low Thermal Drift: 0.02dB/°C Temperature Coefficient of Gain
- Guaranteed 5mV input offset maximum

APPLICATIONS

- Wideband IF Amplification
- Wideband Video Amplification
- Fast Settling Pulse Amplifiers
- High Speed Integrators
- D/A and A/D Conversion
- Fast Multiplier Preamps

ORDERING INFORMATION

SL541 B CM
SL541 B DG
SL541 BB DG

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V+ to V−)		24V
Input voltage (Inv. I/P to non inv. I/P)		±9V
Storage temperature		−55°C to +175°C
Chip operating temperature		+175°C
Thermal resistances		
Chip-to-ambient:	TO-5	220°C/W
	DIL	125°C/W
Chip-to-case:	TO-5	60°C/W
	DIL	40°C/W

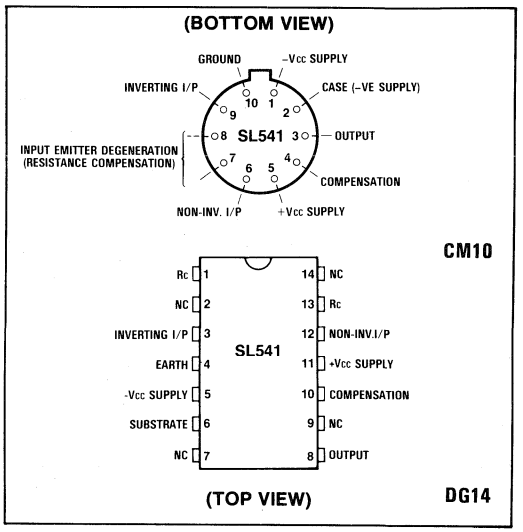


Fig. 1 Pin connections

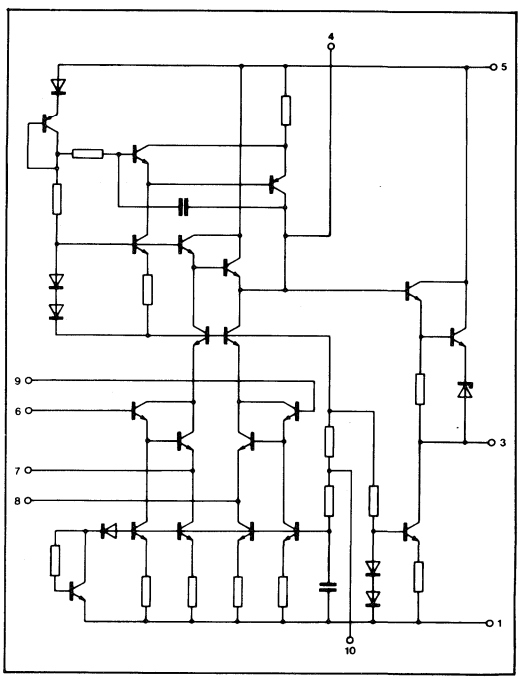


Fig. 2 SL541 circuit diagram (TO-5 pin nos.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25° C

Rc = 0Ω

Test circuits: see Fig.8

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Static nominal supply current	A,B		16	21	mA	
Input bias current	A,B		7	25	μA	
Input offset voltage	A,B			5	mV	
Dynamic open loop gain	A	45	54		dB	600Ω load
	B	60	71		dB	
Open loop temperature coefficient	A,B		-0.02		dB/° C	
Closed loop bandwidth (-3dB)	A,B		100		MHz	X10 gain
Slew rate (4V peak)	A,B	100	175		V/μs	X10 gain
Settling time to 1 %	A,B		50	100	ns	
Maximum output voltage						
(+ve)	A	5.5	5.7		V	
(-ve)	A		-1.9	-1.5	V	
(+ve)	B	2.5	3.0		V	
(-ve)	B		-3.0	-2.5	V	
Maximum output current	A,B	4	6.5		mA	
Maximum input voltage						
(+ve)	A			5	V	
(-ve)	A	-1			V	Non-inverting
(+ve)	B			3	V	modes
(-ve)	B	-3			V	
Supply line rejection						
(+ve)	A,B	54	66		dB	
(-ve)	A,B	46	54		dB	
Input offset current	A,B			9.85	μA	
Common mode rejection	A,B	60.7			dB	
Input offset voltage drift	A		25		μV/° C	

ELECTRICAL CHARACTERISTICS (Typical)

Test conditions (unless otherwise stated):

T_{amb} = -40° C to + 85° C

Rc = 0Ω, Test circuit B

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Static nominal supply current			16	25	mA	
Input bias current				35	μA	
Input offset voltage	(+ve)			8	mV	
	(-ve)	-8			mV	
Maximum output current		3.5	6.5		mA	
Maximum input voltage	(+ve)			3	V	Non-inverting modes
	(-ve)	-3			V	
Supply line rejection	(+ve)	50			dB	
	(-ve)	42			dB	
Maximum output voltage	(+ve)	2.3			V	
	(-ve)			-2.5	V	
Common mode rejection		55			dB	
Input offset current				16	μA	
Output voltage drift			15		μV/° C	
Input bias current drift			60		nA/° C	
Output current drift			40		nA/° C	

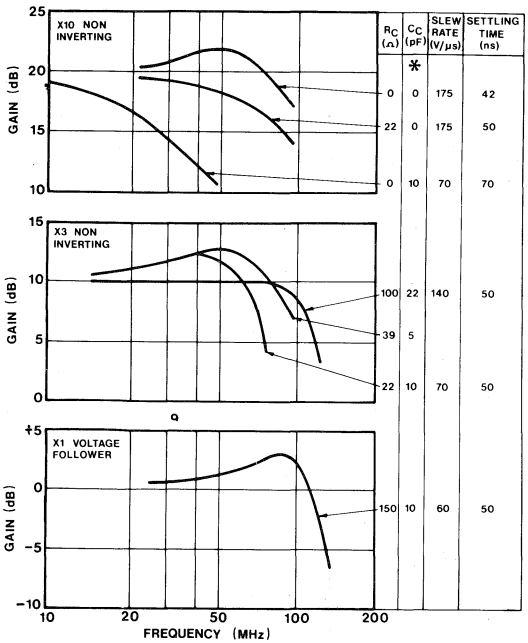


*Fig. 3 Performance graphs – gain v. frequency (load = 2kΩ/10pF) * See operating note 2*

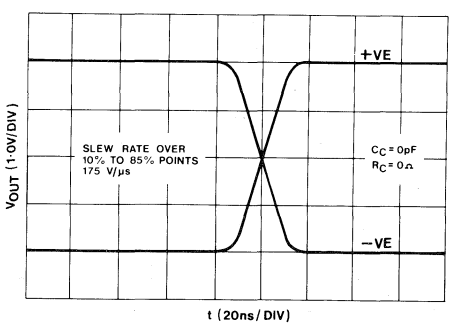


Fig.4 Slew rate - X10 non-inverting mode Input square wave 0.4V p/p

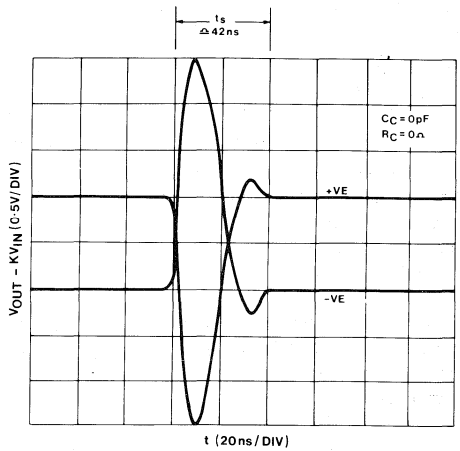


Fig.5 Settling time - X10 non-inverting mode

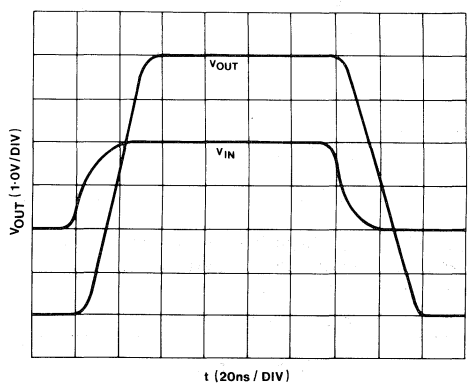


Fig.6 Output clipping levels - X10 non-inverting mode Input moderately overdriven, so that output goes into clipping both sides

OPERATING NOTES

The SL541 may be used as a normal, but non saturating operational amplifier, in any of the usual configurations (amplifiers, integrators etc.), provided that the following points are observed:

1. Positive supply line decoupling back to the output load earth should always be provided close to the device terminals.
2. Compensation capacitors should be connected between pins 4 and 5. These may have any value greater than that necessary for stability without causing side offsets.
3. The circuit is generally intended to be fed from a fairly low impedance (<1kΩ), as seen from pins 6 and 9 – 100Ω or less results in optimum speed.
4. The circuit is designed to withstand a certain degree of capacitive loading (up to 20pF) with virtually no effect. However, very high capacitive loads will cause loss of speed due to the extra compensation required and asymmetric output slew rates.
5. Pin 10 does not need to be connected to zero volts except where the clipping levels need to be defined accurately w.r.t. zero. If disconnected, an extra ±0.5 volt uncertainty in the clipping levels results, but the separation remains. However, the supply line rejection is improved if pin 10 can be left open-circuit (circuit B only).

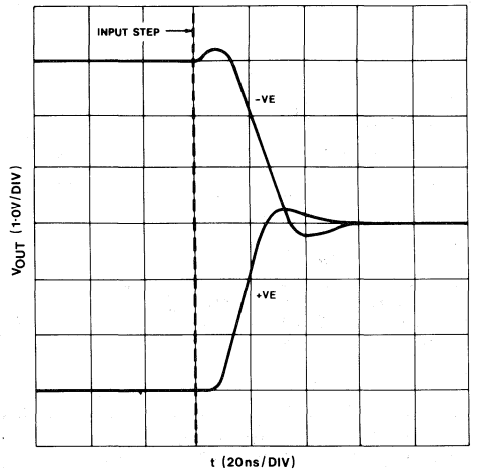


Fig.7 Output clippings levels - X10 non-inverting mode. Output goes from clipping to zero volts. V_{in} = 3V peak step, offset +ve or -ve.

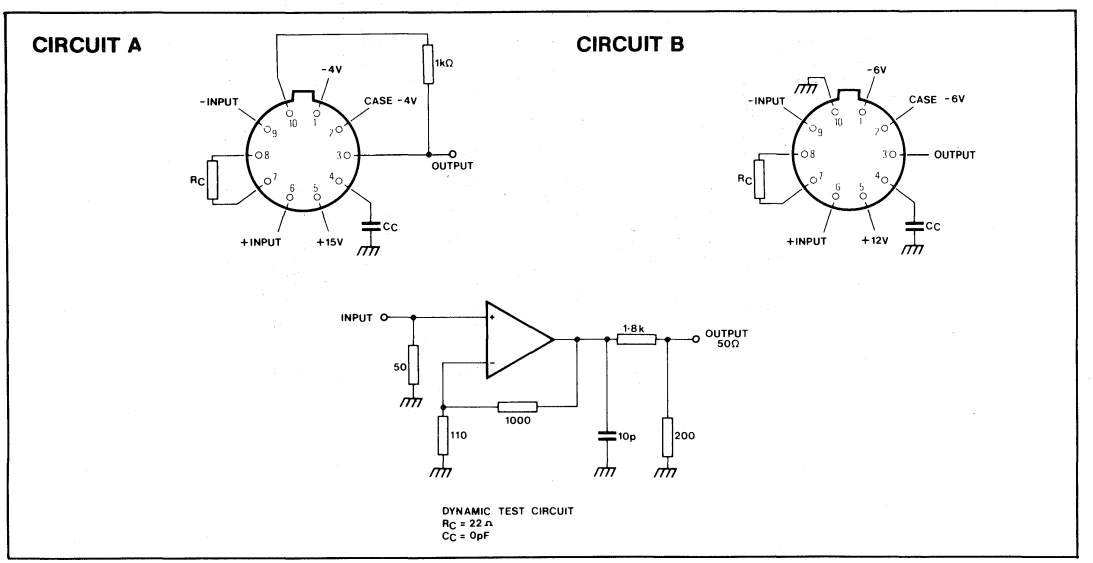


Fig. 8 Test circuits

TEST CONDITIONS AND DEFINITIONS

Both slew rate and settling time are measures of an amplifier's speed of response to an input. Slew rate is an inherent characteristic of the amplifier and is generally less subject to misinterpretation than is settling time, which is often more dependent upon the test circuit than the amplifier's ability to perform.

Slew rate defines the maximum rate of change of output voltage for a large step input change and is related to the full power frequency response (fp) by the relationship.

$$S = 2\pi f_p E_o$$

where E_o is the peak output voltage

Settling time is defined as the time elapsed from the application of a fast input step to the time when the amplifier output has entered and remained within a specified error band that is symmetrical about the final value. Settling time, therefore, is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vincinity of some value of output voltage, plus a period to recover from overload and settle within the given error band.

The SL541 is tested for slew rate in a X10 gain configuration.

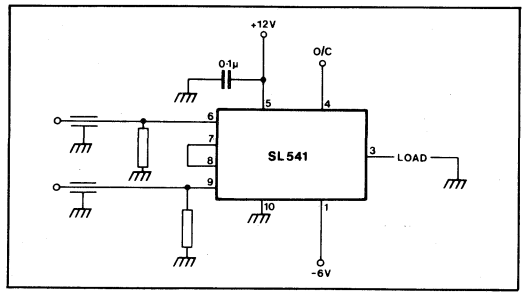


Fig. 9 Non-saturating sense amplifier (30V/μs for 5mV)
Note: the output may be caught at a pre-determined level. (TO-5 pin nos.)

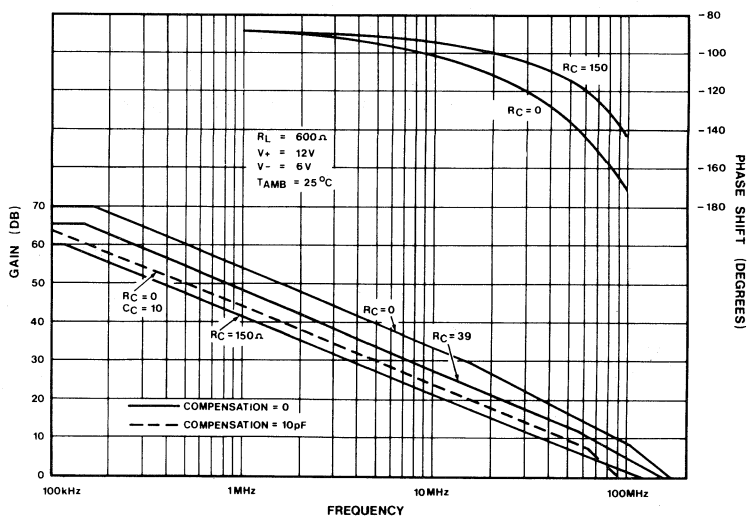


Fig.10 SL541B open loop gain and phase shift v. frequency

TAB1043

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER

The TAB1043 is an advanced bipolar integrated circuit containing four separate operational amplifiers. The amplifiers are programmed by current into the appropriate bias pin. Pin 8 (Bias 2) programmes amplifiers B, C and D and pin 16 (Bias 1) programmes amplifier A.

For example, with a suitable choice of bias current, the TAB1043 will perform in a manner similar to four amplifiers of the 741 type, but with improved frequency response and input characteristics.

The TAB1043 is especially suitable for use in active filter applications.

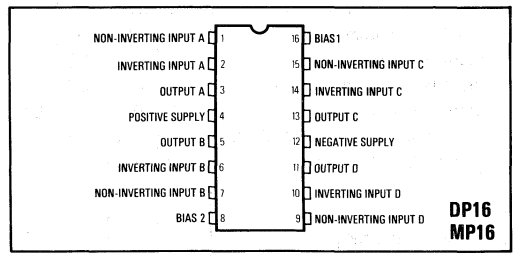


Fig. 1 Pin connections

FEATURES

- Four Independent Op. Amps. in One Package
- Internally Compensated
- Wide Range of Supply Voltages from ±1.5V to ±12V
- No Latch-Up
- Programmable Over 100:1 Current Range
- Gain Bandwidth Product Up to 4MHz
- Built-In Short Circuit Protection
- Very Low Noise

ORDERING INFORMATION

TAB1043 NA DP

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±12V
- Supply Current ±40uA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

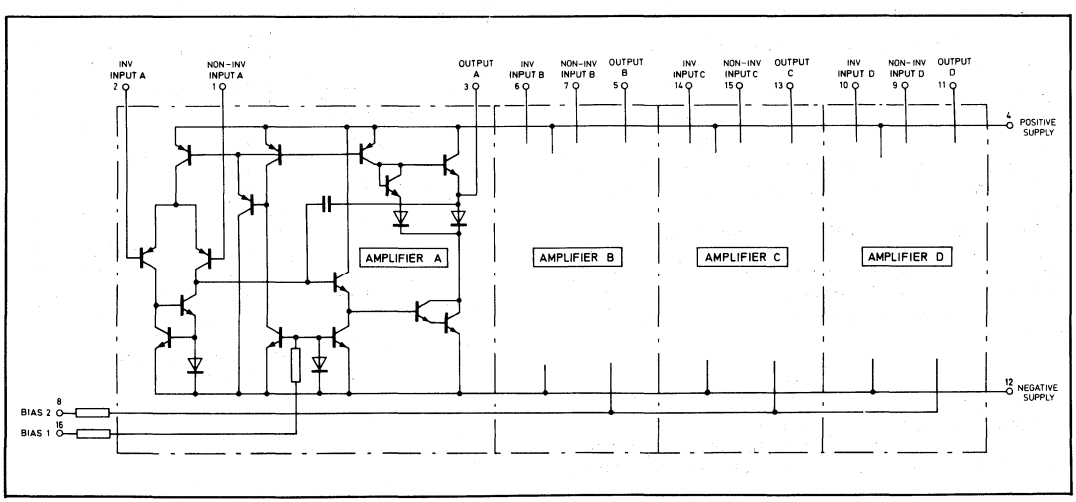


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
Operating mode A:Supply volts ±12V Bias set current 75μA
Operating mode B:Supply volts ±12V Bias set current 1μA
Operating mode C:Supply volts ±1.5V Bias set current 1μA

Characteristics	Operating Mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	Rs 10kΩ
Input offset current		20	200		5	50		5	50	nA	
Input bias current		250	500		30	100		30	100	nA	
Input resistance	0.1	0.6		0.5	2		0.5	2		MΩ	
Supply current (each amplifier)	1000	1600	2200		42		20	40	60	μA	
Large signal volt gain	74	95		66	90		66	90		dB	RL = 4kΩ(A) RL = 100kΩ(B) RL = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	Rs 10kΩ
Common mode rejection ratio	70	110			82			82		dB	
Output voltage swing	9	10.8		9	10.8		0.2	0.3		±V	RL = 4kΩ(A) RL = 100kΩ(B) RL = 4kΩ(C)
Supply voltage rejection ratio	75	96		75	86		75	86		dB	Rs 10kΩ
Gain bandwidth product		3.5			50			50		kHz MHz	Gain = 20dB
Slew rate		1.5			0.02			0.02		V/μs	Gain = 20dB
Input noise voltage		15			45			45		nV/√Hz	f_o = 1kHz
Input noise current		1.6			1.6			1.0		pA/√Hz	f_o = 1kHz

OPERATING NOTES

Bias set current

The amplifiers are programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each amplifier)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02 V/μs (I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{Vs - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

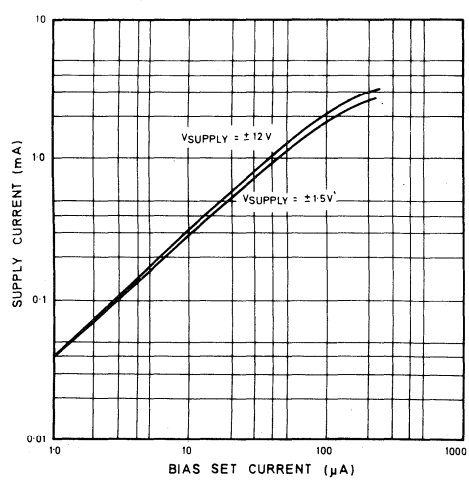


Fig.3 Supply current (each amplifier) v. bias set current

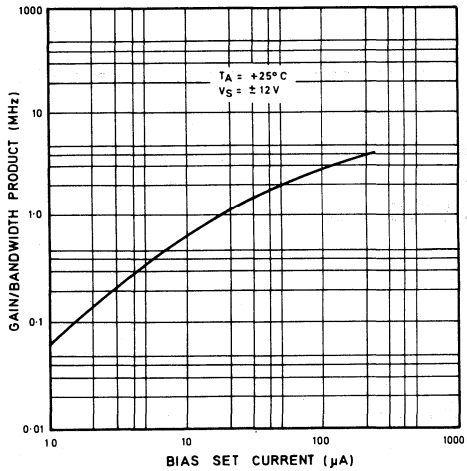


Fig. 4 Gain bandwidth product v. I_{SET}

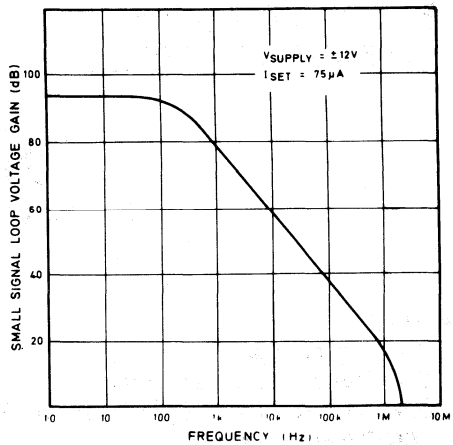


Fig. 5 Typical frequency response

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA each pin
Storage	-55° C to +125° C
Power dissipation	800mW at 25° C
	Derate at 7mW/° C above 25° C
Operating temperature range	-40° C to +85° C

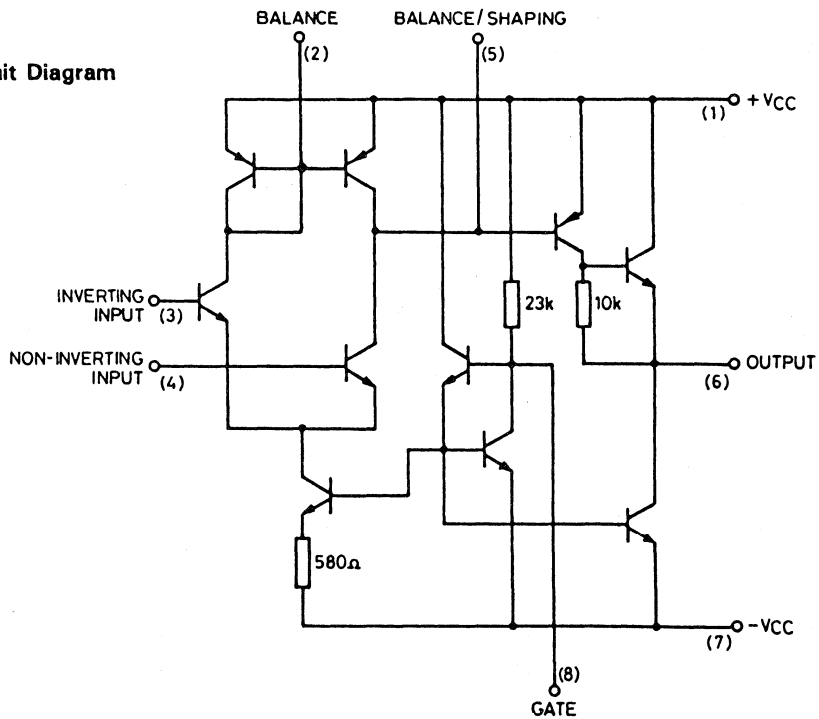
ZN424P

GATED LINEAR AMPLIFIER

FEATURES

- 86dB typical gain
- Very low open loop distortion
- Low noise ($e_n^2 = 4 \times 10^{-17}$ V²/Hz; 100Hz to 20kHz)
- 200kΩ input resistance
- 20kHz open loop bandwidth (−3dB)
- 0.1μs closed loop rise time
- Class A output stage
- 100V/μs slew rate (rising edge)
- Maximum output swing ±11V, ±17V at $V_{CC} = \pm 18$V
- Operation at 5V, TTL compatible
- Logic gate current drive capability
- Input-output isolation gating facility

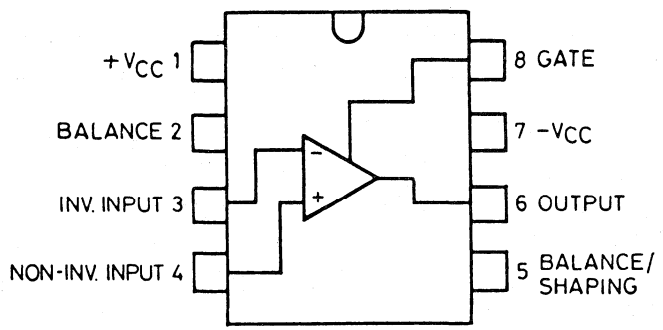
Circuit Diagram



GENERAL DESCRIPTION

The ZN424P is a versatile linear amplifier designed to satisfy the growing requirement for high quality signal processing. As a voltage amplifier the very low distortion and low noise performance makes the device ideally suited for audio applications. The gating facility, coupled with the ability to operate from a TTL supply, gives the device broad appeal in the instrumentation, computing and allied fields. The device is readily stabilised using an external capacitor, or capacitor/resistor combination.

PIN CONFIGURATIONS



ZN424P
(8 lead Moulded Dual in-line)
Viewed from top

DP8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	250mW
Differential Input Voltage	5V
Storage Temperature Range	−65 to +125°C

RECOMMENDED RATINGS

Supply Voltage Range	±2 to ±18V
Operating Temperature Range	0 to +70°C

ELECTRICAL CHARACTERISTICS

($V_S = \pm 12V$, Load = 20kΩ, $T_{amb} = 25°C$ unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units
Input offset voltage		2	6	mV
Input current		0.5	1.2	μA
Input offset current		0.1	0.5	μA
Input offset voltage drift		5		μV/°C
Input current drift		2.0		nA/°C
Input offset current drift		0.4		nA/°C
Input resistance		200		kΩ
Output resistance		4		kΩ
Voltage gain	10,000	20,000		
Mutual conductance		5		A/V
Common mode range	±10	±11		V
Output voltage swing	±10	±11		V
Maximum negative output current (load = 1kΩ)		3.0		mA
Supply current		5.5	7.0	mA
Open loop bandwidth (−3dB)		20		kHz
Unity gain bandwidth (−3dB) (See Note 2)		1		MHz
Common mode rejection ratio	70	100		dB
Supply rejection ratio	80	85		dB
Unity gain rise time(slew rate 1.5V/μs, see Note 2)		0.35		μs
Unity gain overshoot (see Note 2)		10		%
Output leakage current (gated off)		5	30	nA
Voltage gain $V_S = \pm 2.5V$, 3.3kΩ between gating input and $+V_{CC}$, load = 10kΩ	5,000	12,000		
Slew rising edge		100		V/μs
Slew rate falling edge		12		V/μs
Open loop distortion (2V ptp swing)		<1.5		%T.H.D.
Open loop distortion (10V ptp swing)		6		%T.H.D.

OPERATING NOTES

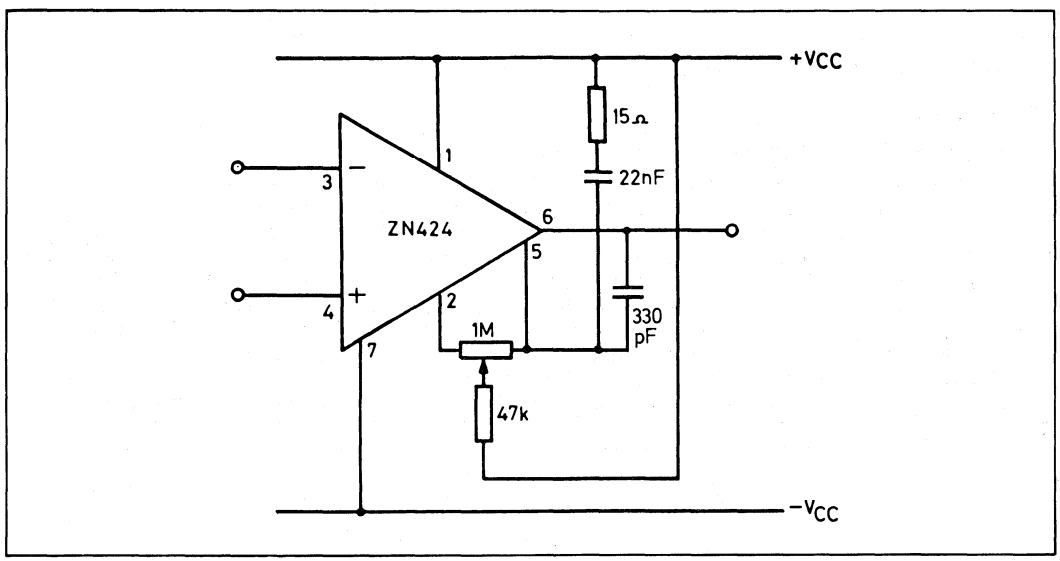
1. When operating with low supply voltages the output bias current may be maintained at about 3mA by connecting an external resistor between the gating input and $+V_{CC}$. Under these conditions the output current is given approximately by:

$$I_C = \frac{(V_{CC} - 1.4) \times 3}{R}$$

R is the parallel combination of the external and internal (23kΩ) resistors.

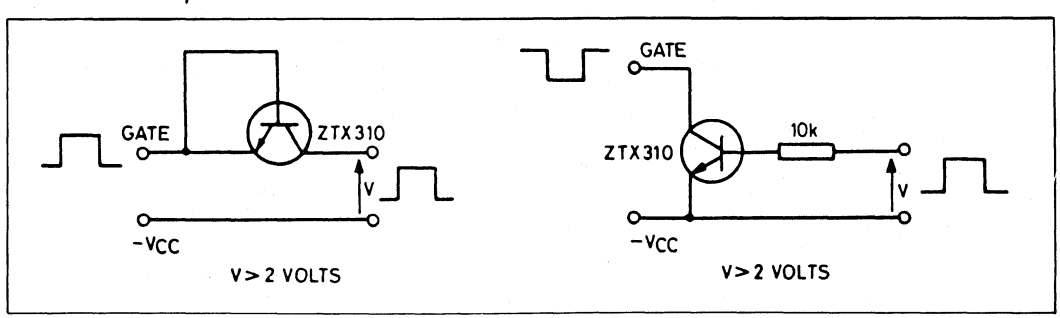
2. Unity frequency stability is achieved by connecting a 22nF capacitor and a 15 ohm resistor in series between 'shaping' and +Vcc, and 330pF between 'shaping' and output.

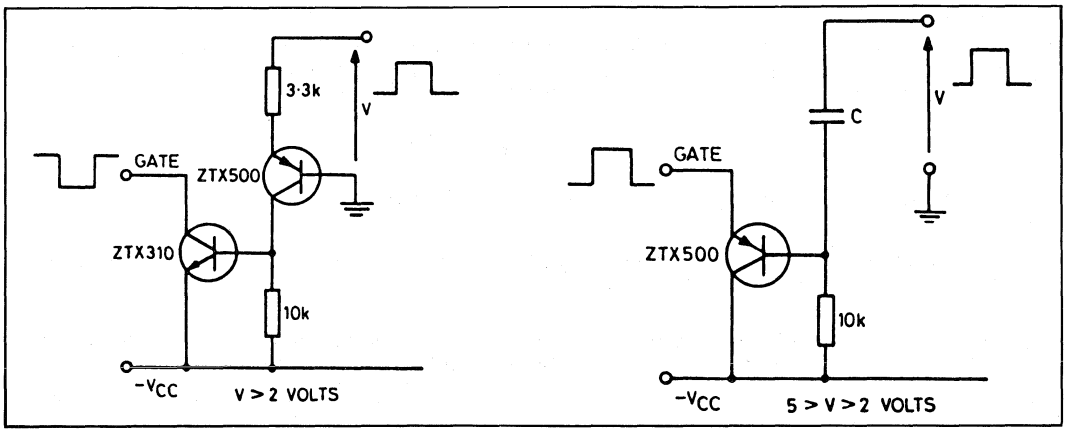
3. Input offset voltage is nullified by connecting a 1MΩ potentiometer between 'balance' and 'balance/shaping' with the wiper connected through a 47kΩ resistor to $+V_{CC}$.



Offset and Frequency Compensation Circuit

4. The ZN424P is gated 'off' by shunting the current source bias current to the negative rail. Four methods of gating the ZN424P are illustrated below, two of which require a drive voltage with respect to the negative rail (e.g. from another ZN424P or from logic, when using a single supply), and the other two allowing the drive pulse to be with respect to earth or another convenient point.



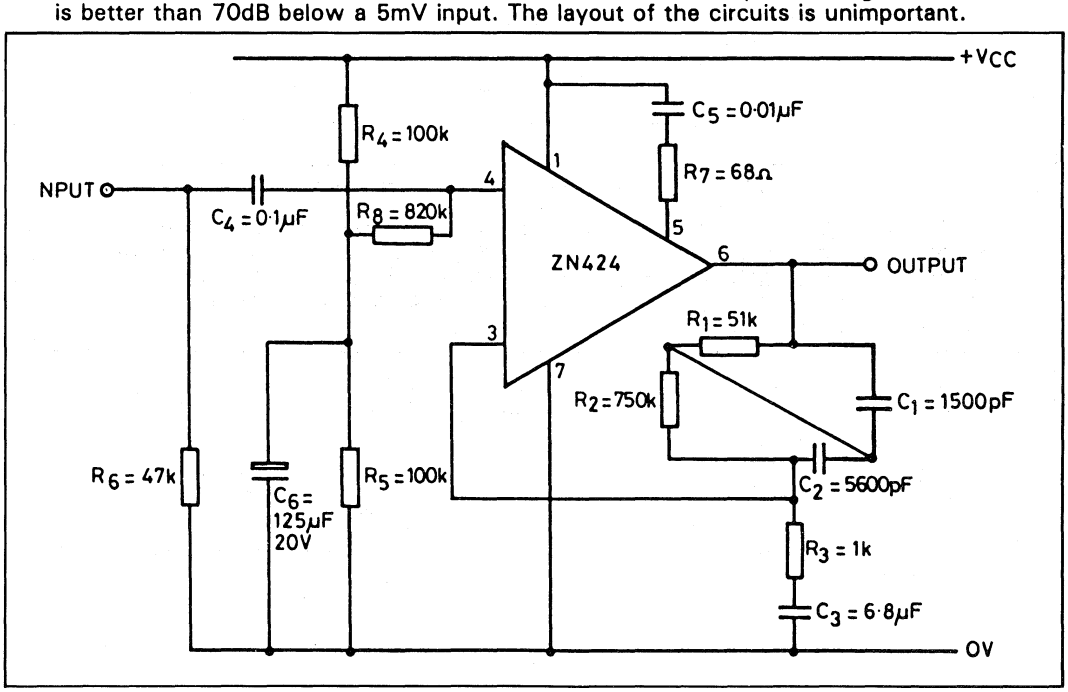


5. When gated off, the input-output coupling is representable by a 1pF capacitor.

APPLICATIONS

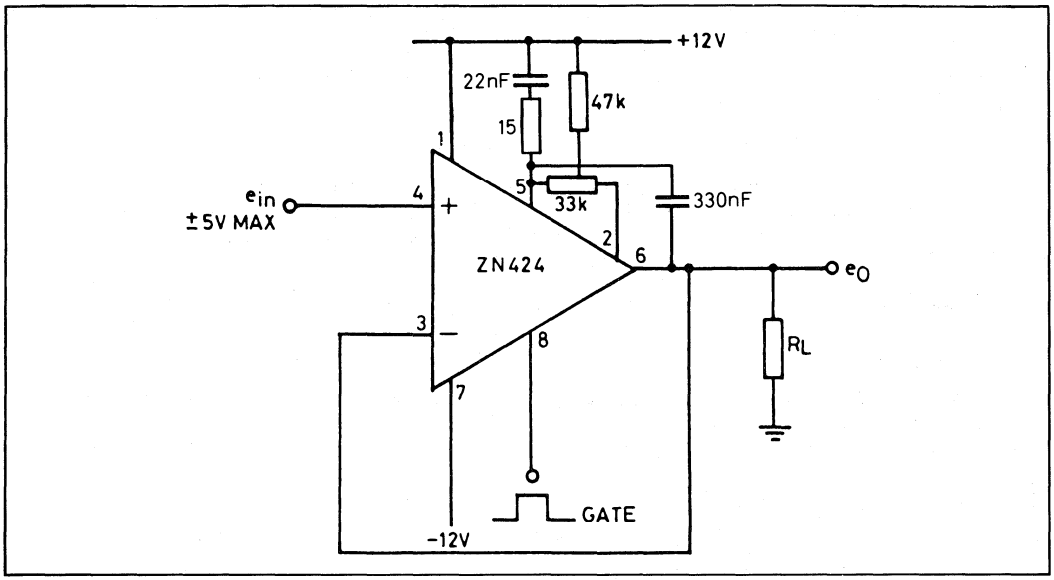
1. Magnetic Cartridge (R.I.A.A.) Preamplifier:

The open loop gain of the ZN424P is 20,000 (86dB) and the open loop distortion is typically, 1.5% corresponding to a 2 volt peak output swing (this is the maximum output ever likely to be encountered from a magnetic cartridge). To feed most power amplifiers a voltage gain, at 1kHz, of 50 (34dB) is necessary between cartridge and amplifier. Thus by applying 52dB of feedback (86dB to 34dB) the distortion figure at 1kHz becomes 0.004%. If more gain is required R_3 may be made smaller but C_3 must be increased proportionaly to avoid loss of bias. C_1, C_2, R_1, R_2 provide R.I.A.A. equlisation and, in addition, C_3 and R_3 provide an effective rumble filter. C_5 and R_7 provide stability for all supply voltages. Assuming a 30 volts supply the overload factor of the circuit is ≃40dB referred to a 5mV input. The signal to noise ratio is better than 70dB below a 5mV input. The layout of the circuits is unimportant.



Magnetic Cartridge Preamplifier Circuit

2(a) X1 Non-Inverting Amplifier:

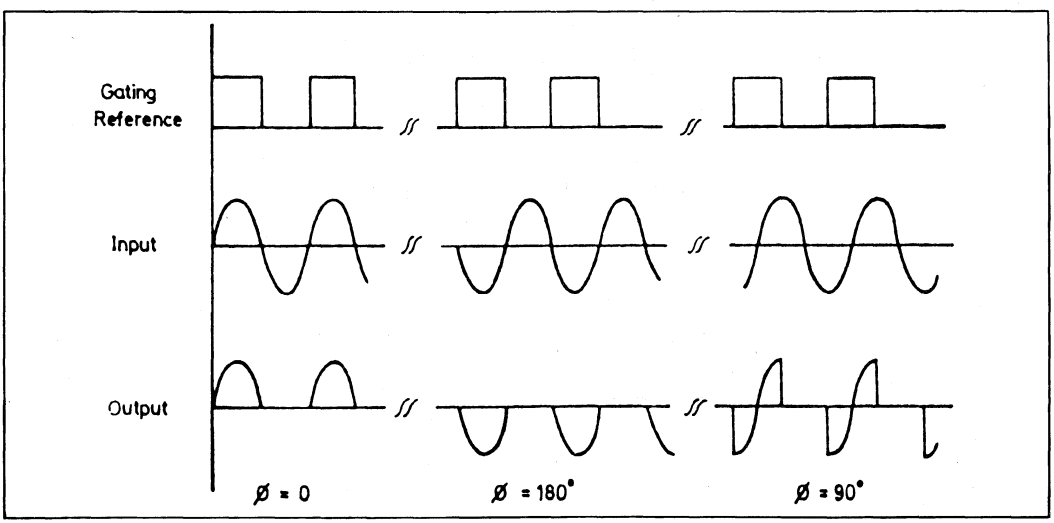


The circuit diagram is shown above. Feedback is applied in the normal way. When the amplifier is gated 'off' the input and output become open circuited as long as the maximum differential input voltage is not exceeded. This limits the input voltage range to ± 5V. This may be effectively increased by attenuating the input suitably and defining the gain of the amplifier to give an overall gain of unity. In order to obtain an overall gain of unity an attenuator comprising of $R_F = 47k\Omega$ and $R_S = 10k\Omega$ is required.

This method has the disadvantages of requiring four accurate resistors, giving a higher output offset voltage (unless an offset control is used) and lower input resistance (57kΩ). However, the settling time is reduced (see Table 1) since lower values of shaping capacitor can be used.

By applying a square wave to the gating point, an output may be obtained which is an amplified square wave modulated version of the input.

2(b) Rectification/Demodulation (no transformers ncessary):



The previous circuit may be used as a half-wave sensitive detector by applying a square wave reference voltage to the gating point and a phase related signal to the input. Typical waveforms are illustrated below for phase differences (ϕ) of 0, 90 and 180 degrees.

The mean d.c. output level is proportional to R cosϕ, where R is the input amplitude. For a half-wave detector with a gain of A:

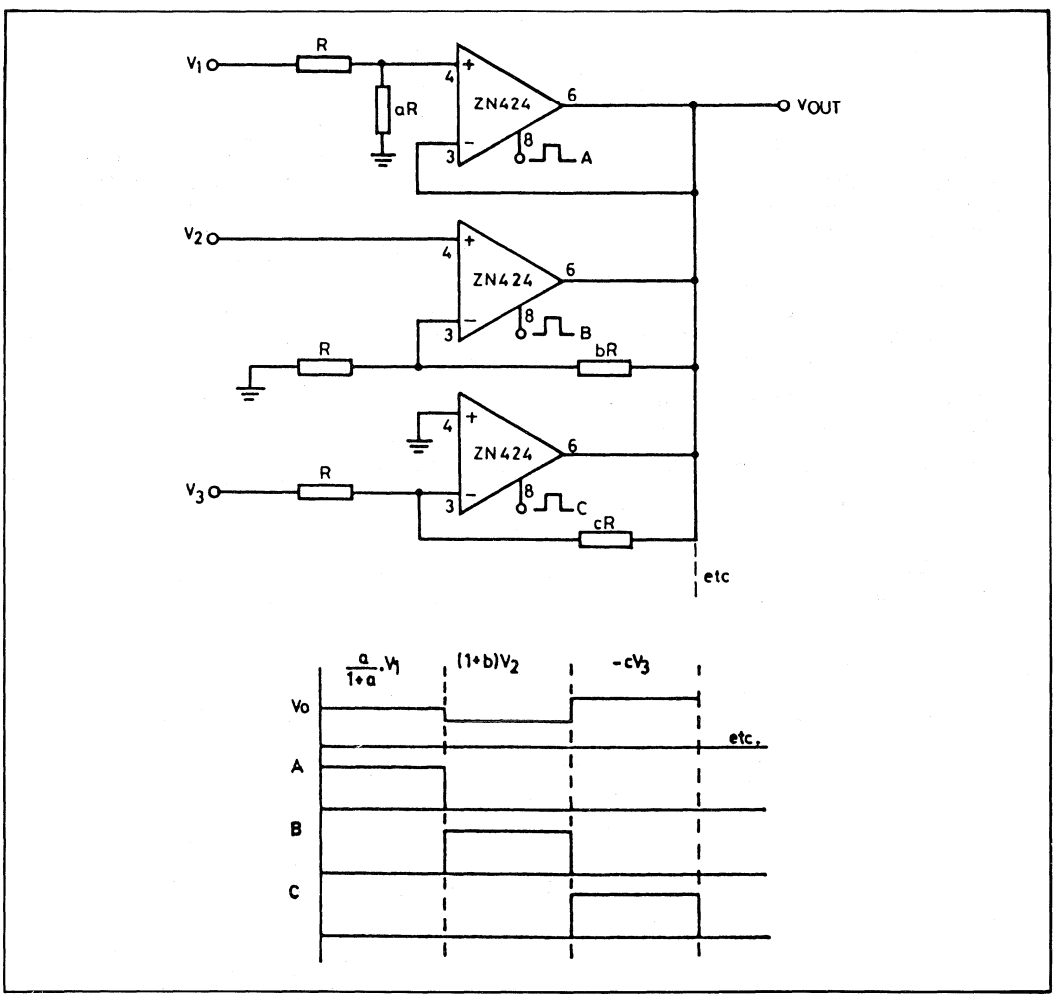
$$\overline{e_O} = \frac{AR}{\pi} \cos\phi$$

Using two phase sensitive detectors driven from square wave reference voltages 90 degrees out of phase, outputs proportional to Rcosϕ and Rsinϕ may be obtained. If these voltages are applied to the X and Y plates of a cathode ray tube the spot will describe the polar plot (R,ϕ). Nyquist plots may thus be obtained directly.

The square wave reference voltages may be generated using a ring counter.

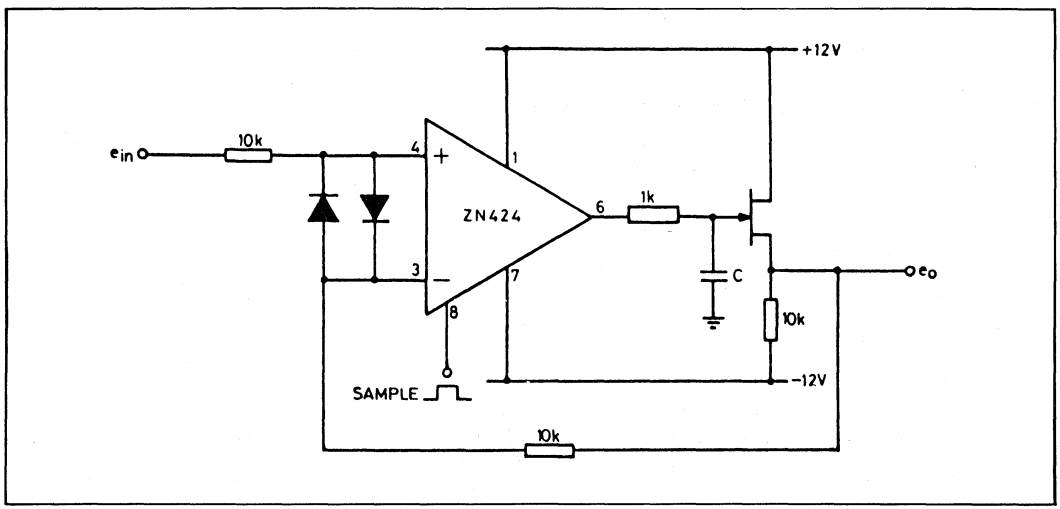
3. Multiplexing:

A ring counter is used to provide a gating pulse to enable the ZN424P to give a multiplexed output as shown below.



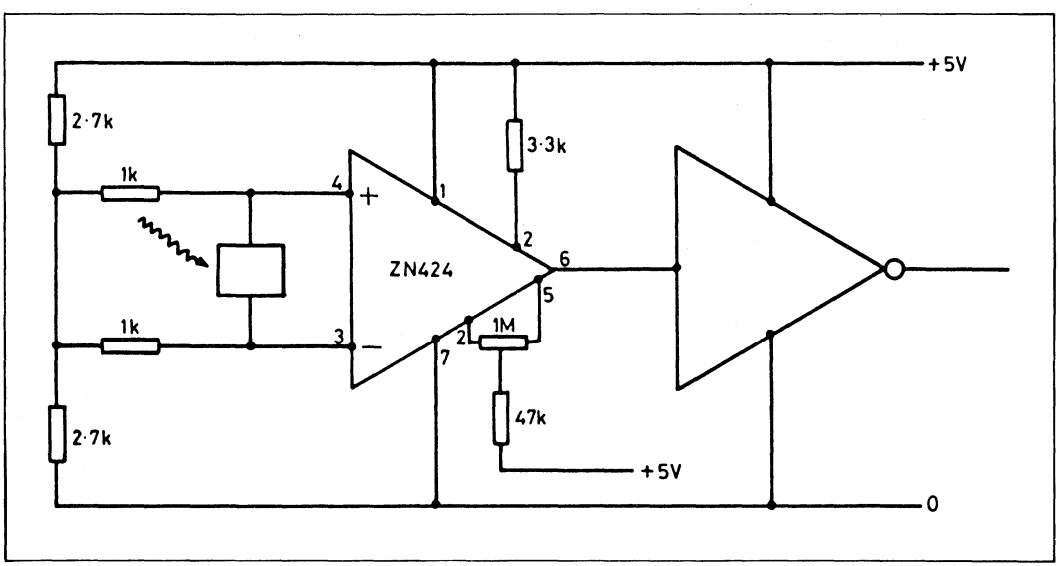
4. Sample and Hold Circuits:

A typical circuit is shown below. The output voltage, e_O, is determined by the choice of feedback resistor when the ZN424P is gated 'on'. When gated 'off', e_O is held for a time which is dependent on 'C', the leakage of the FET and the ZN424P. The value of the capacitor also determines the sampling time necessary. Integrator/Reset circuits can readily be derived from this type of circuit.



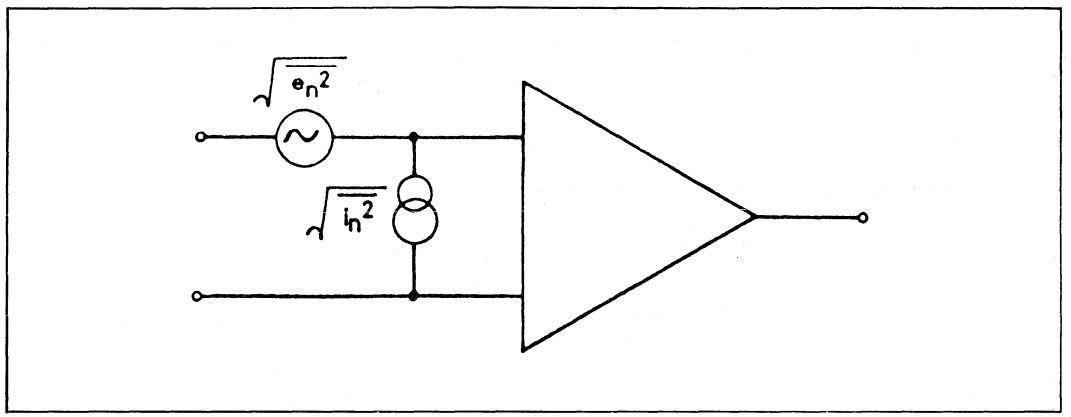
5. Photocell Trigger Circuit Driving TTL Gate(s):

A typical circuit is shown below. The input is biased, so the output is low, when the photocell is irradiated. With no output from the photocell the output is high. The photocell used below gave an output of 60mV, 30μA when irradiated. In this type of circuit the gating facility can be used to switch various combinations of photoelectic, encoder/decoder circuitry.



NOISE

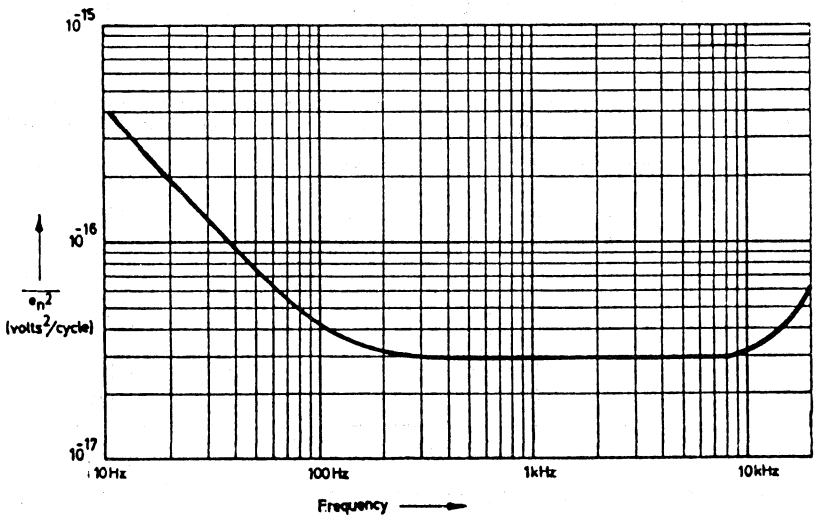
An amplifier always generates noise. At low frequencies flicker noise predominates and increases inversely with the frequency (though presumably not indefinitely). At a sufficiently high frequency this source of noise becomes insignificant compared with shot noise. This is white noise, i.e., has a constant energy/cycle.

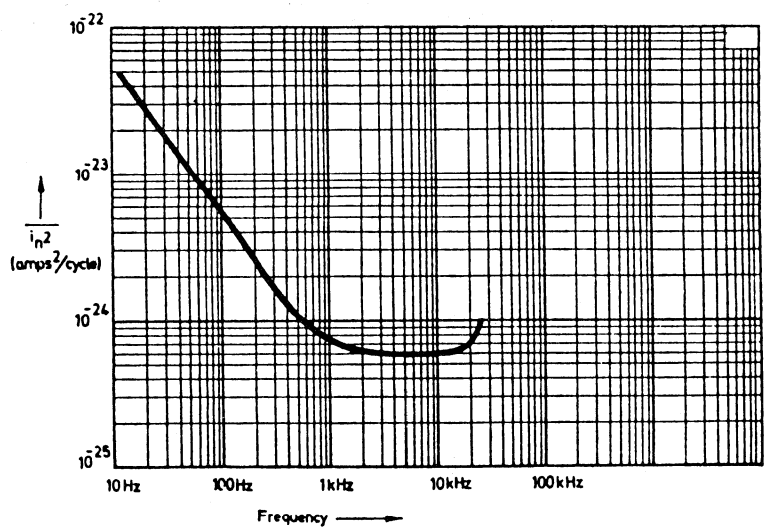


Any amplifier may be represented by an ideal amplifier with equivalent noise voltage and current generators at the input as shown above. The mean square noise voltage is shown as $\overline{e_n^2}$ volts^2/cycle and the mean square noise current as $\overline{i_n^2}$ amps^2/cycle. The noise voltage may be measured by short-circuiting the inputs so that no noise current flows into the amplifier. When the input terminals are open-circuited all the noise current flows into the amplifier and the noise voltage generator is open-circuited. The noise that appears at the output of the amplifier will obviously depend upon the shape of the frequency response. If the frequency response is measured the noise measured at the output may be referred back to the input. This is shown below where $\overline{e_n^2}$ and $\overline{i_n^2}$ are plotted against frequency. In an actual case, a source resistance R_S will be connected across the input terminals.

This resistance will itself generate white noise known as Johnson noise of magnitude $\overline{e_r^2} = 4kTR_S$ volts^2/cycle, where k is the Boltzmann constant and T is the absolute temperature. The noise current flowing in this resistance will also produce a mean square noise voltage of $\overline{i_n^2}\ R_S^2$volts^2/cycle.

TYPICAL CHARACTERISTICS





Graph 1. $\overline{e_n^2}$ and $\overline{i_n^2}$ against frequency for ZN424P

Stabilising the ZN424P in Various Gain Configurations

The ZN424P is designed such that any resistive feedback circuit can be stabilised with less than 50 per cent overshoot using $C_1 = 0.1\mu F$. For better than 10 per cent overshoot, the values given in the following table are suitable.

TABLE 1

Closed loop gain	R_F (kΩ)	C_F (pF)	R_1 (Ω)	C_1 (nF)	C_2 (pF)	Rise Time (μs)	Slew Rate (V/μs)
⩾ 250	10	-	-	-	-	0.35	45
100	10	10	68	4.7	-	0.65	12
50	10	10	68	4.7	3.3	0.55	10
20	10	10	68	4.7	7.5	0.4	8
10	10	10	68	4.7	15	0.35	5
5	10	10	68	4.7	33	0.3	3
2	10	10	68	4.7	68	0.22	1.7
1	0	-	15	22	330	0.33	1.5

The rise times and slew rates are given as a guide when the supply current is maintained at about 5mA (see Operating Note 1).

R_1 and C_1 are connected in series between pins 5 and 1; C_2 is connected between pins 5 and 6.

For other values of R_F it may be necessary to change C_F for optimum response.

ZN402 Gated Op Amp (Obsolete)

The ZN402 is electrically similar to the ZN424P and the devices are interchangeable. However, because testing procedures are more rigorous for the ZN424P, its performance is better than that of the ZN402; the ZN424P is therefore recommended for all new designs.

SL561

ULTRA LOW NOISE PREAMPLIFIERS

This integrated circuit is a high gain, low noise preamplifier designed for use in audio and video systems at frequencies up to 6MHz. Operation at low frequencies is eased by the small size of the external components and the low 1/f noise. Noise performance is optimised for source impedances between 20Ω and 1kΩ making the device suitable for use with a number of transducers including photo-conductive IR detectors, magnetic tape heads and dynamic microphones.

The SL561B is only available in the TO-5 package.

The SL561C is only available in the Plastic package.

FEATURES

- High Gain 60dB
- Low noise 0.8nV/√Hz (Rs = 50Ω)
- Bandwidth 6MHz
- Low Power Consumption 10mW (V_{CC} = 5V)

APPLICATIONS

- Audio Preamplifiers (low noise from low impedance source)
- Video Preamplifier
- Preamplifier for use in Low Cost Infra-Red Systems

ORDERING INFORMATION

SL561 AC CM
SL561 B CM
SL561 BB CM
SL561 C DP

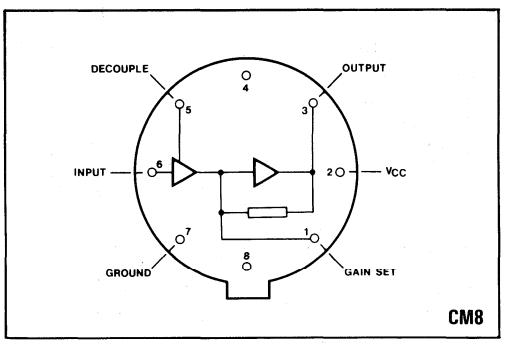


Fig.1 Pin connections (viewed from above) SL561B

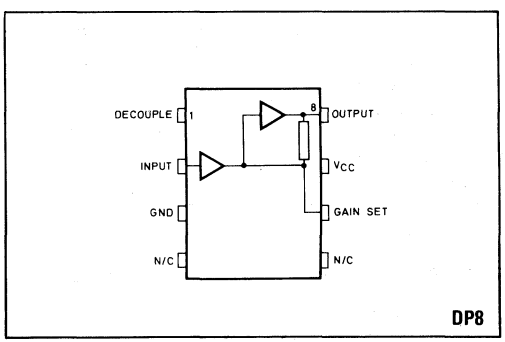


Fig.2 Pin connections (viewed from above) SL561C

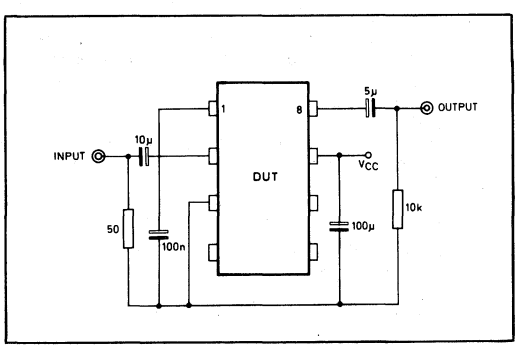


Fig.3 Test circuit

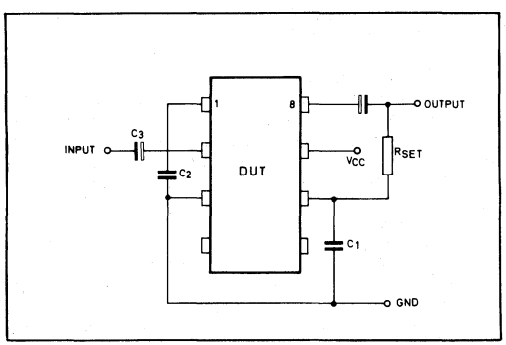


Fig.4 Typical application

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{CC}	5V
Source impedance	50Ω
Load impedance	10kΩ
T_{amb}	25°C

SL561B

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 1 O/C
Equivalent input noise voltage		0.8	1.2	nV/√Hz	100Hz to 6MHz
Output voltage	2	3		V p-p	See note
Supply current		2.0	3.0	mA	
Output resistance		50		Ω	
Input resistance		3		kΩ	
Input capacitance		15		pF	
Upper cut-off frequency	5	6.5		MHz	V_{out} = 10mV p-p
		6.2		MHz	V_{out} = 1.5V p-p

SL561C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 6 O/C
Equivalent input noise voltage		0.8		nV/√Hz	100Hz to 6MHz
Input resistance		3		kΩ	
Input capacitance		15		pF	
Output impedance		50		Ω	
Output voltage	2	3		V p-p	See note
Supply current		2	3	mA	
Bandwidth		6		MHz	

OPERATING NOTES (Pin numbers refer to DIL package)

Upper cut-off Frequency

The bandwidth of the amplifier can be reduced from 6MHz to any desired value by a capacitor from pin 6 to ground. This is shown in Fig.5. No degradation in noise or output swing occurs when this capacitor is used. The high frequency roll off is approximately 6dB/octave.

Low frequency response

The capacitors C_2 and C_3 (Fig.4) determine the lower cut-off frequency. C_2 decouples an internal feedback loop and if its value is close to that of C_3 an increase in gain at low frequencies can occur. For a flat response either make C_2 less than 0.05 C_3 or make C_2 greater than 5 C_3.

Gain set facility

Provision is made to adjust the gain by means of a resistor between pin 6 and the output. Gains as low as 10dB can be selected. This resistor increases the feedback around the output stage and stability problems can result if the bandwidth of the amplifier is not reduced as indicated in Note 1. Fig.6 shows recommended values of C_1 for each gain range. Since the input stage is a common emitter stage without emitter degeneration (for best noise) at values of gain less than 40dB this input stage, rather than the output stage, determines the maximum output voltage swing. For a distortion of less than 10% the input voltage should be restricted to less than 5mV (see Fig.9).

Driving low impedance loads

The quiescent current of the output emitter follower is 0.5mA. If larger voltage swings are required into low impedance loads this current can be increased by a resistor from pin 8 to ground. To avoid exceeding the ratings of the output transistor the resistor should not be less than 200Ω.

Noise performance

The equivalent input voltage for the amplifier is shown in Fig.7 From this the input noise voltage and current generators can be derived. They are:

$$e_n = 0.8nV/\sqrt{Hz}$$
$$i_n = 2.0pA/\sqrt{Hz}$$

Flicker or 1/f noise is not normally a problem, the knee frequency being typically below 100Hz.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	10V
Storage temperature range	-55°C to +125°C
Operating temperature range DIL	-55°C to +100°C
Operating temperature range TO5	-55°C to +125°C

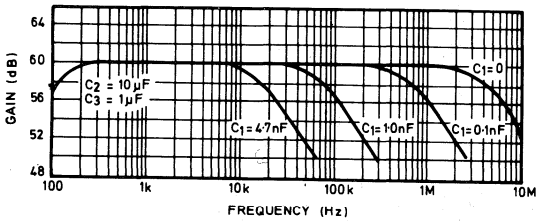


Fig.5 Gain v. frequency

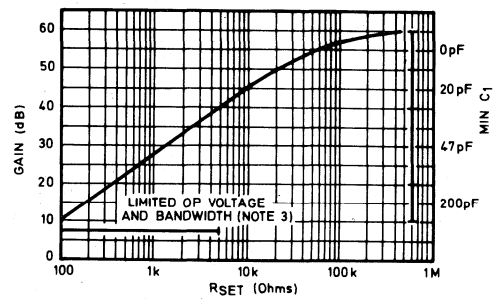


Fig.6 Gain v. R_{set}

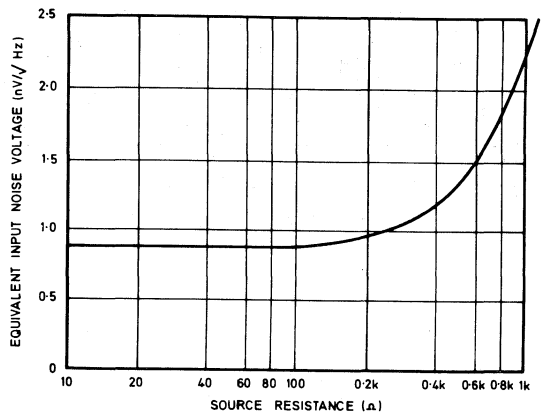


Fig.7 Noise v. source impedance

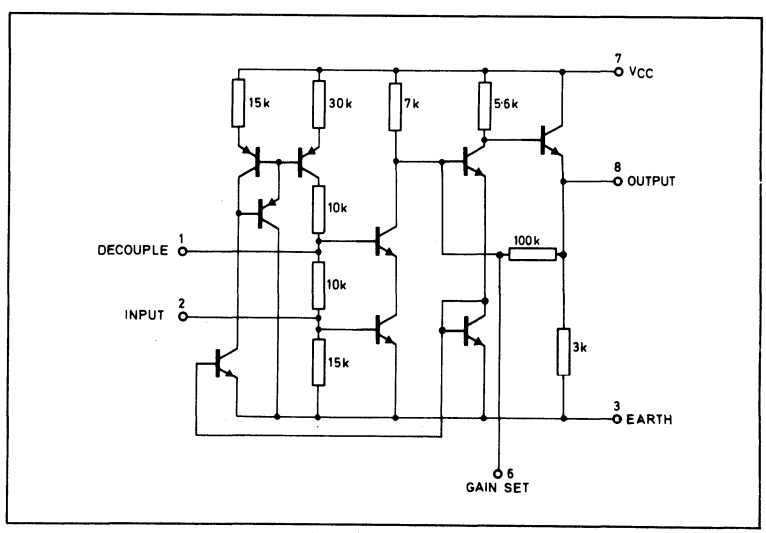


Fig.8 Circuit diagram

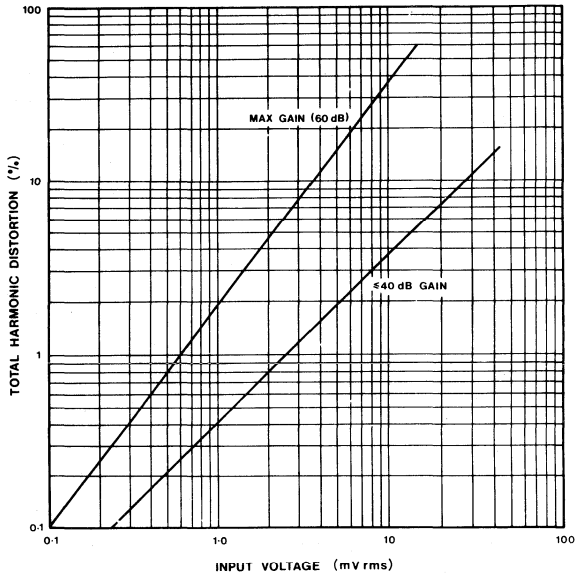


Fig.9 Harmonic distortion SL561 at 20kHz

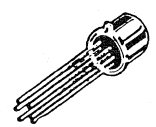
ZN459, ZN459CP

ULTRA LOW NOISE WIDEBAND PREAMPLIFIER

FEATURES

- High Controlled Gain : 60 dB ±1 dB typical
- Low Noise : 40Ω Equivalent Noise Resistance, or 800 pV/$\sqrt{Hz}$
- Wide Bandwidth : 15 MHz typical
- Low Supply Current : <3 mA from 5V

ZN459



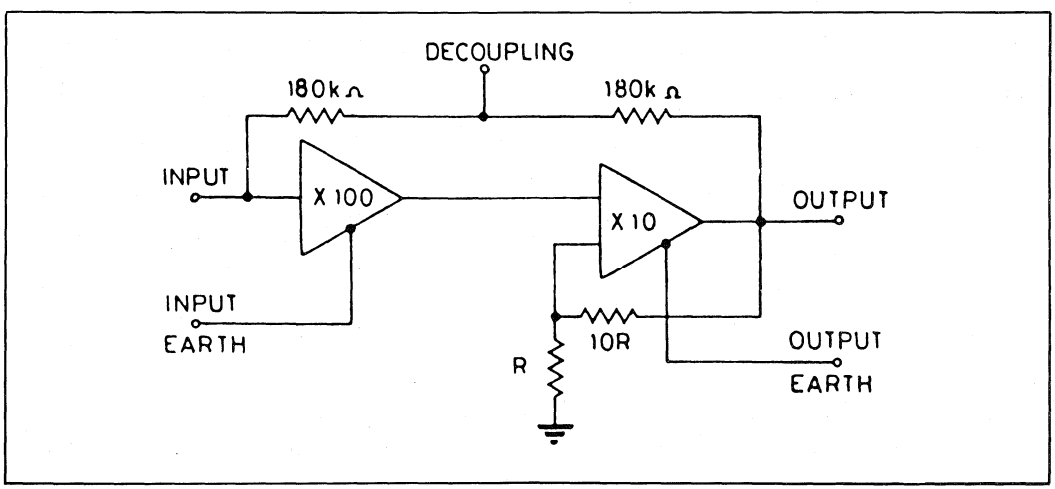
CM6

ZN459CP

DP8

DESCRIPTION

A versatile high grade a.c. pre-amplifier designed for applications requiring ultra low noise such as infra-red imaging and low noise wide band amplifiers e.g. microphone, acoustic emission, transducer bridge amplifier. The matching of open loop gain coupled with small physical size make the ZN459 series ideal for multichannel amplification.



ZN459 OUTLINE CIRCUIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .. .. 6·0 Volts

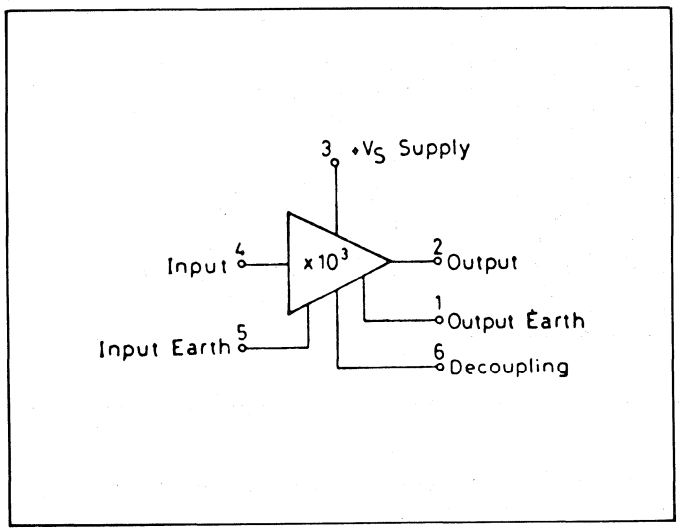
Operating Temperature Range:
for ZN459 .. .. .. −55 to +125°C
for ZN459CP .. .. .. 0 to +70 °C

Storage Temperature Range .. .. .. −55 to +125°C

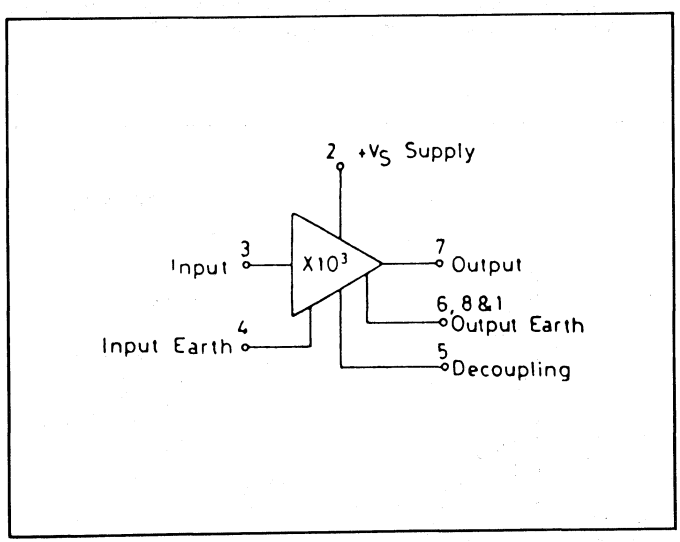
CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C).

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current	2·0	2·5	3·0	mA	
Voltage Gain	59	60	61	dB	10 kHz
TC of Voltage Gain	—	−0·2	—	%/°C	
V_{CC} Coefficient of Voltage Gain	—	25	—	%/V	
Cut-off Frequency	—	15	—	MHz	3 dB down
Input Resistance	3·5	7	—	kΩ	10 kHz
Input Capacitance	—	80	—	pF	Note 1
Noise Resistance	—	40	—	Ω	$R_S = 0$
White Noise Voltage	—	800	1100	$pV/\sqrt{Hz}$	$R_S = 0$
L.F. Spot Noise	—	3	—	$nV/\sqrt{Hz}$	$R_S = 0$, f = 25 Hz
White Noise Current	—	1	—	$pA/\sqrt{Hz}$	
Output Level	1·5	2·0	2·5	V	
Supply Voltage Coefficient of Output Level	—	0·34	—	V/V	
Output Current Limit	0·6	0·8	1·1	mA	Sink current
Total Harmonic Distortion ..	—	0·15	—	%	1 V_{pp} at 10 kHz
Output Resistance	—	75	—	Ω	10 kHz
Supply Rejection Ratio ..	—	42·5	—	dB	
Delay Time	—	20	—	ns	Small signal
Delay Time	—	40	—	ns	100 mV rms input
Positive Input Overdrive ..	—	10	—	mA	
Negative Input Overdrive ..	—	−5	—	V	

Note 1: In P.C.B. The Input Capacitance may be reduced to 25pF by screening between output and input.

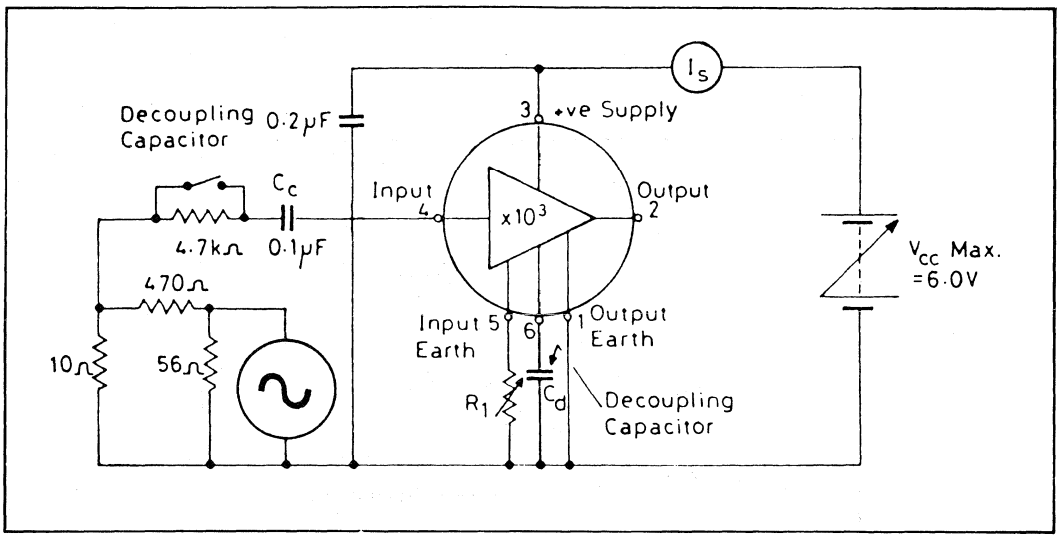


PINNING CONFIGURATION - ZN459



PINNING CONFIGURATION - ZN459CP

GAIN TEST CIRCUIT (ZN459)

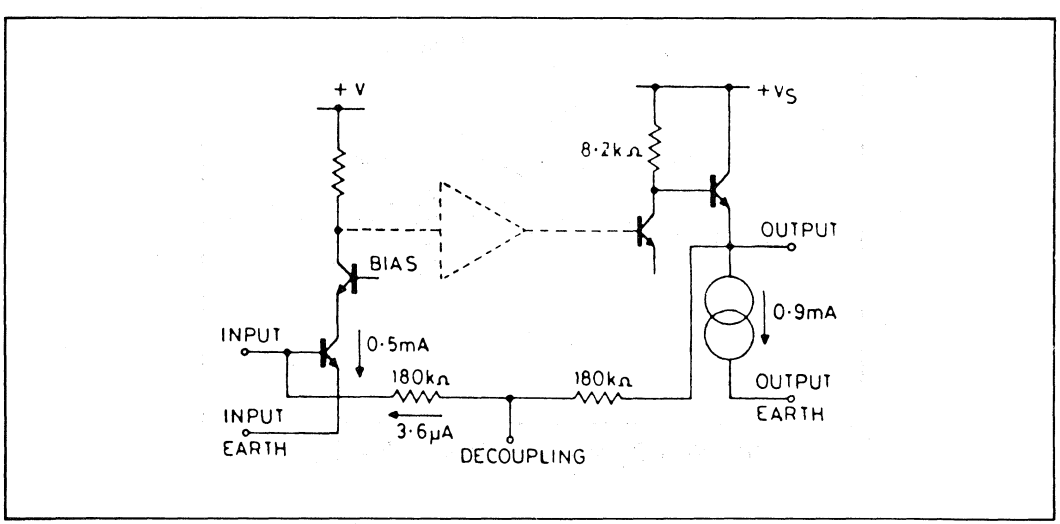


The input impedance may be increased at the expense of noise by including R_1 to vary the gain ($R_1 = 0$, gain $= 10^3$; $R_1 = 470\Omega$, gain $= 10^2$).

C_d is required to decouple the internal feedback loop and in order to obtain a flat frequency response make $C_d \geqslant C_c$.

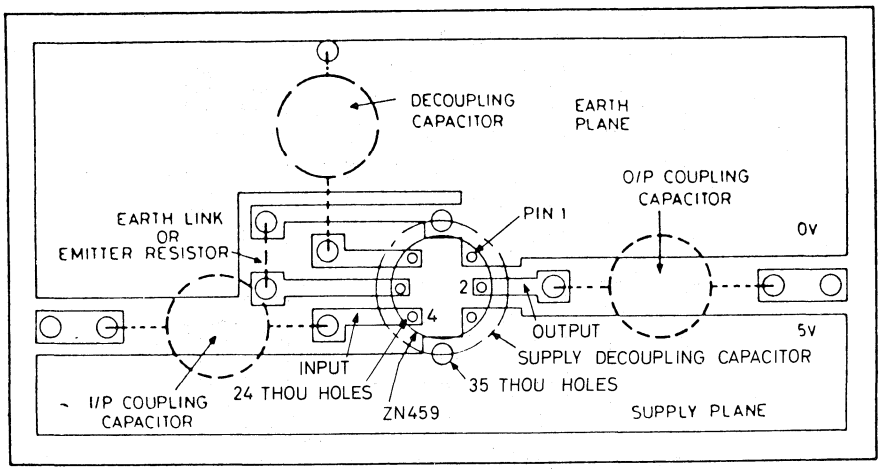
The earth lead of the supply decoupling capacitor should be as close as possible to that of R_1.

For optimum Common Mode Rejection connect a twisted pair between source and pins 4 and 5 of the device, and complete the earth return from source ground.

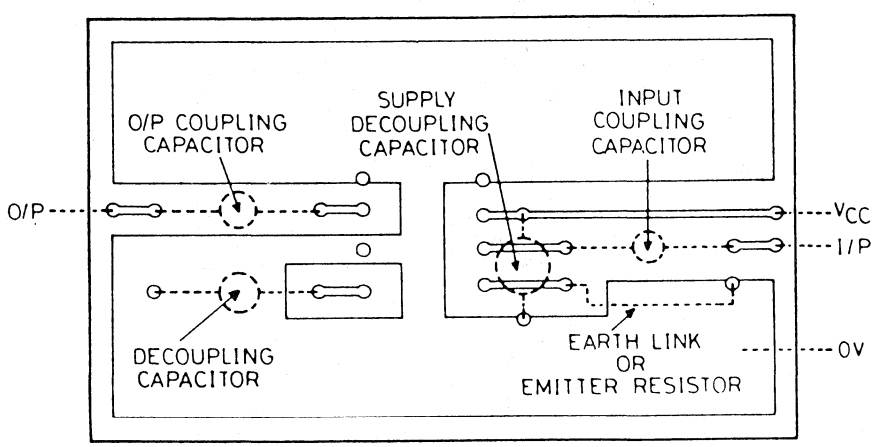


ZN459 INPUT AND OUTPUT CIRCUIT

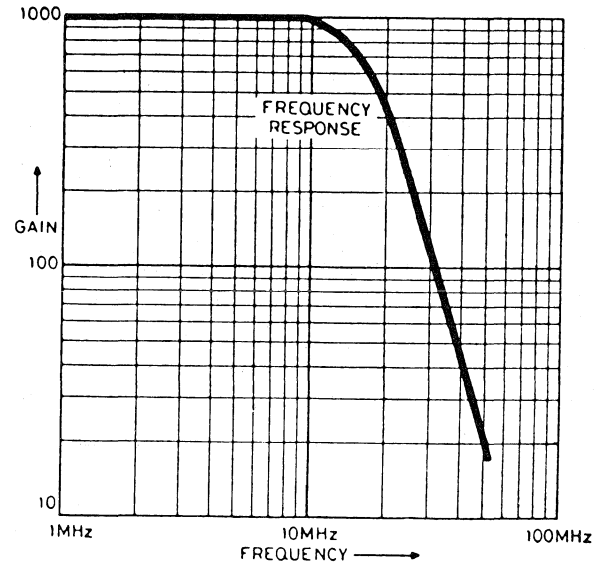
PCB LAYOUT (ZN459)



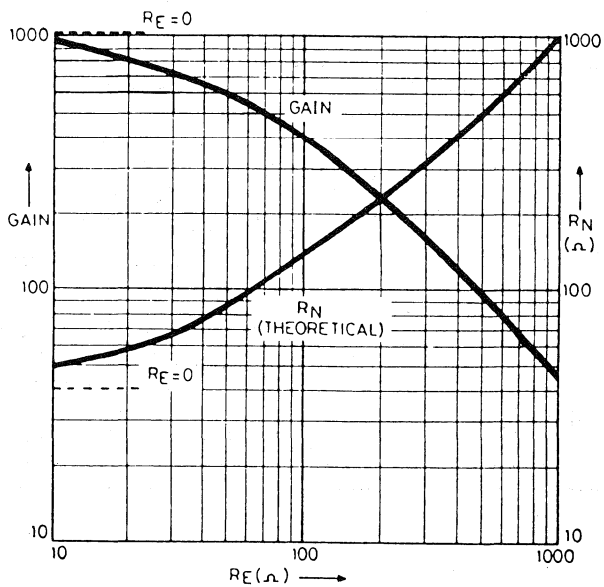
PCB LAYOUT (ZN459CP)



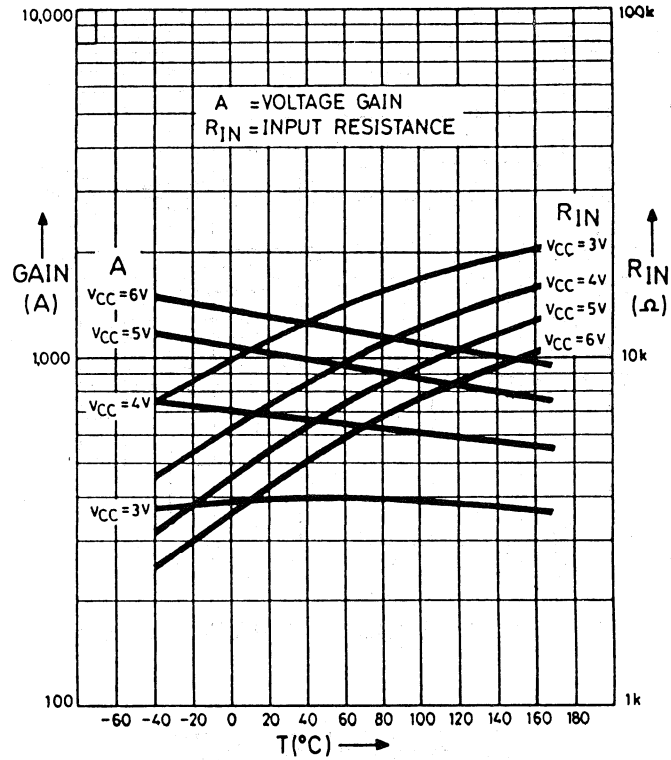
TYPICAL CHARACTERISTICS



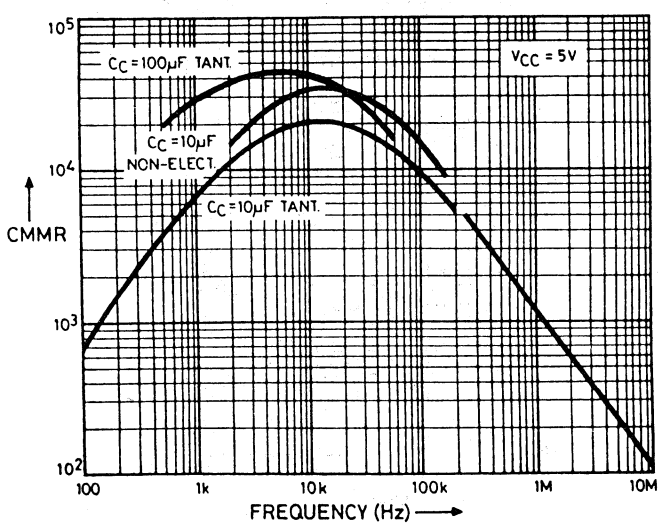
GAIN V_S FREQUENCY



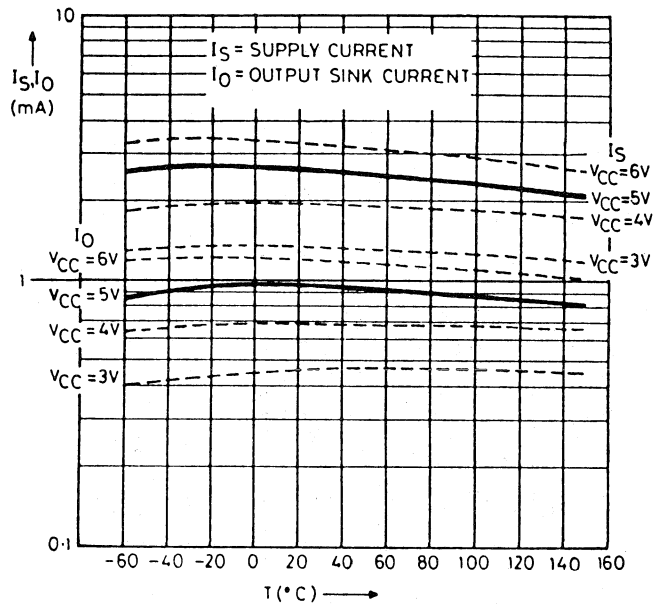
GAIN AND NOISE RESISTANCE V_S EMITTER RESISTANCE



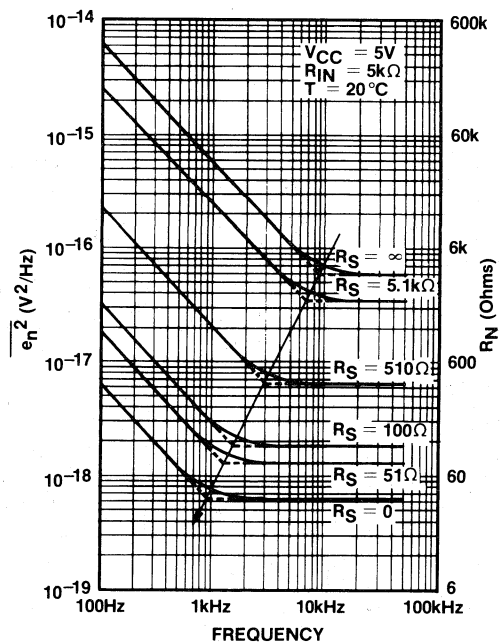
GAIN AND INPUT IMPEDANCE



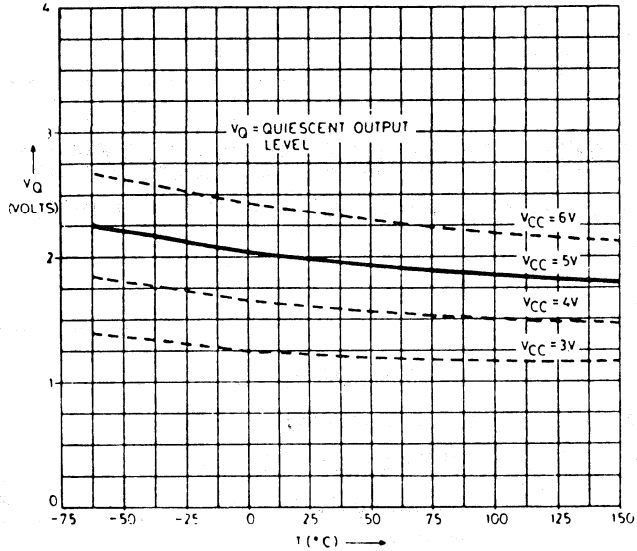
COMMON MODE REJECTION Vs FREQUENCY
(Measured between input earth and output earth)



SUPPLY CURRENT AND OUTPUT SINK CURRENT



NOISE VOLTAGE



QUIESCENT OUTPUT LEVEL

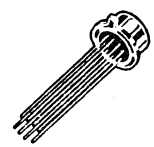
ZN460, ZN460AM, ZN460CP

ULTRA LOW NOISE WIDEBAND PREAMPLIFIER

FEATURES

- **High Controlled Gain** : **60 dB ± 1 dB typical**
- **Programmable Gain** : **50-60 dB typical**
- **Programmable Bandwidth** : **6MHz downwards**
- **Low Noise** : **40Ω Equivalent Noise Resistance, or 800 pV/√Hz**
- **Low Supply Current** : **<3 mA from 5V**

ZN460



CM8

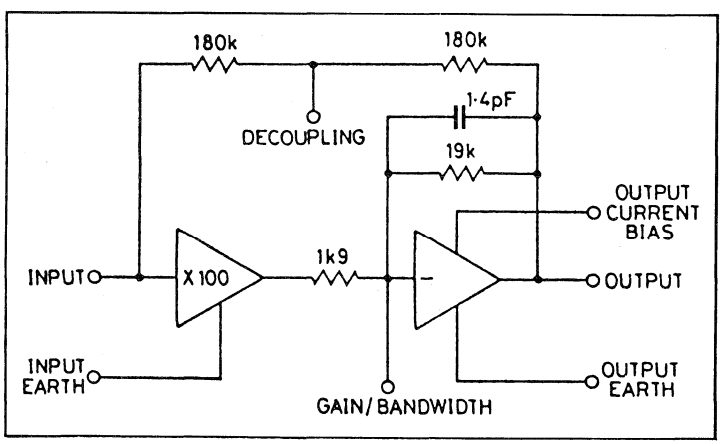
DESCRIPTION

The ZN460 is a versatile high performance AC preamplifier, designed for applications requiring ultra low noise such as infra-red imaging and low noise wideband amplifiers e.g. microphone, acoustic emission, transducer bridge amplifier. The matching of open loop gain, coupled with small physical size, makes the ZN460 ideal for multichannel amplification.

The programmable gain feature allows variable detector gain factors to be trimmed out. The programmable bandwidth feature allows the noise bandwidth to be reduced to the required signal bandwidth, thus minimising the wideband output noise.

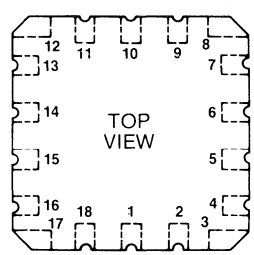
ZN460CP

DP8



CIRCUIT DIAGRAM

ZN460AM



AM18

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .. .. 6.0 Volts

Operating Temperature Range:

for ZN460 and ZN460AM .. .. .. −55 to +125°C

for ZN460CP .. .. .. 0 to +70 °C

Storage Temperature Range .. .. .. −55 to +125°C

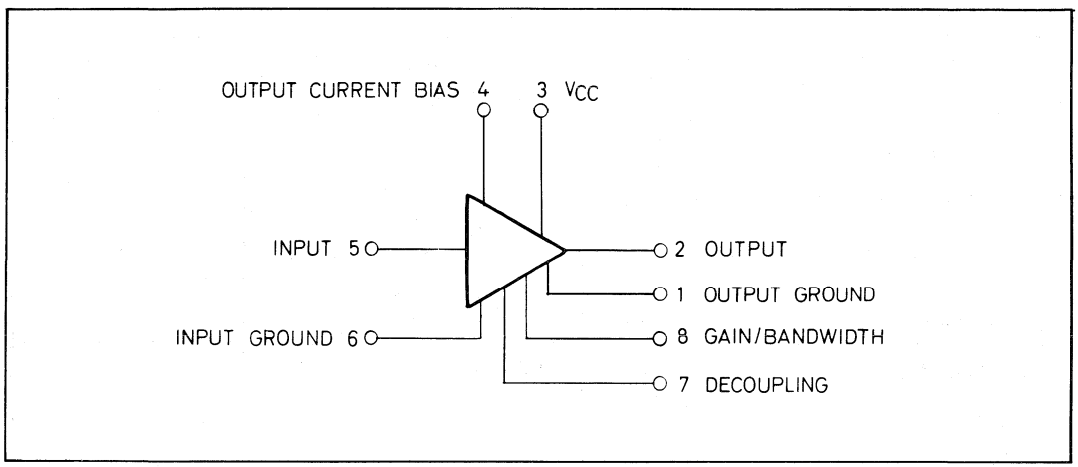
CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C).

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current	2.0	2.5	3.0	mA	
Voltage Gain	59	60	61	dB	10 kHz (Note 1)
TC of Voltage Gain	—	−0.2	—	%/°C	
V_{CC} Coefficient of Voltage Gain	—	25	—	%/V	
Cut-off Frequency	—	6	—	MHz	3 dB down (Note 1)
Input Resistance	3.5	7		kΩ	10 kHz
Input Capacitance	—	80	—	pF	Note 2
Noise Resistance	—	40	—	Ω	$R_S = 0$
White Noise Voltage	—	800	1100	$pV/\sqrt{Hz}$	$R_S = 0$
L.F. Spot Noise	—	3		$nV/\sqrt{Hz}$	$R_S = 0$, f = 25 Hz
White Noise Current	—	1	—	$pA/\sqrt{Hz}$	
Output Level	1.5	2.0	2.5	V	
Output Swing	2	4 —		V_{pp} V_{pp}	$R_F = \infty$ $R_F = 6\ k\Omega$
Supply Voltage Coefficient of Output Level	—	0.34	—	V/V	
Output Current Limit	0.6	0.8	1.1	mA	Note 3
Total Harmonic Distortion ..	—	0.15	—	%	1 V_{pp} at 10 kHz
Output Resistance	—	75	—	Ω	10 kHz
Supply Rejection Ratio ..	—	42.5	—	dB	
Delay Time	—	20	—	ns	Small signal
Delay Time	—	40	—	ns	100 mV rms input
Positive Input Overdrive ..	—	—	10	mA	
Negative Input Overdrive ..	—	—	−5	V	

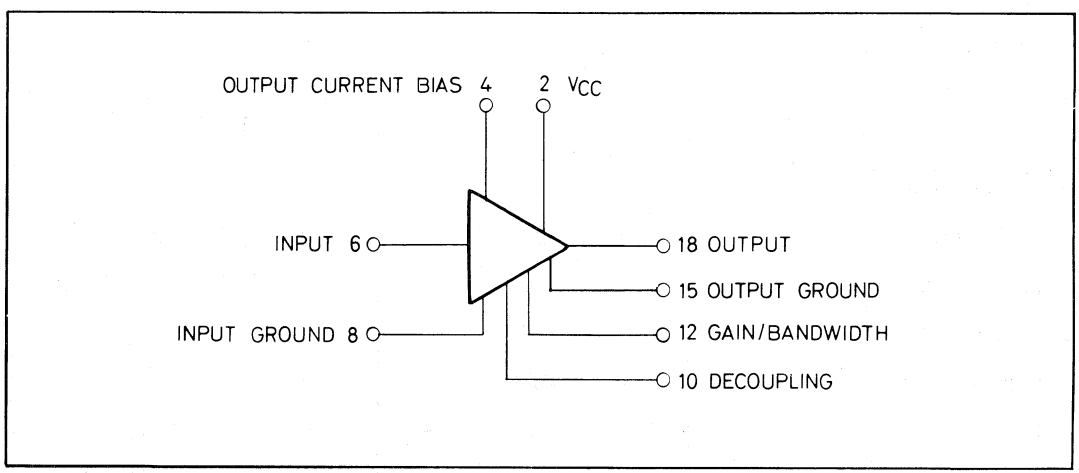
NOTE 1. Without external components.

NOTE 2. In P.C.B. The Input Capacitance may be reduced to 25 pF by screening between output and input

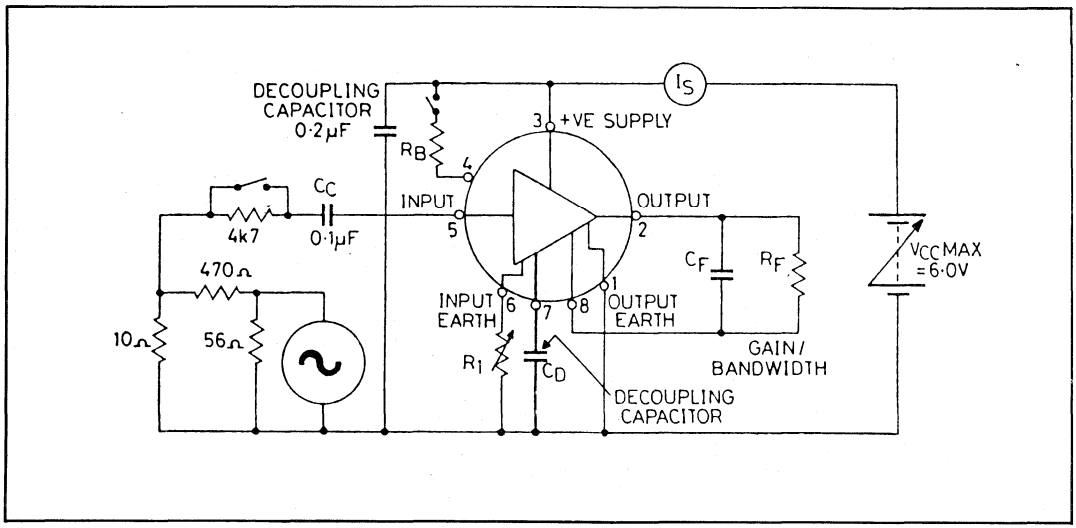
NOTE 3. Sink current without external bias resistor.



PINNING CONFIGURATION - ZN460 and ZN460CP



PINNING CONFIGURATION - ZN460AM



GAIN TEST CIRCUIT (ZN460)

The input impedance may be increased at the expense of noise by including R_1 to vary the gain ($R_1 = 0$, gain $= 10^3$; $R_1 = 470\Omega$, gain $= 10^2$).

C_D is required to decouple the internal feedback loop and in order to obtain a flat frequency response make $C_D \geqslant C_C$.

The earth lead of the supply decoupling capacitor should be as close as possible to that of R_1.

R_B may be used to increase the output quiescent current up to a maximum of 5 mA. The value is given by:

$$I_O = \frac{10(V_{CC} - 1.34)}{R_B'}$$

where R_B' is the parallel combination of R_B and 40 kΩ.

The gain and bandwidth may be modified by means of R_F and C_F. The gain is given by:

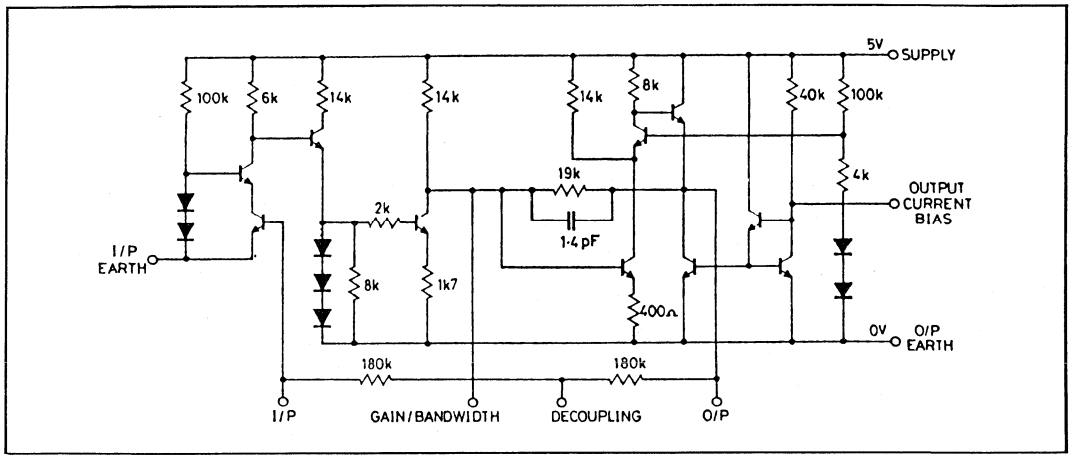
$$A = \frac{10^3 . R_F}{R_F + 19} \text{ with } R_F \text{ in k}\Omega$$

and the bandwidth by:

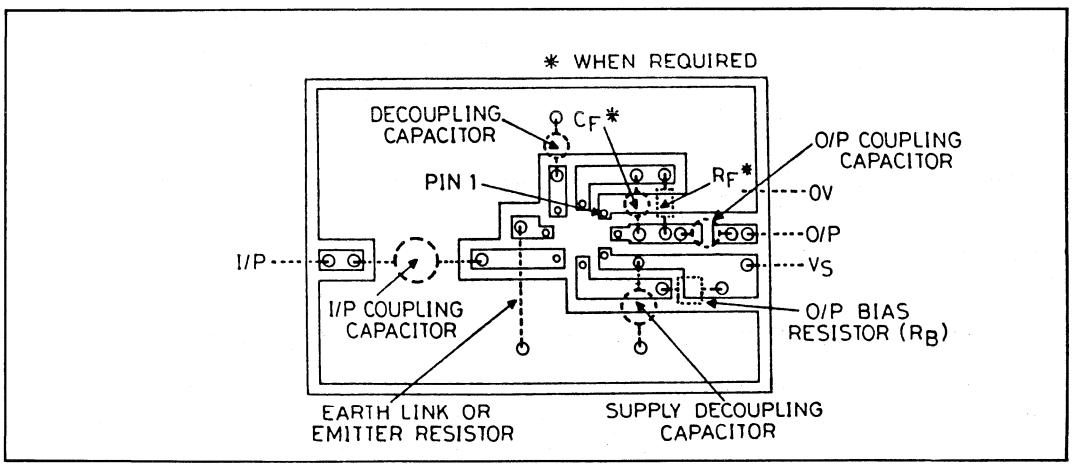
$$f_C = \frac{10^{12}}{2\pi R_F' (C_F + 1.4)} \text{ Hz with } C_F \text{ in pF}$$

where R_F' is the parallel combination of R_F and 19 kΩ.

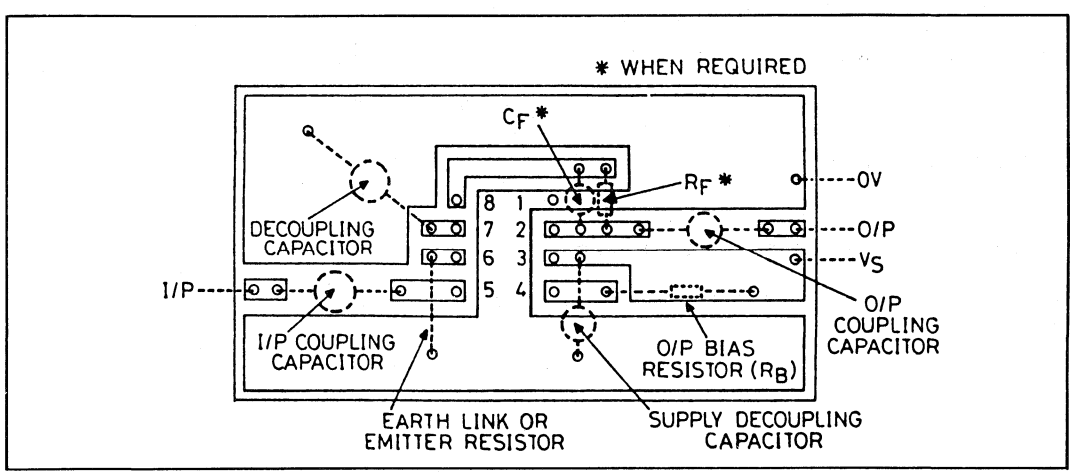
The recommended minimum value of R_F is 6 kΩ since a lesser value reduces the output swing below $2V_{pp}$.



ZN460 CIRCUIT DIAGRAM (Typical Values)

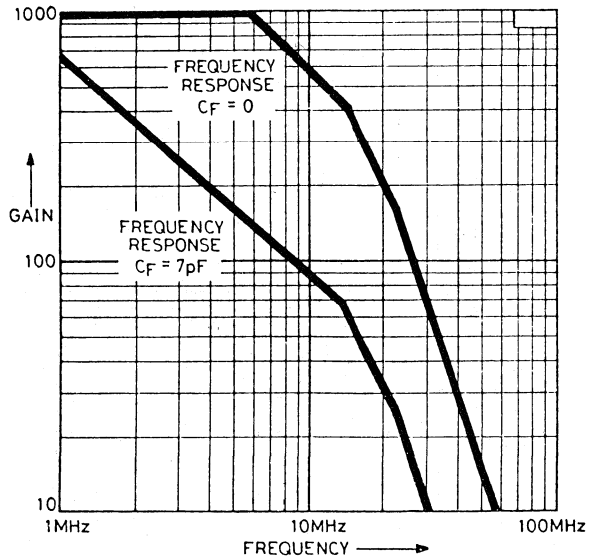


PCB LAYOUT -ZN460

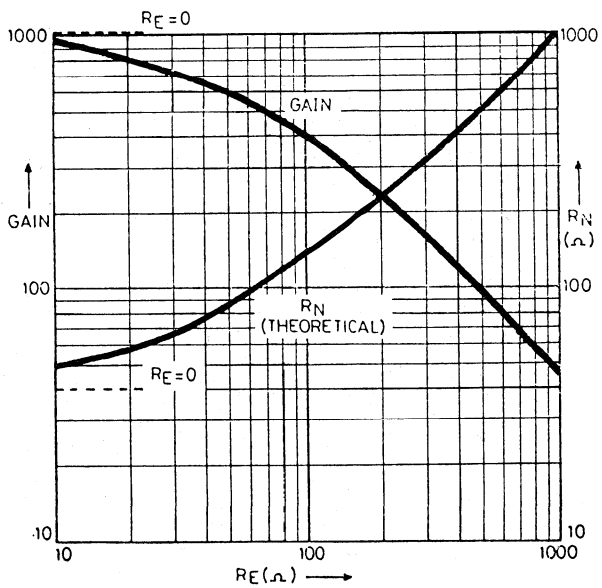


PCB LAYOUT ZN460CP

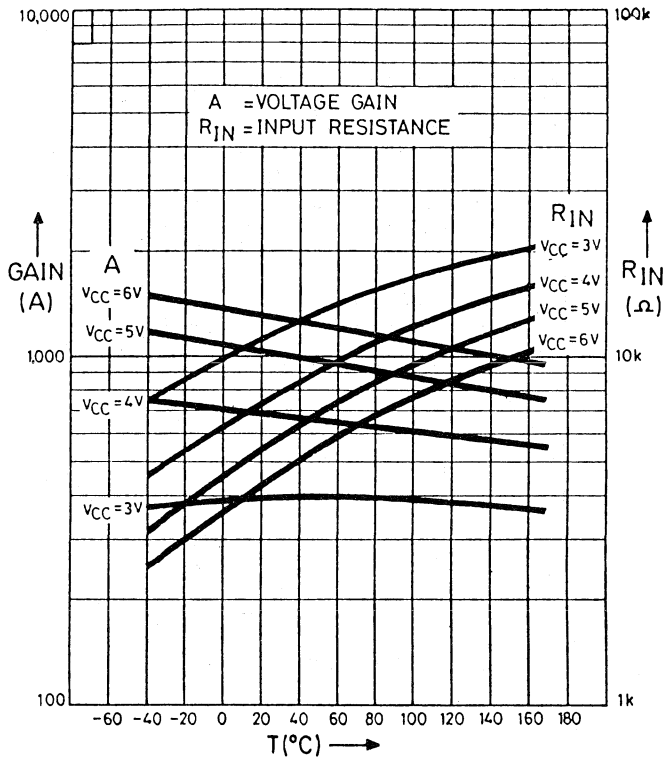
TYPICAL CHARACTERISTICS



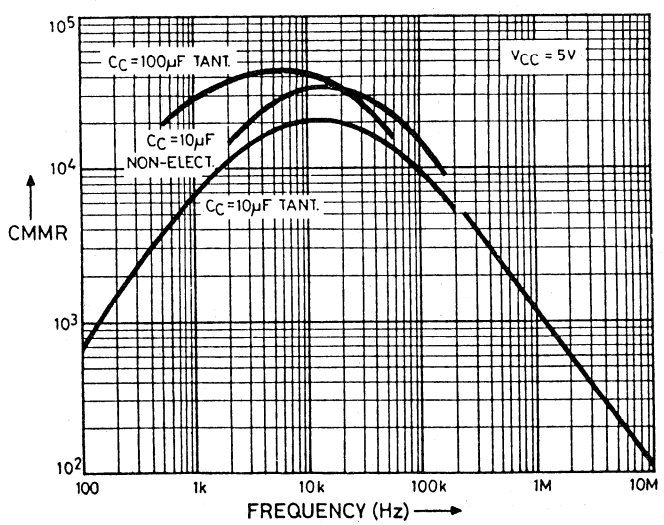
GAIN V_S FREQUENCY ($R_F = \infty$)



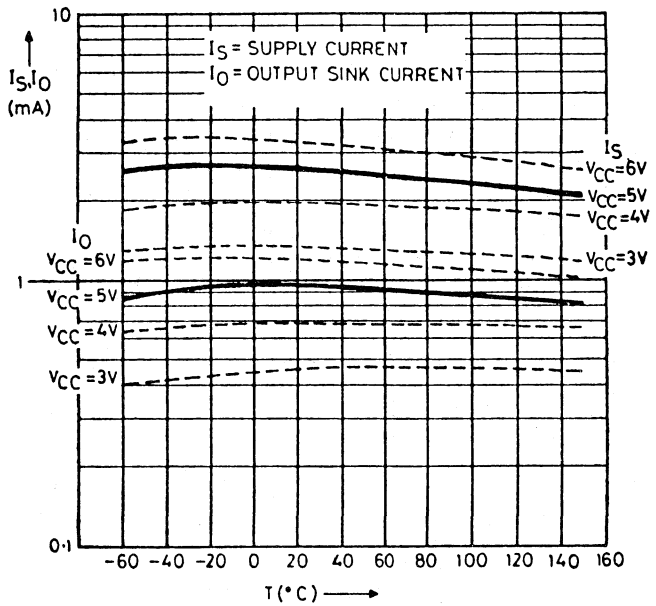
GAIN AND NOISE RESISTANCE V_S EMITTER RESISTANCE ($R_F = \infty$)



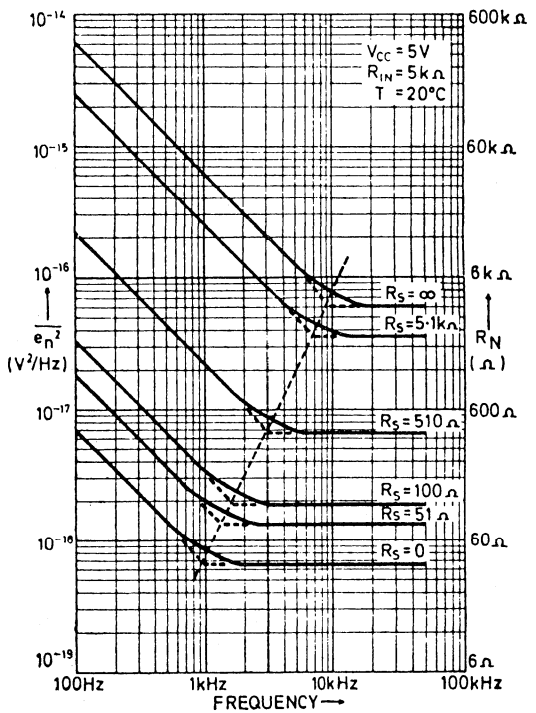
GAIN AND INPUT IMPEDANCE



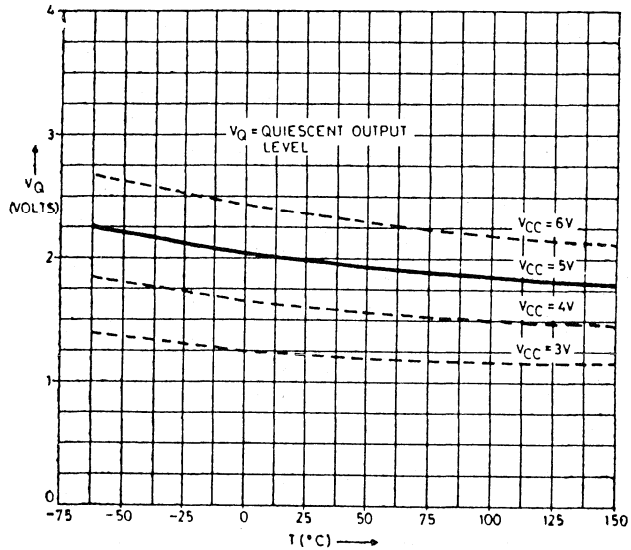
COMMON MODE REJECTION V_S FREQUENCY
(Measured between input earth and output earth)



SUPPLY CURRENT AND OUTPUT SINK CURRENT ($R_B = \infty$)



NOISE VOLTAGE



QUIESCENT OUTPUT LEVEL

SL360G & SL362C

HIGH PERFORMANCE NPN DUAL TRANSISTOR ARRAYS

The SL360G and SL362C are high performance NPN dual transistor arrays fabricated as monolithic silicon devices. They feature accurate parameter matching and close thermal tracking. They have high transition frequencies (typ. 2.2GHz) and low device capacitance. In addition the SL362C offers good noise performance (1.6dB noise figure at 60MHz).

APPLICATIONS

- Instrumentation
- PCM Repeaters
- Analog Signal Processing
- High Speed Switches — Digital and Analog

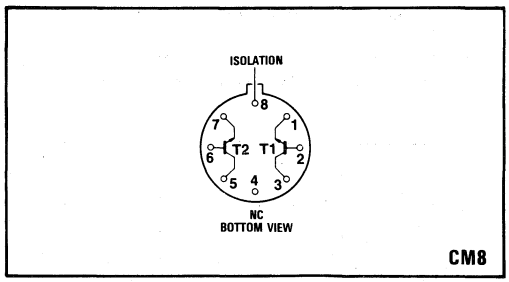


Fig. 1 Pin connections

ORDERING INFORMATION

SL360 G CM
SL362 C CM

FEATURES

- Accurate Parameter Matching.
- High f_T (1.5GHz min., SL360)
- Low Noise (1.6dB at 60MHz SL362)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Type	Value			Units	Conditions
			Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	Both	10	32		V	I_C = 10μA
Collector isolation breakdown	BV_{CIO}	Both	16	60		V	I_C = 10μA
Emitter base leakage	I_{EBO}	SL360/362C			1	μA	V_{EB} = 4V
Emitter base leakage	I_{EBO}	SL360			1	nA	V_{EB} = 2V
Collector emitter breakdown	LV_{CEO}	All	7	14		V	I_C = 5mA
DC current gain	H_{FE}	SL360	30	65			V_{CE} = 2V, I_E = 5mA
		SL362	30	70			V_{CE} = 2V, I_E = 1mA
Transition frequency	f_T	SL360G	1.6	2.2		GHz	V_{CE} = 2.5V, I_E = 25mA, f = 200MHz (See Notes)
		SL362	1.0	1.5		GHz	V_{CE} = 5V, I_F = 5mA, f = 200MHz
Input offset voltage	V_{BE1} - V_{BE2}	SL360		3	10	mV	V_{CE} = 2V, I_E = 1mA
		SL362		5		mV	V_{CE} = 2V, I_E = 1mA
Input offset current	H_{FE1}/H_{FE2}	Both	0.9	1.0	1.1		V_{CE} = 2V, I_E = 5mA
Saturation voltage	$V_{CE(SAT)}$	SL360		0.25	0.6	V	I_E = 10mA, I_B = 1mA
Noise figure	NF	SL362		1.6	2.0	dB	I_E = 1mA, R_S = 200Ω, f = 60MHz
Collector base capacitance	C_{OB}	SL360		0.5		pF	V_{CB} = 0V
		SL362		1.3		pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}	SL360		2.3		pF	V_{CI} = 0V
		SL362		3.8		pF	V_{CI} = 0V
Emitter base capacitance	C_{TE}	SL360		0.5		pF	V_{BE} = 0V
		SL362		2.1		pF	V_{BE} = 0V
Forward base emitter voltage	$V_{BE(ON)}$	SL360		0.72		V	I_E = 1mA, V_{CE} = 2V
Collector base leakage	I_{CBO}	SL360			1	nA	V_{CB} = 10V
Collector isolation leakage	I_{CIO}	SL360			1	nA	V_{CI} = 10V

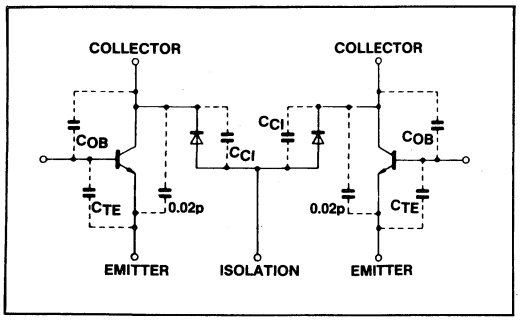


Fig.2 Equivalent circuit for SL360, SL362

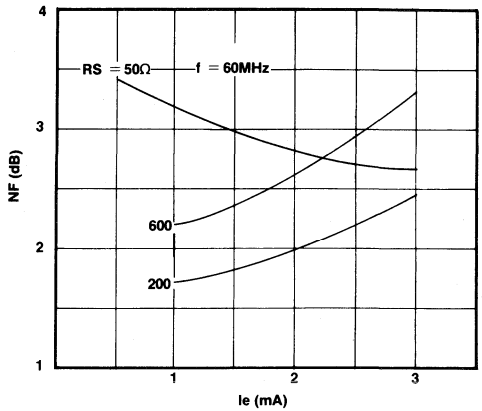


Fig. 3 Typical noise figure emitter current for SL362

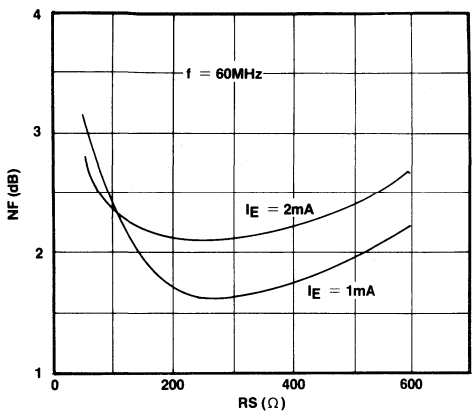


Fig. 4 Typical noise figure v source impedance for SL362

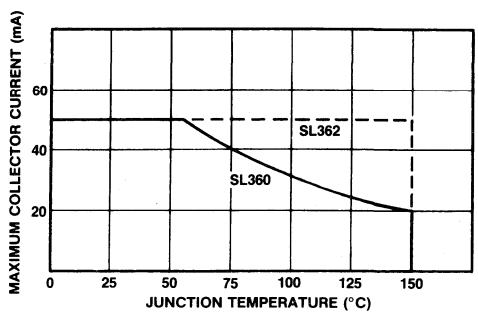


Fig.5 Max. continuous collector current vs junction temperature

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The absolute maximum ratings are limiting values above which life may be shortened or specified parameters may be degraded.

The isolation pin (substrate) must be connected to the most negative point of the circuit to maintain electrical isolation between transistors.

Electrical ratings

V_{CB} = 10V V_{EB} = 4V V_{CE} = 8V
V_{CI} = 16V I_C = 20mA (SL360); 50mA (SL362)
(see Figure 5)

Thermal ratings

	CM8
Storage temperature	−55°C to +150°C
Operating junction temperature	150°C
Thermal resistance (see Note)	
Chip-to-case	265° C/W
Chip-to-ambient	425° C/W

These figures are worst case, assuming all power is dissipated in one transistor. If the power is equally shared between the two transistors, both thermal resistance figures can be reduced by 50° C/watt.

SL2363 & SL2364

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5GHz, (typically 5GHz).

FEATURES

- Complete Dual Long-Tailed Pair in One Package.
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ORDERING INFORMATION

SL2363 C CM
SL2363 CB CM
SL2364 C DC
SL2364 C DP
SL2364 C LC
SL2364 C MP
SL2364 CB DC

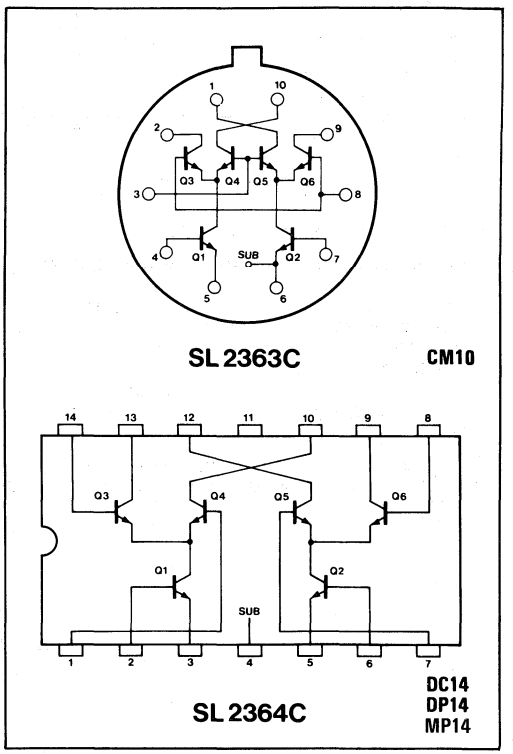


Fig. 1 Pin connections for CM, DC, DP and MP packages - top view. NOTE: See Fig. 4 for pinout of SL2364 in LC package

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10μA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10μA
BV_{CIO}	16	40		V	I_C = 10μA
h_{FE}	50	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C (Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C (Tail) = 8 mA, V_{CE} = 2V
$\Delta V_{BE}/T_{AMB}$		-1.7		mV/°C	I_C (Tail) = 8 mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1. ΔV_{BE} applies to $V_{BEQ3} - V_{BEQ4}$ and $V_{BEQ5} - V_{BEQ6}$

TYPICAL CHARACTERISTICS

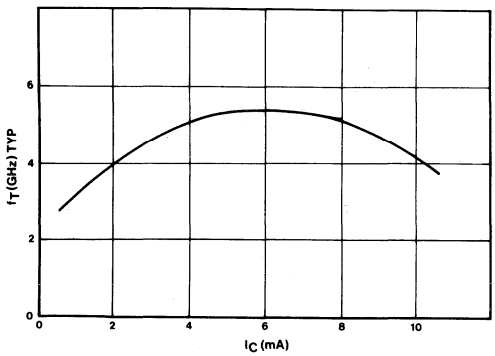


Fig. 2 Collector current

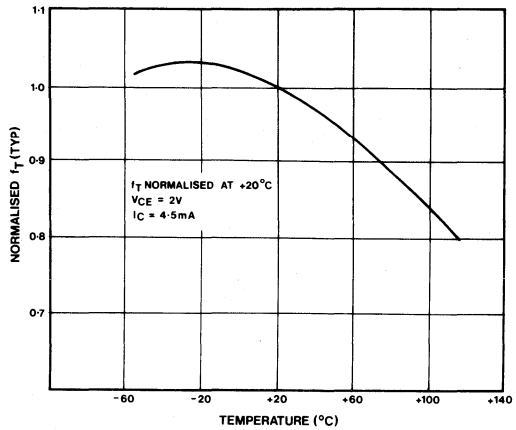


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature −55°C to +150°C
Maximum junction temperature +150°C
Package thermal resistance (°C/W):
Chip to case 65 (CM10)
Chip to ambient 225 (CM10) 175 (DP14)
V_{CBO} = 10V, V_{EBO} = 2.5V, V_{CEO} = 6V, V_{CIO} = 15V, IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

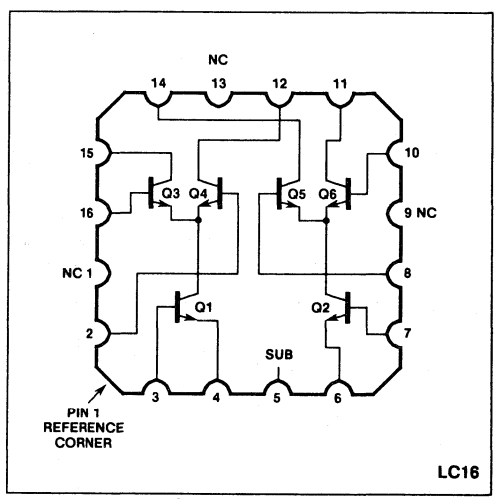


Fig.4 SL2364 LC pin connections

SL3127

HIGH FREQUENCY NPN TRANSISTOR ARRAY

The SL3127C is a monolithic array of five high frequency low current NPN transistors in a 16 lead DIL package. The transistors exhibit typical f_{TS} of 1.6GHz and wideband noise figures of 3.6dB. The SL3127C is pin compatible with the CA3127.

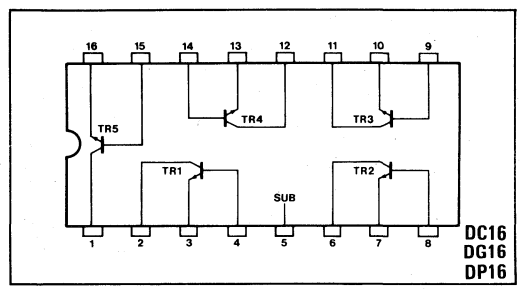


Fig.1 Pin connections SL3127

FEATURES

- f_T Typically 1.6 GHz
- Wideband Noise Figure 3.6dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ORDERING INFORMATION

SL3127 C DC
SL3127 C DP
SL3127 CB DC
SL3127 A DG

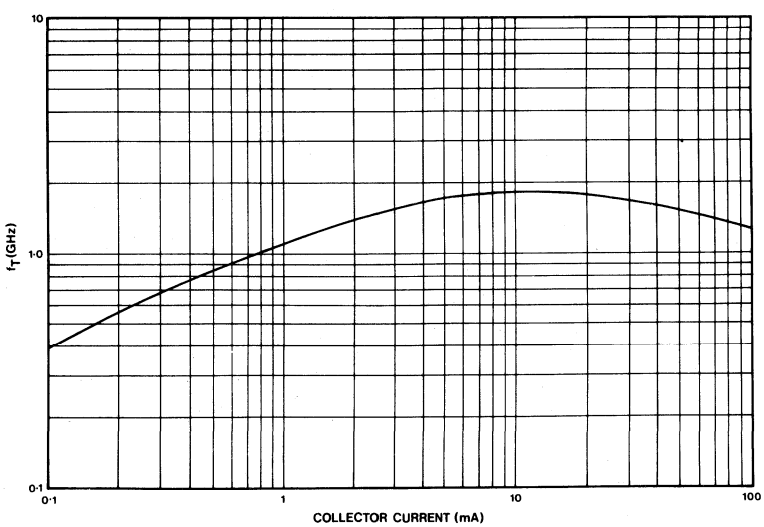


Fig.2 Transition frequency (f_T) v. collector current (V_{CB}=2V, f=200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22° C ± 2° C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static characteristics						
Collector base breakdown	BV_{CBO}	20	30		V	I_C = 10μA, I_E = 0
Collector emitter breakdown	LV_{CEO}	15	18		V	I_C = 1mA, I_B = 0
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	I_C = 10μA, I_R = I_E = 0
Base to isolation breakdown	BV_{BIO}	10	20		V	I_B = 10μA, I_C = I_E = 0
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V, I_C = 1mA
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.26	0.5	V	I_C = 10mA, I_B = 1mA
Emitter base leakage current	I_{EBO}		0.1	1	μA	V_{EB} = 4V
Base emitter saturation voltage	$V_{BE(SAT)}$		0.95		V	I_C = 10mA, I_B = 1mA
Base emitter voltage difference, all transistors	ΔV_{BE}		0.45	5	mV	V_{CE} = 6V, I_C = 1mA
Input offset current	ΔI_B		0.2	3	μA	V_{CE} = 6V, I_C = 1mA
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		μV/° C	V_{CE} = 6V, I_C = 1mA
Temperature coefficient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/° C	V_{CE} = 6V, I_C = 1mA
Static forward current ratio	H_{FE}	35	95			V_{CE} = 6V, I_C = 5mA
		35	100			V_{CE} = 6V, I_C = 0.1mA
		40	100			V_{CE} = 6V, I_C = 1mA
Collector base leakage	I_{CBO}		0.3		nA	V_{CB} = 16V
Collector isolation leakage	I_{CIO}		0.6		nA	V_{CI} = 20V
Base isolation leakage	I_{BIO}		100		nA	V_{BI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance	C_{CB}		0.4		pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}		0.8		pF	V_{CI} = 0V
Dynamic characteristics						
Transition frequency	f_T		1.6		GHz	V_{CE} = 6V, I_C = 5mA
Wideband noise figure	NF		3.6		dB	f = 60MHz, V_{CC} = 6V, I_C = 2mA, R_S = 200Ω
Knee of 1/f noise curve			1		kHz	

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life maybe shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 20 volt
V_{EB} = 4.0 volt
V_{CE} = 15 volt
V_{CI} = 20 volt
I_C = 20 mA
Maximum individual transistor dissipation 200 mWatt
Storage temperature −55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):−

Package Type	DC16	DP16
Chip to case	40	
Chip to ambient	120	180

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100° C/watt.

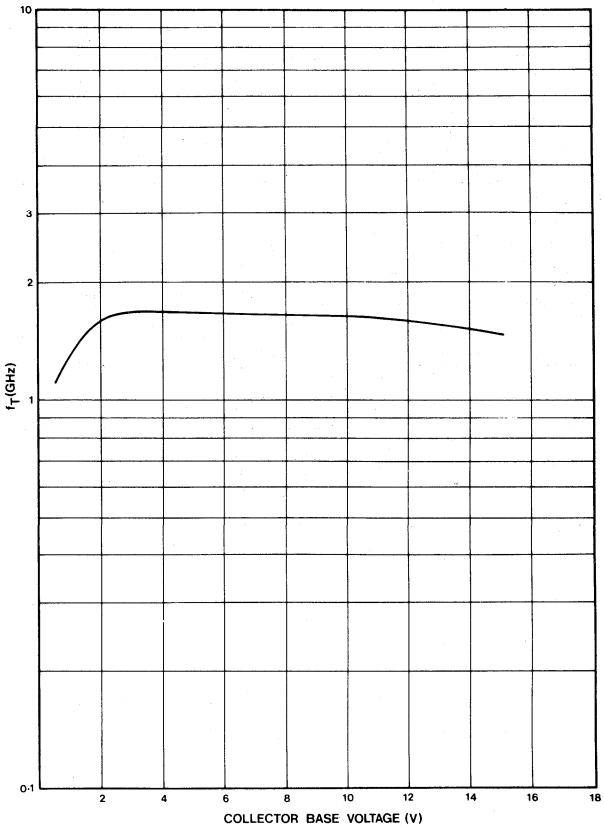


Fig.3 Transition frequency (f_T) v. collector base voltage

(I_C = 5mA, Frequency = 200MHz)

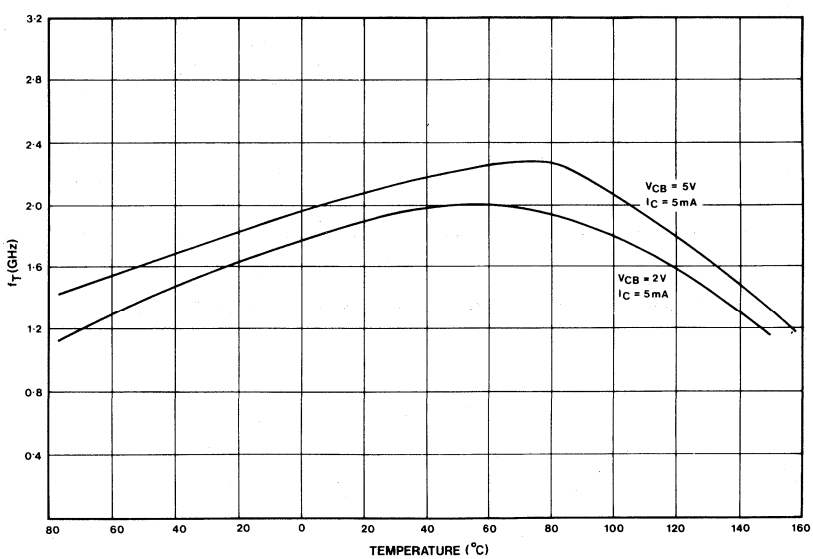


Fig.4 Variation of transition frequency (f_T) with temperature

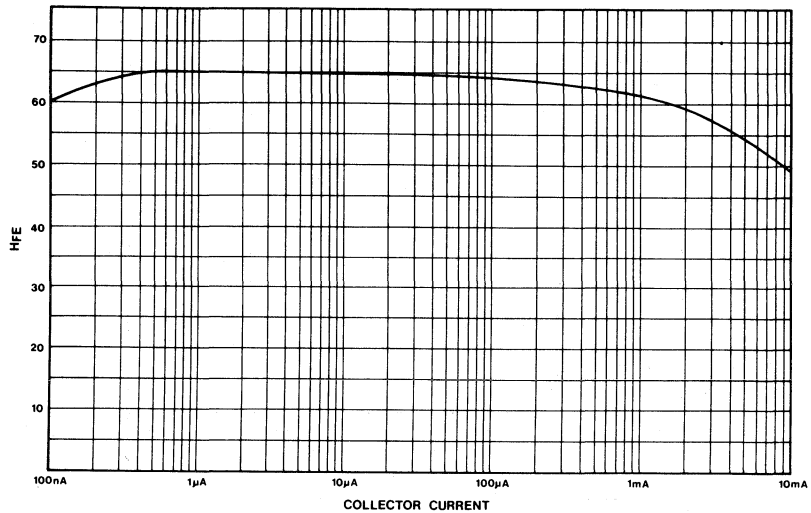


Fig.5 DC current gain v. collector current

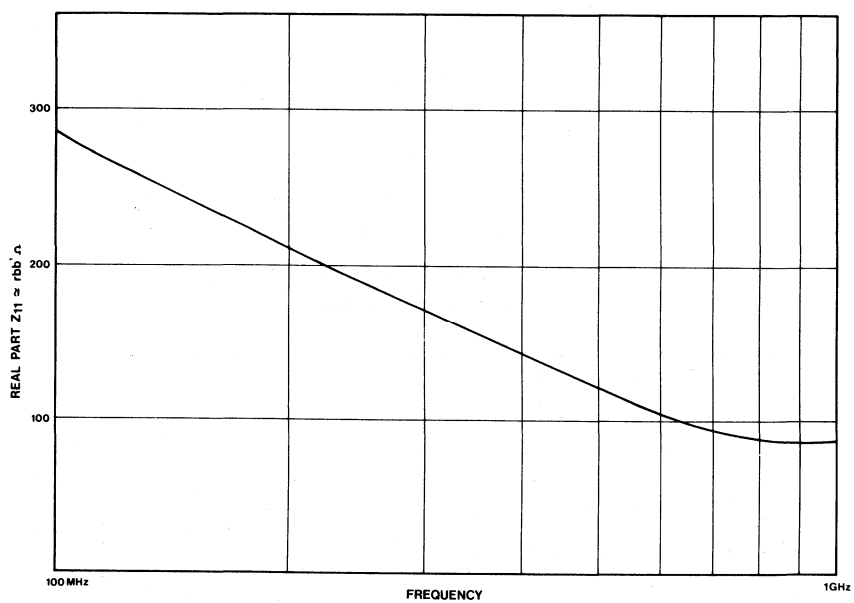


Fig.6 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \triangleq r_{bb'}$)

SL3145

1.6GHz NPN TRANSISTOR ARRAYS

The SL3145C is a monolithic array of five high frequency low current NPN transistors. The SL3145C consists of 3 isolated transistors and a differential pair in a 14 lead DIL package. The transistors exhibit typical f_{TS} of 1.6GHz and wideband noise figures of 3.0dB. The device is pin compatible with the CA3046. The SL3145E has guaranteed C_{CB} and f_T figures.

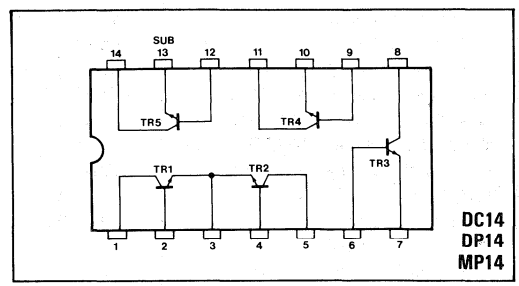


Fig.1 Pin connections SL3145

FEATURES

- f_T Typically 1.6 GHz
- Wideband Noise Figure 3.0dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ORDERING INFORMATION

SL3145 C DC
SL3145 C DP
SL3145 C MP
SL3145 CB DC
SL3145 E DC
SL3145 E DP

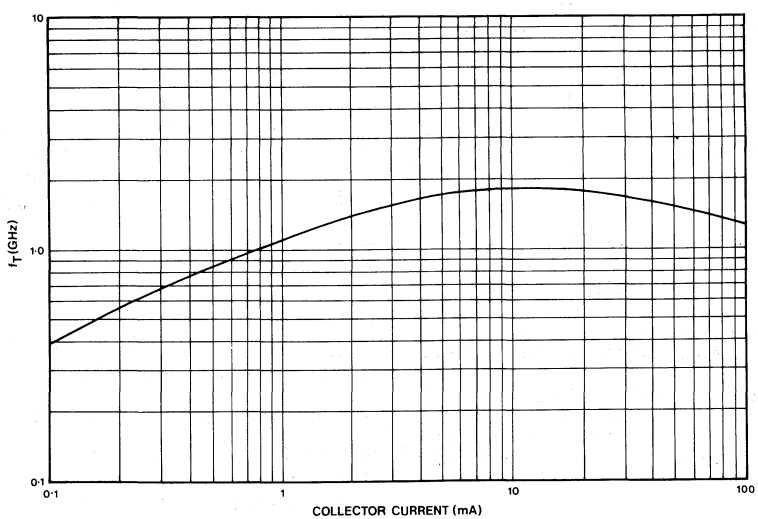


Fig.2 Transition frequency (f_T) v. collector current (V_{CB} = 2V, f = 200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static characteristics						
Collector base breakdown	BV_{CBO}	20	30		V	I_C = 10μA,I_E = 0
Collector emitter breakdown	LV_{CEO}	15	18		V	I_C = 1mA,I_B = 0
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	I_C = 10μA,I_R = I_E = 0
Base to isolation breakdown	BV_{BIO}	10	20		V	I_B = 10μA,I_C = I_E = 0
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V,I_C = 1mA
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.26	0.5	V	I_C = 10mA,I_B = 1mA
Emitter base leakage current	I_{EBO}		0.1	1	μA	V_{EB} = 4V
Base emitter saturation voltage	$V_{BE(SAT)}$		0.95		V	I_C = 10mA,I_B = 1mA
Base emitter voltage difference, all transistors except TR1,TR2	ΔV_{BE}		0.45	5	mV	V_{CE} = 6V,I_C = 1mA
Base emitter voltage difference TR1, TR2	ΔV_{BE}		0.35	5	mV	V_{CE} = 6V,I_C = 1mA
Input offset current (except for TR1, TR2)	ΔI_B		0.2	3	μA	V_{CE} = 6V,I_C = 1mA
Input offset current TR1, TR2	ΔI_B		0.2	2	μA	V_{CE} = 6V,I_C = 1mA
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		μV/°C	
Temperature coefficient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/°C	V_{CE} = 6V,I_C = 1mA
Static forward current ratio	H_{FE}	40	100			V_{CE} = 6V,I_C = 1mA
Collector base leakage	I_{CBO}		0.3		nA	V_{CB} = 16V
Collector isolation leakage	I_{CIO}		0.6		nA	V_{CI} = 20V
Base isolation leakage	I_{BIO}		100		nA	V_{BI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance						
SL3145C	C_{CB}		0.4		pF	V_{CB} = 0V
SL3145E			0.4	1.1	pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}		0.8		pF	V_{CI} = 0V
Dynamic characteristics						
Transition frequency						
SL3145C	f_T		1.6		GHz	V_{CE} = 6V,I_C = 5mA
SL3145E		1.2			GHz	V_{CE} = 6V,I_C = 10mA
Wideband noise frequency	NF		3.0		dB	V_{CE} = 2V,R_S = 1kΩ I_C = 100μA,f = 60MHz
Knee of 1/f noise curve			1		kHz	V_{CE} = 6V,R_S = 200Ω I_C = 2mA

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life maybe shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 20 volt
V_{EB} = 4.0 volt
V_{CE} = 15 volt
V_{CI} = 20 volt
Ic = 20 mA

Maximum individual transistor dissipation 200 mWatt
Storage temperature −55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):−

Package Type	DC14	DP14
Chip to case	40	
Chip to ambient	120	180

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100° C/watt.

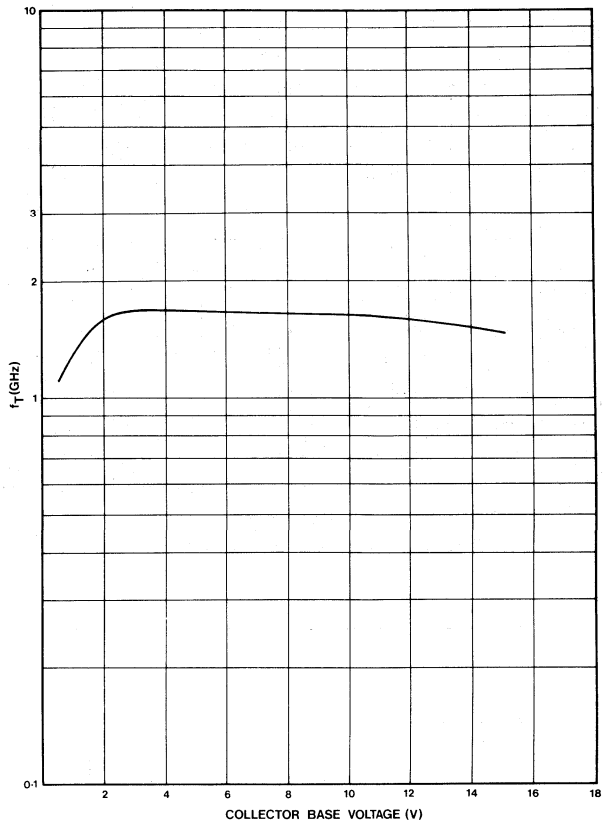


Fig.3 Transition frequency (f_T) v. collector base voltage (I_C = 5mA, frequency = 200MHz)

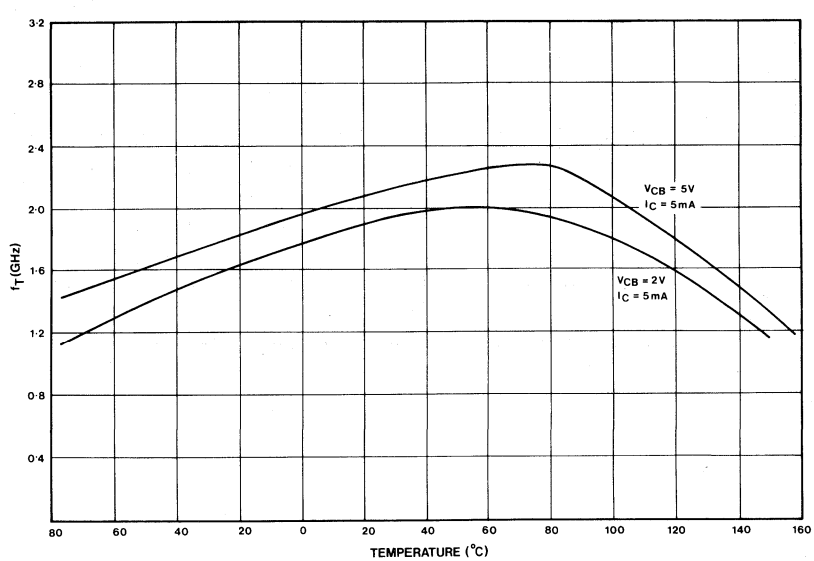


Fig.4 Variation of transition frequency (f_T) with temperature

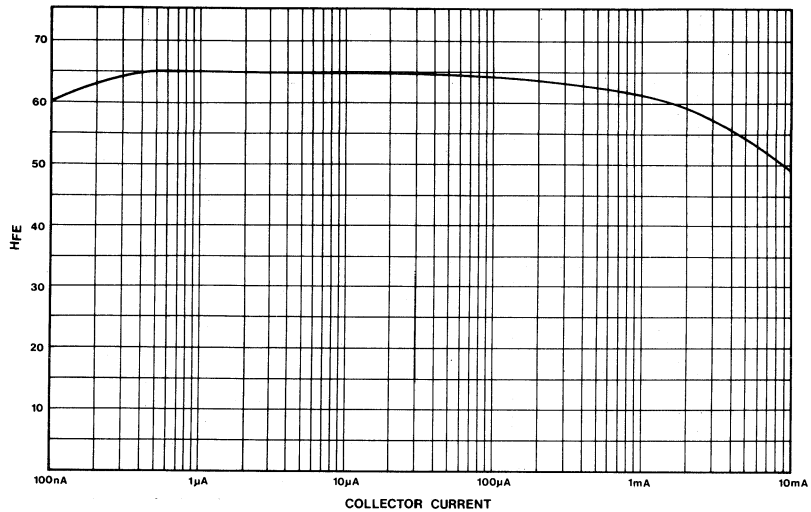


Fig.5 DC current gain v. collector curent

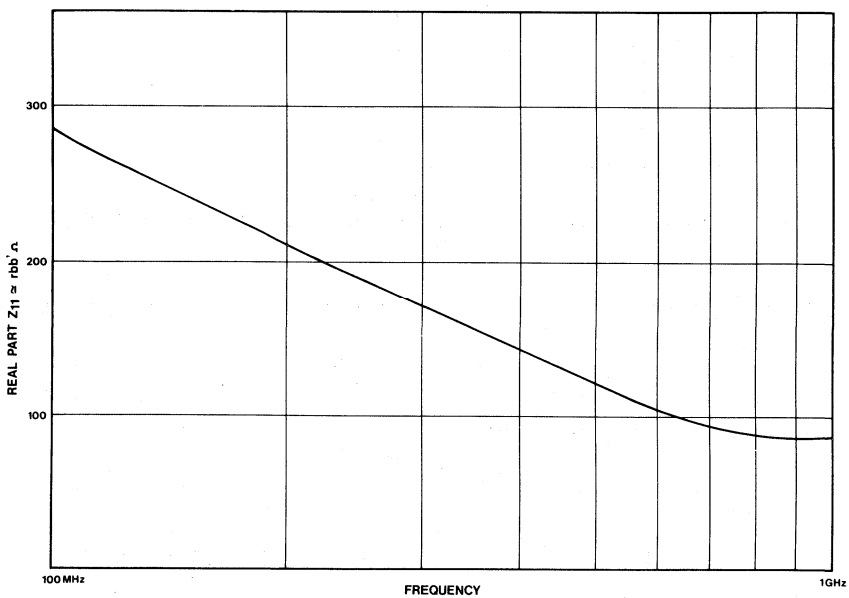


Fig.6 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \simeq r66'$)

SL3227

3GHz NPN TRANSISTOR ARRAYS

The SL3227 is a monolithic array of the five high frequency low current NPN transistors in a 16 lead DIL package. The transistors exhibit typical f_T of 3GHz and wideband noise figures of 2dB. The SL3227 is pin compatible with the CA3127 and SL3127.

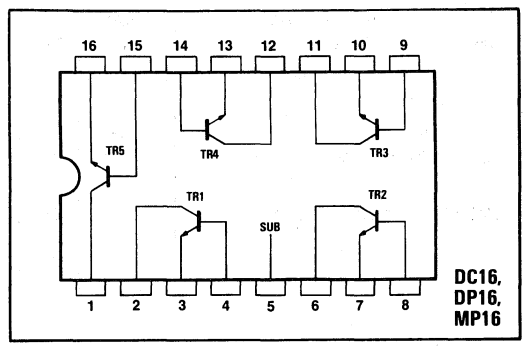


Fig.1 Pin connections - SL3227

FEATURES

- f_T Typically 3GHz
- Wideband Noise Figure 2.0dB
- V_{BE} Matching better than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

All Electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 10V
V_{EB} = 2.5V
V_{CE} = 6V
V_{CI} = 15V
I_C = 20mA
Maximum individual transistor dissipation 200mW
Storage temperature -55° C to +150° C
Max. junction temperature +150° C

Package thermal resistance (° C/watt)

Package Type	DC16	DP16	MP16
Chip to Case	40		
Chip to Ambient	120	180	200

NOTE: If all the power is being dissipated in one transistor these thermal resistance figures should be increased by 100° C/watt.

ORDERING INFORMATION

SL3227 NA DC
SL3227 NA DP
SL3227 NA MP

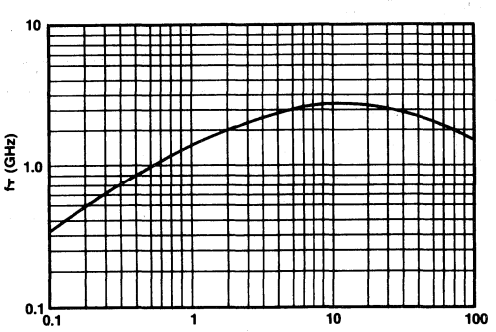


Fig.2 Transition frequency (f_T) v. collector current (V_{CB} = 2V, f = 200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 22°C \pm 2°C$

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	10	20		V	$I_C = 10\mu A$
Collector isolation breakdown	BV_{CIO}	16	40		V	$I_C = 10\mu A$
Base emitter breakdown	BV_{EBO}	2.5	5.0		V	$I_E = 10\mu A$
Collector emitter breakdown	LV_{CEO}	6	9		V	$I_C = 5mA$
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.22	0.5	V	$I_C = 10mA$, $I_B = 1mA$
Base emitter voltage	V_{BE}	0.73	0.78	0.81	V	$V_{CE} = 2V$, $I_C = 1mA$
Base emitter voltage difference all transistors	ΔV_{BE}		0.45	5.0	mV	$V_{CE} = 2V$, $I_C = 1mA$
Input offset current	ΔI_B		0.2	3	μA	$V_{CE} = 2V$, $I_C = 1mA$
Temperature coefficient of V_{BE}	$\frac{\Delta V_{BE}}{T}$		-1.69		mV/°C	$V_{CE} = 2V$, $I_C = 1mA$
Static forward current ratio	H_{fe}	35	80			$V_{CE} = 2V$, $I_C = 5mA$
		35	95			$V_{CE} = 2V$, $I_C = 0.1mA$
		40	85			$V_{CE} = 2V$, $I_C = 1mA$
Emitter base leakage	I_{EBO}		15		nA	$V_{EB} = 2V$
Collector base leakage	I_{CBO}		5		pA	$V_{CB} = 10V$
Collector isolation leakage	I_{CIO}		5		pA	$V_{CI} = 16V$
Emitter base capacitance	C_{EB}		0.7		pF	$V_{EB} = 0V$
Collector base capacitance	C_{CB}		0.4		pF	$V_{CI} = 0V$
Collector isolation capacitance	C_{CI}		1.5	2.0	pF	$V_{CI} = 0V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Transition frequency	f_T		3		GHz	$V_{CE} = 2V$, $I_C = 5mA$
Wideband noise figure	NF		2.0		dB	f = 60MHz $V_{CC} = 6V$
Knee of NF noise curve			1		kHz	$I_C = 1mA$
						$R_S = 1k\Omega$

SL3245

3GHz NPN TRANSISTOR ARRAY

The SL3245 is a monolithic array of five high frequency low current NPN transistors. The SL3245 consists of 3 isolated transistors and a differential pair in a 14 lead DIL package. The transistors exhibit typical f_T of 3GHz and wideband noise figures of 2dB. The device is pin compatible with the SL3045C and SL3145.

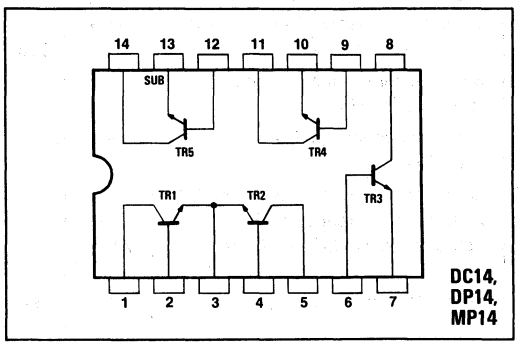


Fig.1 Pin connections - SL3245

FEATURES

- f_T Typically 3GHz
- Wideband Noise Figure 2.0dB
- V_{BE} Matching better than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

All Electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 10V
V_{EB} = 2.5V
V_{CE} = 6V
V_{CI} = 15V
I_C = 20mA
Maximum individual transistor dissipation 200mW
Storage temperature -55°C to +150°C
Max. junction temperature +150°C
Package thermal resistance (°C/watt)

Package Type	DC14	DP14	MP14
Chip to Case	40		
Chip to Ambient	120	180	200

NOTE: If all the power is being dissipated in one transistor these thermal resistance figures should be increased by 100°C/watt.

ORDERING INFORMATION

SL3245 NA DC
SL3245 NA DP
SL3245 NA MP

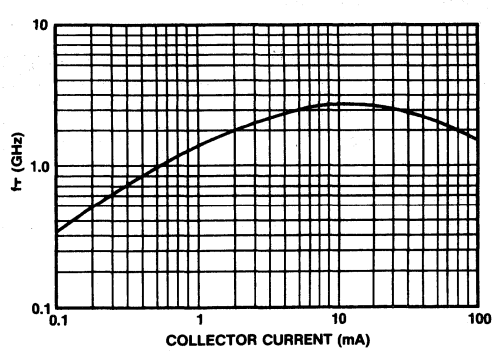


Fig.2 Transition frequency (f_T) v. collector current (V_{CB} = 2V, f = 200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	10	20		V	I_C = 10μA
Collector isolation breakdown	BV_{CIO}	16	40		V	I_C = 10μA
Base emitter breakdown	BV_{EBO}	2.5	5.0		V	I_E = 10μA
Collector emitter breakdown	LV_{CEO}	6	9		V	I_C = 5mA
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.22	0.5	V	I_C = 10mA, I_B = 1mA
Base emitter voltage	V_{BE}	0.73	0.78	0.81	V	V_{CE} = 2V, I_C = 1mA
Base emitter voltage difference (except TR1, TR2)	ΔV_{BE}		0.45	5.0	mV	V_{CE} = 2V, I_C = 1mA
Base emitter voltage difference TR1, TR2	ΔV_{BE}		0.33	5.0	mV	V_{CE} = 2V, I_C = 1mA
Input offset current (except TR1,TR2)	ΔI_B		0.2	3	μA	V_{CE} = 2V, I_C = 1mA
Input offset current TR1,TR2	ΔI_B		0.2	2	μA	V_{CE} = 2V, I_C = 1mA
Temperature coefficient of V_{BE}	$\frac{\Delta V_{BE}}{T}$		-1.69		mV/°C	V_{CE} = 2V, I_C = 1mA
Static forward current ratio	H_{fe}	35	80			V_{CE} = 2V, I_C = 5mA
		35	90			V_{CE} = 2V, I_C = 0.1mA
		40	85			V_{CE} = 2V, I_C = 1mA
Emitter base leakage	I_{EBO}		10		nA	V_{EB} = 2V
Collector base leakage	I_{CBO}		5		pA	V_{CB} = 10V
Collector isolation leakage (TR1-TR4)	I_{CIO}		10		pA	V_{CI} = 16V
Collector isolation leakage (TR5)	I_{CIO}		10		pA	V_{CI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance	C_{CB}		0.4		pF	V_{CI} = 0V
Collector isolation capacitance	C_{CI}		1.4	2.0	pF	V_{CI} = 0V

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Transition frequency	f_T		3		GHz	V_{CE} = 2V, I_C = 5mA
Wideband noise figure	NF		2.0		dB	f = 60MHz V_{CC} = 6V I_C = 1mA
Knee of NF noise curve			1		kHz	R_S = 1kΩ

SL610, SL611 & SL612

RF/IF AMPLIFIERS

The SL1610C, SL1611C and SL1612C are RF voltage amplifiers with AGC facilities. The voltage gains are 10, 20 and 50 times respectively and the upper frequency response varies from 15MHz to 120MHz according to type.

FEATURES

- Wide AGC Range: 50dB
- Easy Interfacing
- Integral Power Supply RF Decoupling

APPLICATIONS

- RF Amplifiers
- IF Amplifiers

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Voltage Gain: 20dB to 34dB

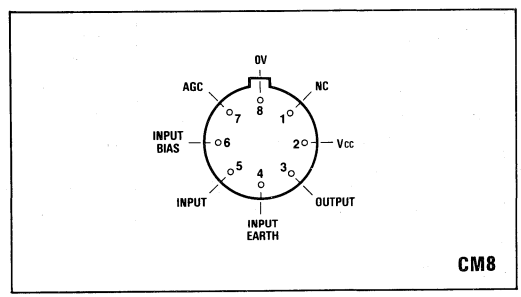


Fig. 1 Pin connections (bottom view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

ORDERING INFORMATION

SL610/1/2 C CM
SL610/1/2 CB CM

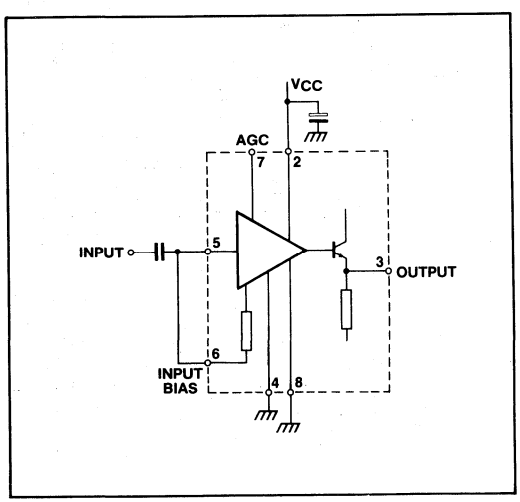


Fig. 2 Block diagram

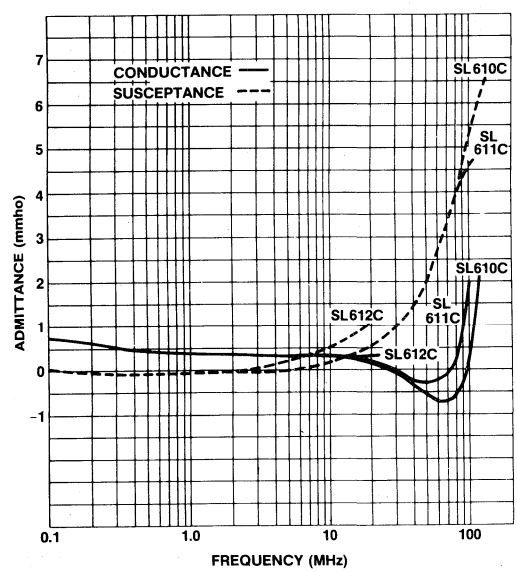


Fig. 3 Input admittance with o/c output (G_{11})

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C
Test frequency: SL610C 30MHz
SL611C 30MHz
SL612C 1.75MHz

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL610C		15	20	mA	
	SL611C		15	20	mA	No signal, pin 3 open circuit
	SL612C		3.3	5	mA	
Voltage gain	SL610C	18	20	22	dB	R_S = 50Ω
	SL611C	24	26	28	dB	RL = 22°C
	SL612C	32	34	36	dB	T_{amb} = 22°C
Cut-off frequency (-3dB)	SL610C	85	120		MHz	
	SL611C	50	80		MHz	
	SL612C	10	15		MHz	
Max.output signal (max.AGC)			1.0		V rms	RL = 150Ω (SL610C/611C)
						RL = 1.2kΩ (SL612C)
Max.input signal (max.AGC)			250		mV rms	
AGC range	SL610C	40	50		dB	
	SL611C	40	50		dB	Pin 7 0V to 5.1V
	SL612C	60	70		dB	
AGC current			0.15	0.6	mA	Current into pin 7 at 5.1V

APPLICATION NOTES

Input circuit

The SL610C, SL611C and SL612C are normally used with pins 5 and 6 connected together and with the input connected via a capacitor as shown in Fig. 2.

The input impedance is negative between 30MHz and 100MHz (SL610C, SL611C only) and is shown in Fig. 3. If the source is inductive it should be shunted by a 1kΩ resistor to prevent oscillation.

An alternative input circuit with improved noise figure is shown in Fig. 4.

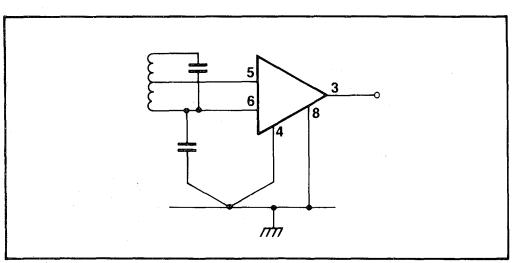


Fig. 4 Alternative input circuit

Output circuit

The output stage is an emitter follower and has a negative output impedance at certain frequencies as shown in Fig. 5.

To prevent oscillation when the load is capacitive a 47Ω resistor should be connected in series with the output.

AGC

When pin 7 is open circuit or connected to a voltage less than 2V the voltage gain is normal. As the AGC voltage is increased there is a reduction in gain as shown in Fig.6. This reduction varies with temperature.

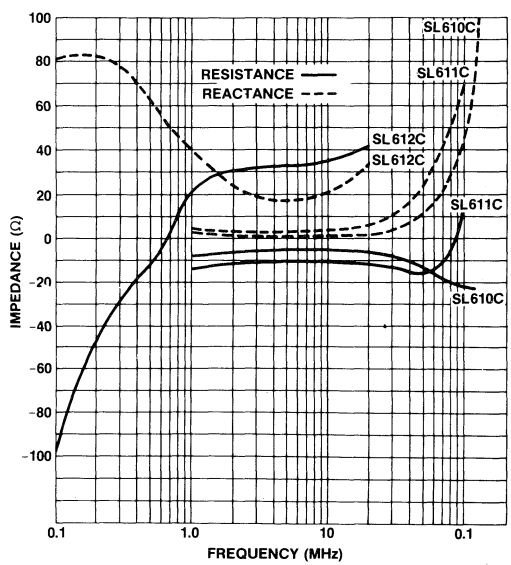


Fig. 5 Typical output impedance with s/c input (G22)

Typical applications

The circuit of Fig. 7 is a general purpose RF preamplifier. The voltage gain (from pin 5 to pin 3) is shown in Fig. 8. Fig. 9 is the IF section of a simple SSB transceiver. At 9MHz it has a gain of 100dB.

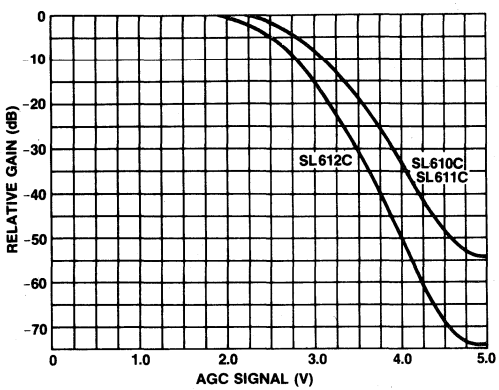


Fig. 6 AGC characteristics (typical)

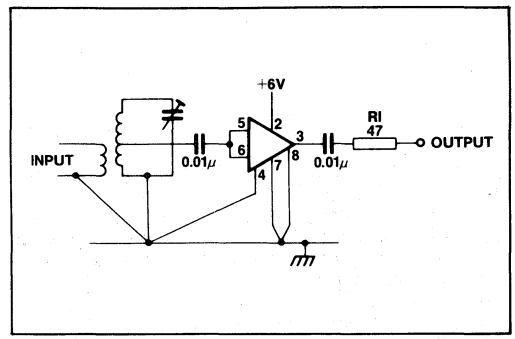


Fig. 7 RF preamplifier

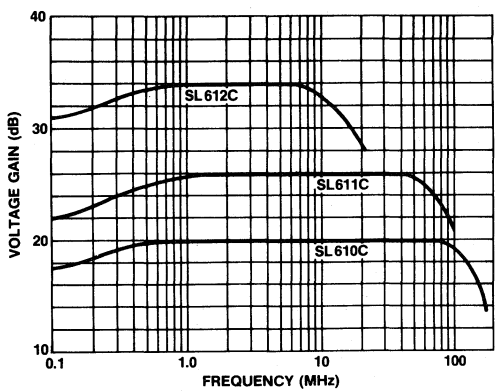


Fig. 8 Typical voltage gain (R_S=50 Ω)

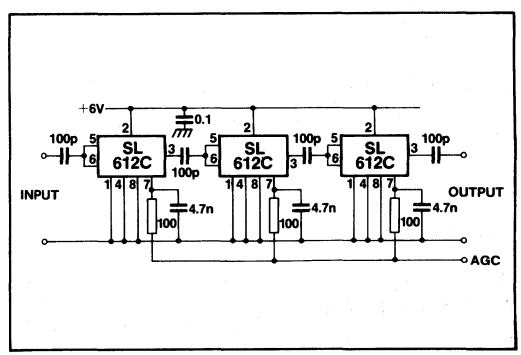


Fig. 9 IF amplifier using SL612

SL621

AGC GENERATOR

The SL621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL610C, SL611C and SL612C RF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL610C and one SL612C amplifier and a suitable detector, the SL621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

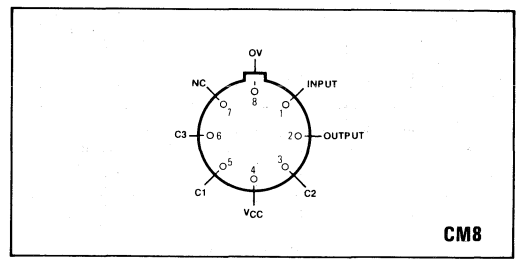


Fig. 1 Pin connections (bottom view)

FEATURES

- All Time Constants Set Externally
- Easy Interfacing
- Compatible with SL610/611/612

APPLICATIONS

- SSB Receivers
- Test Equipment

QUICK REFERENCE DATA

- Supply voltage: 6V
- Supply current: 3mA

ORDERING INFORMATION

SL621 C CM
SL621 CB CM

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

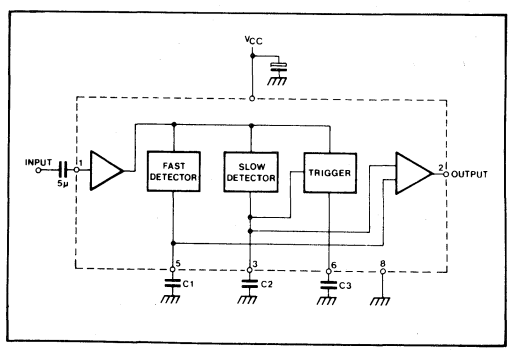


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 6V
Ambient temperature: −30°C to +85°C
Test frequency: 1kHz
Test circuit as Fig. 2

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.1	4.3	mA	No signal
Cut-off frequency (−3dB)		6		kHz	
Input for 2.2V DC output	3	7	11	mVrms	
Input for 4.6V DC output	9	11	16	mVrms	
Maximum output voltage	5.1			V	
AC ripple on output		12	20	mV pk-pk	1kHz, output open circuit
Input resistance	350	500	700	Ω	
Output resistance		70	230	Ω	
'Fast' rise time t_1		20	55	ms	0 to 50% full output
'Fast' decay time t_2	150	200	330	ms	100% to 36% full output
'Slow' rise time t_3	150	200	300	ms	Time to output transistion point
Hold collapse time t_4	65	100	150	ms	90% to 10% full output
Hold time t_5	0.75	1.0	1.25	s	

APPLICATION NOTES

The SL621C consists of an input AF amplifier coupled to a DC output amplifier by means of two detectors having short and long rise and fall times respectively. The time constants of these detectors are set externally by capacitors on pins 5 (C_1) and 3 (C_2).

The detected audio signal at the input will rapidly establish an AGC level via the 'fast' detector time in t_1 (see Fig. 3). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is more sensitive.

Input signals greater than approximately 4mV rms will actuate a trigger circuit whose output pulses provide a discharge current for C_2.

By this means the voltage on C_2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C_2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C_3. When the trigger pulses cease, C_3 discharges and after t_5 C_2 is discharged rapidly (in time t_4) and so full receiver gain is restored. The hold time, t_5 is approximately one second with C_3 = 100µF.

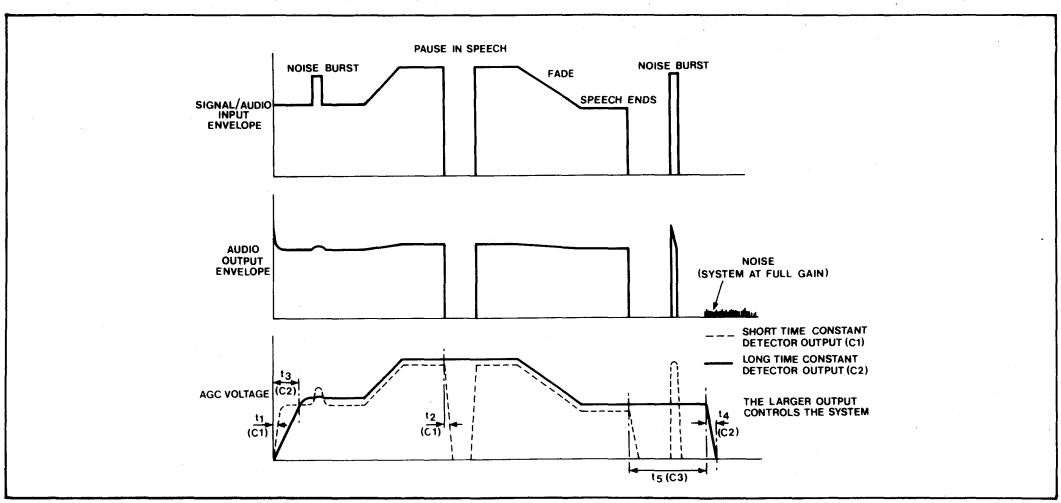


Fig. 3 Dynamic response of a system controlled by SL621C AGC generator

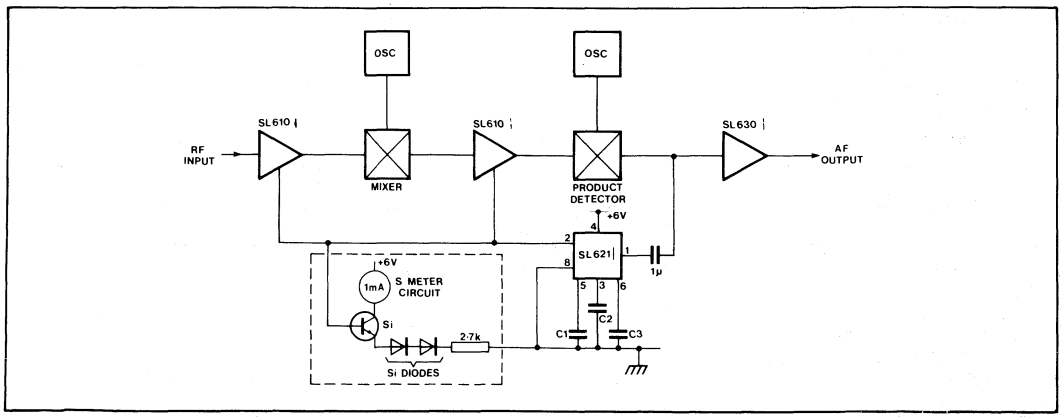


Fig. 4 SL621C used to control SSB receiver

If signals reappear during t_5, then C_3 will recharge and normal operation will continue. The C_3 recharge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 3 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

The various time constants quoted are for $C_1 = 50\mu F$ and $C_2 = C_3 = 100\mu F$. These time constants may be altered by varying the appropriate capacitors. C_1 controls t_1, t_2; C_2 controls t_3, t_4; C_3 controls t_5.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least $500\mu F$ so that it is not affected by the current surge resulting from a sudden input on pin 1.

In a receiver for both AM and SSB using an SL623C detector/carrier AGC generator, the AGC outputs of the SL621C and SL623C may be connected together provided that no audio reaches the SL621C input while the SL623C is controlling the system.

AGC lines may require some RF decoupling but the total capacitance on the output should not exceed 15000pF or the impulse suppression will suffer.

Under some conditions,overload of the AGC output may occur in a receiver. Possible solutions are shown in Figs.6 and 7.

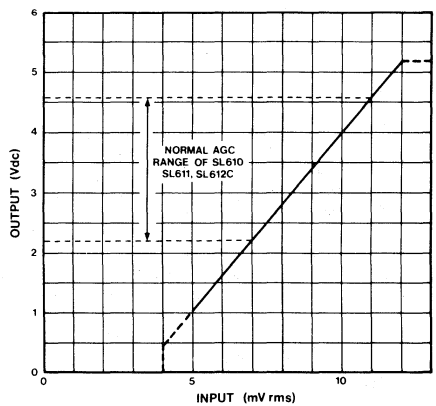


Fig. 5 Transfer characteristic of SL621C (typical)

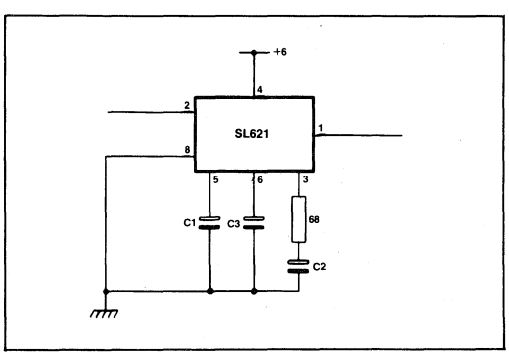


Fig.6

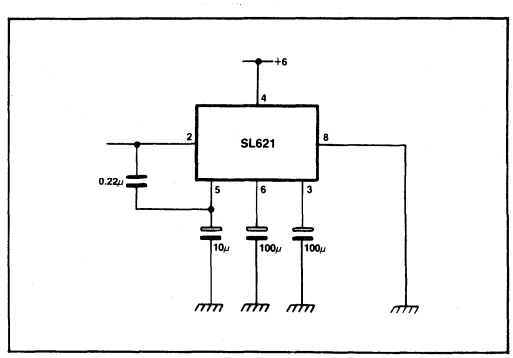


Fig.7

SL623

AM DETECTOR, AGC AMPLIFIER & SSB DEMODULATOR

The SL623C is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator with SSB demodulator. It is designed specially for use in SSB/AM receivers in conjunction with SL610C, SL611C and SL612C RF and IF amplifiers. It is complementary to the SL621C SSB AGC generator.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL610C and one SL612C amplifier, the SL623C will maintain the output within a 5dB range for a 90dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100mV, contributes negligible distortion up to 90% modulation. The SSB demodulator is of single balanced form. The SL623C is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies.

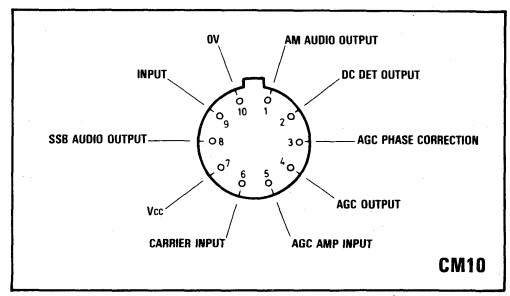


Fig. 1 Pin connections (bottom view)

FEATURES

- Negligible Distortion
- Easy Interfacing
- Fast Response Time

APPLICATIONS

- AM SSB Receivers
- Test Equipment

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Maximum Frequency: 30MHz

ORDERING INFORMATION

SL623 C CM
SL623 CB CM

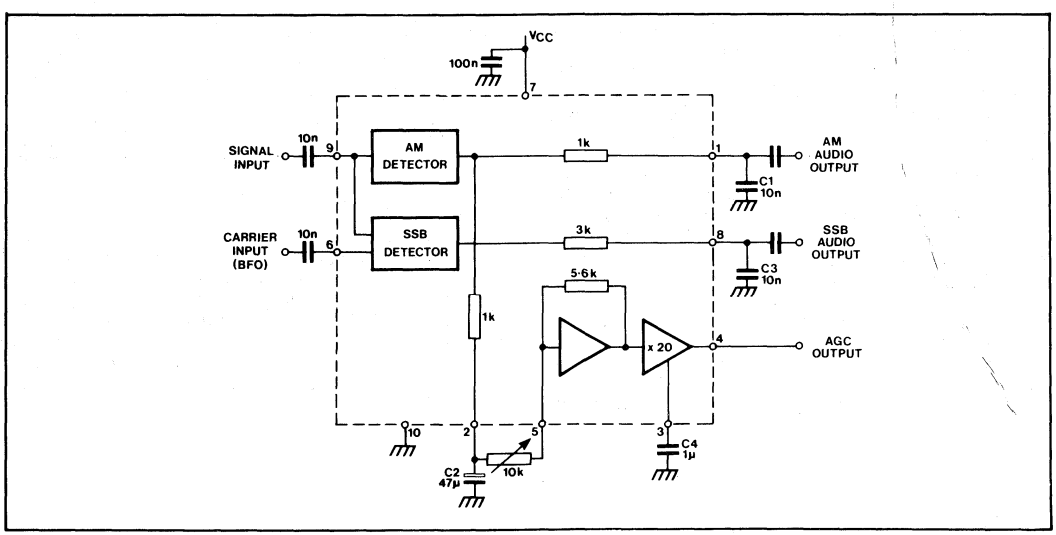


Fig. 2 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 6V |
Ambient temperature = −30°C to +85°C
Test circuit as Fig. 2

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		9	11	mA	No signal, Pin 4 open
Input impedance		800		Ω	Pins 6, 9
SSB audio output	22	30	47	mV rms	Signal input 20mV rms @ 1.748 MHz. Ref. signal input 100mV @ 1.750 MHz
AM audio output	43	55	67	mV rms	Signal input 125mV rms @ 1.75MHz modulated to 80% at 1kHz
AGC range (Note 1)			6	dB	Initial signal input 125mV rms at 1.75MHz modulated to 80% at 1kHz. Output set to 2.0V with 10kΩ potentiometer between Pins 2 & 5.

NOTES
1. The AGC range is the change in input level to increase AGC output voltage from 2.0V to 4.6V

APPLICATION NOTES

AGC Generator

Pin 3, the AGC amplifier phase correction point should be decoupled to ground by a 1 microfarad capacitor (C4), keeping leads as short as possible. The value of C4 is quite critical, and should not be altered: if it is increased the increased phase shift in the AGC loop may cause the receiver to become unstable at LF and if it is reduced the modulation level of the incoming signal will be reduced by fast-acting AGC.

The AGC output (Pin 4) will drive at least two SL610/11/12 amplifiers. The SL623AGC output is an emitter follower similar to that of the SL621C. Hence the outputs of the two devices may be connected in parallel when constructing AM/SSB systems.

Less signal is needed to drive the SSB demodulator than the AM detector. In a combined AM/SSB system, therefore, the signal will automatically produce an SSB AGC voltage via the SL621C as long as a carrier (BFO) is present at the input to the SSB demodulator of the SL623C. The AGC generator of the SL623 will not contribute in such a configuration.

For AM operation the BFO must be disconnected from the carrier input of the SSB demodulator. In the absence of an input signal, the SL621C will then return to its quiescent state. To switch over a receiver using the SL623C from SSB to AM operation it is therefore necessary to turn off the BFO and transfer the audio pick-off from the SSB to the AM detector.

Neglecting to disconnect the SSB carrier input during AM operation can result in heterodyning due to pick-up of carrier on the input signal. In some sets different filters are used for AM and SSB; these will also need to be switched.

The 10 kilohm gain-setting preset potentiometer is adjusted so that a DC output of 2 volts is achieved for an input of 125mV rms. There will then be full AGC output from the SL623C for a 4dB increase in input. A fixed resistor of 1.5 kilohms can often be used instead of the potentiometer.

SSB Demodulator

The carrier input is applied to Pin 6, via a low-leakage capacitor. It should have an amplitude of about 100mV rms and low second harmonic content to avoid disturbing the DC level at the detector output.

Pin 8 is the SSB output and should be decoupled at RF by a 0.01 microfarad capacitor. The output impedance of the detector is 3 kilohm and the terminal is at a potential of about +2V which may be used to bias an emitter follower if a lower output impedance is required. The input to the audio stage of a receiver using an SL623C should be switched between the AM and the SSB outputs — no attempt should be made to mix them. Since the SL621C is normally used in circumstances where low-level audio is obtained from the detector, the relatively high SSB audio output of the SL623C must be attenuated before being applied to the SL621C. This is most easily done by connecting the SL623C to the SL621C via a 2 kilohm resistor in series with a 0.5 microfarad capacitor.

Input Conditions

The input impedance is about 800 ohms in parallel with 5pF. Connection must be made to the input via a capacitor to preserve the DC bias. An input of about 125mV rms is required for satisfactory carrier AGC performance and 20mV rms for SSB detection. Normally, the AGC will cope with this variation but in an extreme case a receiver using an SL623C and having the same gain to the detector in both AM and SSB modes will be some 10dB less sensitive to AM.

SL640 & SL641

DOUBLE BALANCED MODULATORS

The SL640C and SL641C are double balanced modulators intended for use in radio systems at frequencies up to 75MHz. The SL640 has an integral output load resistor (Pin 5) together with an emitter follower output (Pin 6) whereas the SL641 has a single output designed as a current drive to a tuned circuit.

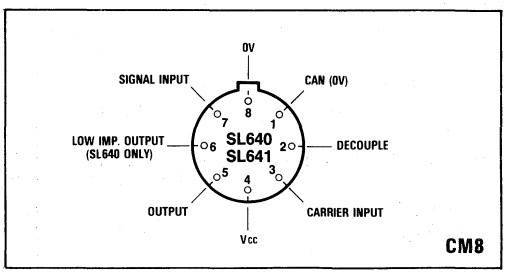


Fig. 1 Pin connections (bottom view)

FEATURES

- No External Bias Networks Needed
- Easy Interfacing
- Choice of Voltage or Current Outputs

APPLICATIONS

- Mixers In Radio Transceivers
- Phase Comparators
- Modulators

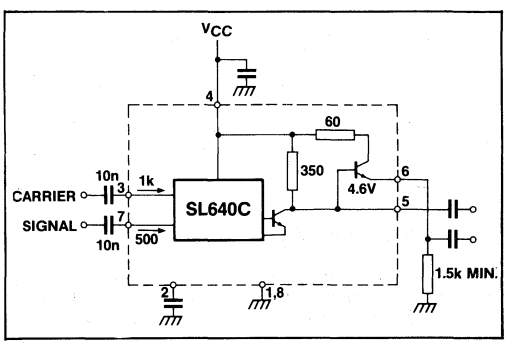


Fig. 2 Block diagram (SL640C)

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Conversion Gain: 0dB
- Maximum Inputs: 200mV rms

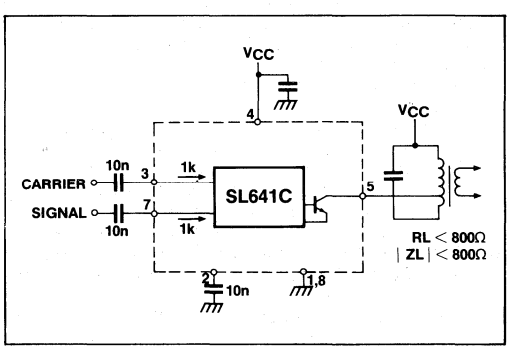


Fig. 3 Block diagram (SL641C)

ABSOLUTE MAXIMUM RATINGS

Supply voltage 9V
Storage temperature: −55°C to +125°C

ORDERING INFORMATION

SL640/1 C CM

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL640C		12	17	mA	
	SL641C		10	13	mA	
Conversion gain	SL640C	−3	0	+3	dB	
Conversion transconductance	SL641C	1.75	2.5	3.5	mmho	
Noise figure			10		dB	
Carrier input impedance			1		kΩ	
Signal input impedance	SL640C		500		Ω	
	SL641C		1		kΩ	
Maximum input voltage	SL640C		210		mV rms	
	SL641C		250		mV rms	
Signal leak	SL640C		−30	−18	dB	Signal: 70mV rms, 1.75MHz Carrier: 100mV rms, 28.25 MHz Output: 30MHz
Carrier leak	SL640C		−30	−20	dB	
Signal leak	SL641C		−18	−12	dB	Signal: 70mV rms, 30MHz Carrier: 100mV rms, 28.25 MHz Output: 1.75MHz
Carrier leak	SL641C		−25	−12	dB	
Intermodulation products	SL640C		−45	−35	dB	Signal1: 42.5mV rms, 1.75MHz Signal2: 42.5mV rms, 2MHz Carrier: 100mV rms, 28.25MHz Output: 29.75MHz
	SL641C		−45	−30	dB	Signal1: 42.5mV rms, 30MHz Signal2: 42.5mV rms, 31MHz Carrier:100mV rms, 28.25MHz Output: 3.75MHz

APPLICATION NOTES

The SL640C and SL641C require input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see Electrical Characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance. Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at Pin 2 would give rise to poor rejection figures and to distortion.

The output of the SL641C is an open collector. If both sidebands are developed across the load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course increases the gain of the circuit.

There are two outputs from the SL640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output. The output on pin 6 requires a discrete load resistor of not less than 1500 ohms to ground. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

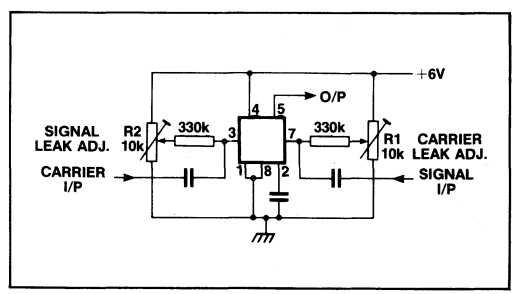


Fig. 4 Signal and carrier leak adjustment

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig.4. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

SL1611 IS FOR MAINTENANCE PURPOSES ONLY AND IS NOT RECOMMENDED FOR NEW DESIGNS

SL1610, SL1611, SL1612

RF/IF AMPLIFIERS

The SL1610C, SL1611C and SL1612C are RF voltage amplifiers with AGC facilities. The voltage gains are 10, 20 and 50 times respectively and the upper frequency response varies from 15 MHz to 120|MHz according to type.

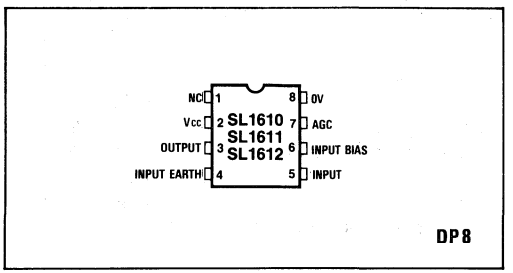


Fig. 1 Pin connections (top view)

FEATURES

- Wide AGC Range: 50dB
- Easy Interfacing
- Integral Power Supply RF Decoupling

APPLICATIONS

- RF Amplifiers
- IF Amplifiers

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Voltage Gain: 20dB to 34dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to|+|125°C

ORDERING INFORMATION

SL1610/1/2 C DP

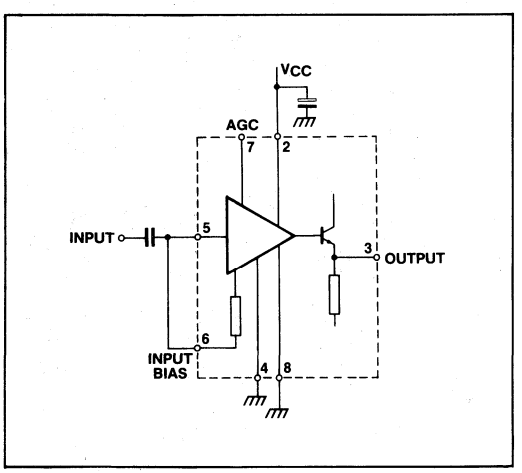


Fig. 2 Block diagram

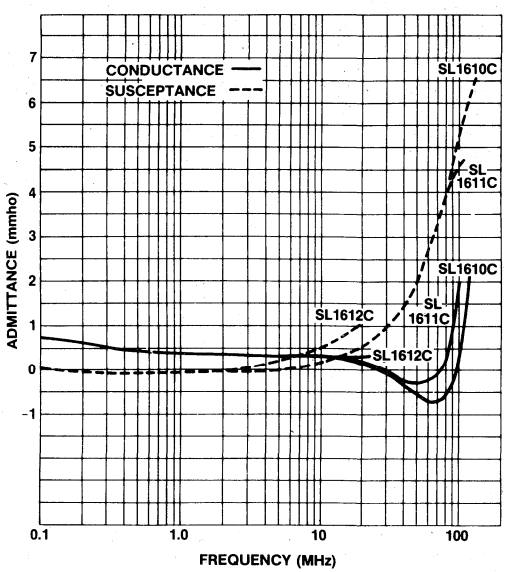


Fig. 3 Input admittance with o/c output (G_{11})

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C
Test frequency: SL1610C 30MHz
SL1611C 30MHz
SL1612C 1.75MHz

Characteristics	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL1610C		15	24	mA	
	SL1611C		15	24	mA	No signal, pin 3 open circuit
	SL1612C		3.3	6	mA	
Voltage gain	SL1610C	17	20	24	dB	R_S = 50Ω
	SL1611C	23	26	30	dB	RL = 500Ω
	SL1612C	31	34	38	dB	T_{amb} = 22°C
Cut-off frequency (-3dB)	SL1610C		120		MHz	
	SL1611C		80		MHz	
	SL1612C		15		MHz	
Max.output signal (max.AGC)			1.0		V rms	RL = 150Ω (SL1610C/1611C)
						RL = 1.2kΩ (SL1612C)
Max.input signal (max.AGC)			250		mV rms	
AGC range	SL1610C	40	50		dB	
	SL1611C	40	50		dB	Pin 7 0V to 5.1V
	SL1612C	60	70		dB	
AGC current			0.15	0.6	mA	Current into pin 7 at 5.1V

APPLICATION NOTES

Input circuit

The SL1610C, SL1611C and SL1612C are normally used with pins 5 and 6 connected together and with the input connected via a capacitor as shown in Fig. 2.

The input impedance is negative between 30MHz and 100MHz (SL1610C, SL1611C only) and is shown in Fig. 3. the source is inductive it should be shunted by a 1kΩ resistor to prevent oscillation.

An alternative input circuit with improved noise figure is shown in Fig. 4.

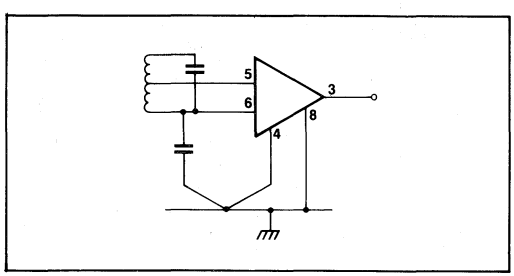


Fig. 4 Alternative input circuit

Output circuit

The output stage is an emitter follower and has a negative output impedance at certain frequencies as shown in Fig. 5.

To prevent oscillation when the load is capacitive a 47Ω resistor should be connected in series with the output.

AGC

When pin 7 is open circuit or connected to a voltage less than 2V the voltage gain is normal. As the AGC voltage is increased there is a reduction in gain as shown in Fig.6. This reduction varies with temperature.

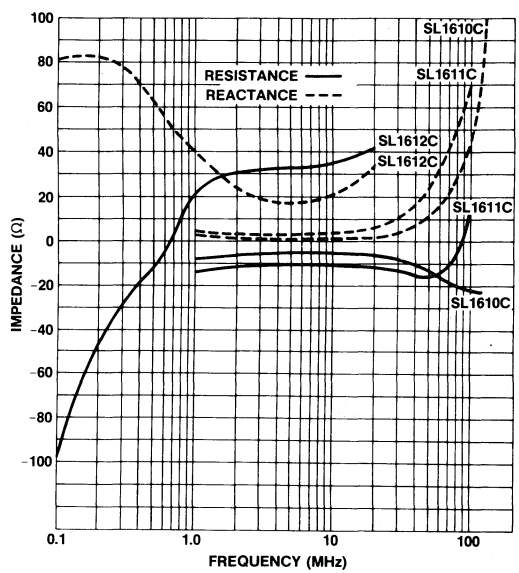


Fig. 5 Typical output impedance with s/c input (G22)

Typical applications

The circuit of Fig. 7 is a general purpose RF preamplifier. The voltage gain (from pin 5 to pin 3) is shown in Fig. 8. Fig. 9 is the IF section of a simple SSB transceiver. At 9MHz it has a gain of 100dB.

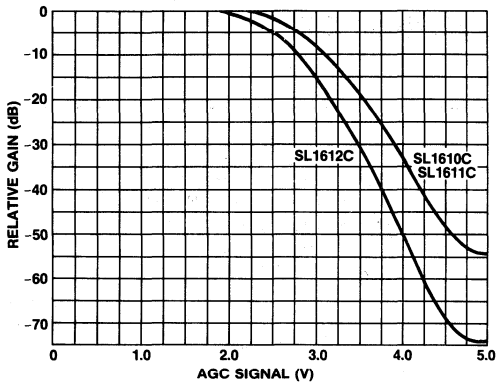


Fig. 6 AGC characteristics (typical)

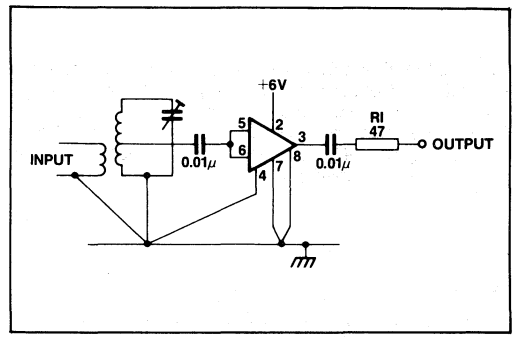


Fig. 7 RF preamplifier

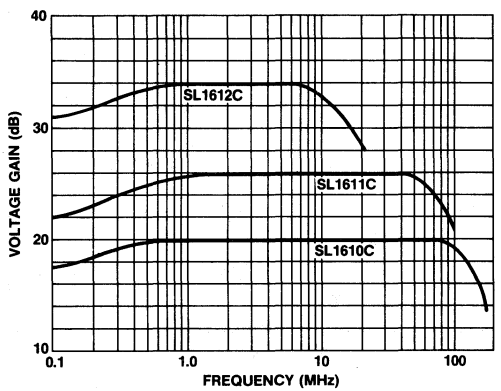


Fig. 8 Typical voltage gain (R_S=50Ω)

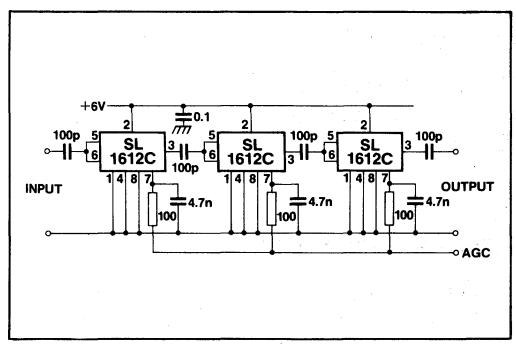


Fig. 9 IF amplifier using SL1612

SL1640C IS FOR MAINTENANCE PURPOSES ONLY AND IS NOT RECOMMENDED FOR NEW DESIGNS

SL1640 & SL1641

DOUBLE BALANCED MODULATORS

The SL1640C and SL1641C are double balanced modulators intended for use in radio systems at frequencies up to 75MHz. The SL1640 has an integral output load resistor (Pin 5) together with an emitter follower output (Pin 6) whereas the SL1641 has a single output designed as a current drive to a tuned circuit.

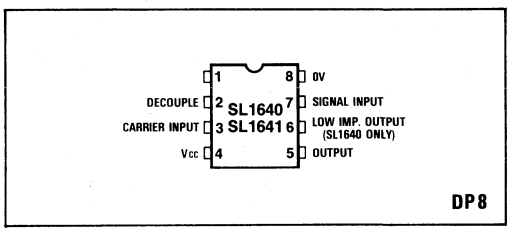


Fig. 1 Pin connections (top view)

FEATURES

- No External Bias Networks Needed
- Easy Interfacing
- Choice of Voltage or Current Outputs

APPLICATIONS

- Mixers In Radio Transceivers
- Phase Comparators
- Modulators

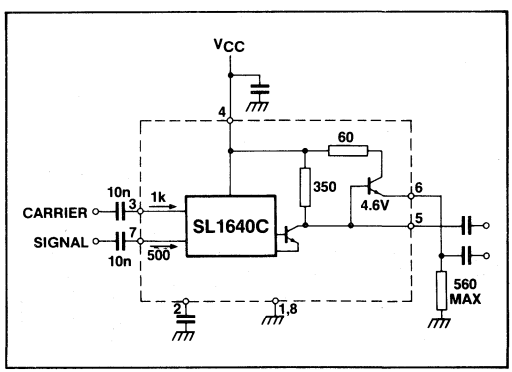


Fig. 2 Block diagram (SL1640C)

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Conversion Gain: 0dB
- Maximum Inputs: 200mV rms

ABSOLUTE MAXIMUM RATINGS

Supply voltage 9V
Storage temperature: −55°C to +125°C

ORDERING INFORMATION

SL1640/1 C DP

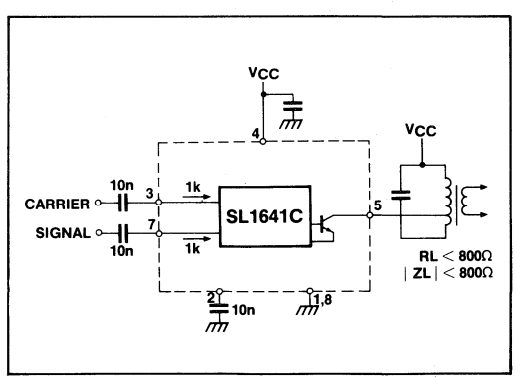


Fig. 3 Block diagram (SL1641C)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL1640C		12	18	mA	
	SL1641C		10	15	mA	
Conversion gain	SL1640C	−3	0	+3	dB	
Conversion transconductance	SL1641C	1.7	2.5	3.5	mmho	
Noise figure			10		dB	
Carrier input impedance			1		kΩ	
Signal input impedance	SL1640C		500		Ω	
	SL1641C		1		kΩ	
Maximum input voltage	SL1640C		210		mV rms	
	SL1641C		250		mV rms	
Signal leak	SL1640C		−30		dB	Signal: 70mV rms, 1.75MHz Carrier: 100mV rms, 28.25 MHz Output: 30MHz
Carrier leak	SL1640C		−30		dB	
Signal leak	SL1641C		−18		dB	Signal: 70mV rms, 30MHz Carrier: 100mV rms, 28.25 MHz Output: 1.75MHz
Carrier leak	SL1641C		−25		dB	
Intermodulation products	SL1640C		−45		dB	Signal1: 42.5mV rms, 1.75MHz Signal2: 42.5mV rms, 2MHz Carrier: 100mV rms, 28.25MHz Output: 29.75MHz
	SL1641C		−45		dB	Signal1: 42.5mV rms, 30MHz Signal2: 42.5mV rms, 31MHz Carrier:100mV rms, 28.25MHz Output: 2.75MHz

APPLICATION NOTES

The SL1640C and SL1641C require input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see Electrical Characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance. Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at Pin 2 would give rise to poor rejection figures and to distortion.

The output of the SL1641C is an open collector. If both sidebands are developed across the load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course increases the gain of the circuit.

There are two outputs from the SL1640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output. The output on pin 6 requires a discrete load resistor of not less than 1500 ohms to ground. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

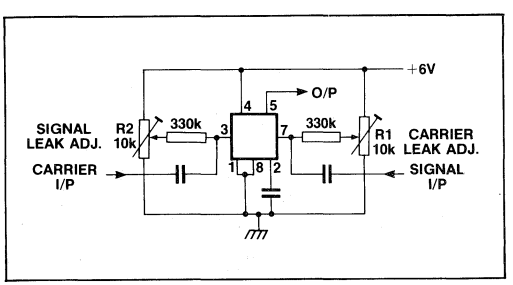


Fig. 4 Signal and carrier leak adjustment

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig.4. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

SL6140

400MHz WIDEBAND AGC AMPLIFIER

(Supersedes edition in September 1988 Linear IC Handbook)

The SL6140 is an integrated broadband AGC amplfier, designed on an advanced 3-micron all implanted bipolar process. The amplifier provides over 15dB of linear gain into 50Ω at 400MHz.

Accurate gain control is also provided with over 70dB of dynamic range.

The SL6140 provides over 45dB of voltage gain with an R_L of 1kΩ.

FEATURES

- 400MHz Bandwidth (R_L = 50Ω)
- High Voltage Gain 45dB (R_L = 1kΩ)
- 70dB Gain Control Range
- High Output Level at Low Gain
- Accurate Gain Control
- Full Military Temperature Range (CM only)
- MC1590 Replacement with Improved Performance

APPLICATIONS

- RF/IF Amplifier
- High Gain Mixers
- Video Amplifiers

ORDERING INFORMATION

SL6140 NA MP **SL6140 B CM**
SL6140 A CM **SL6140AC CM**

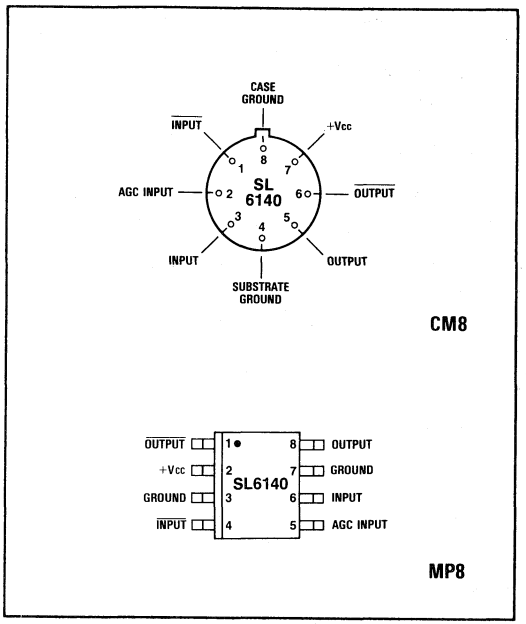


Fig.1 Pin connections (top view)

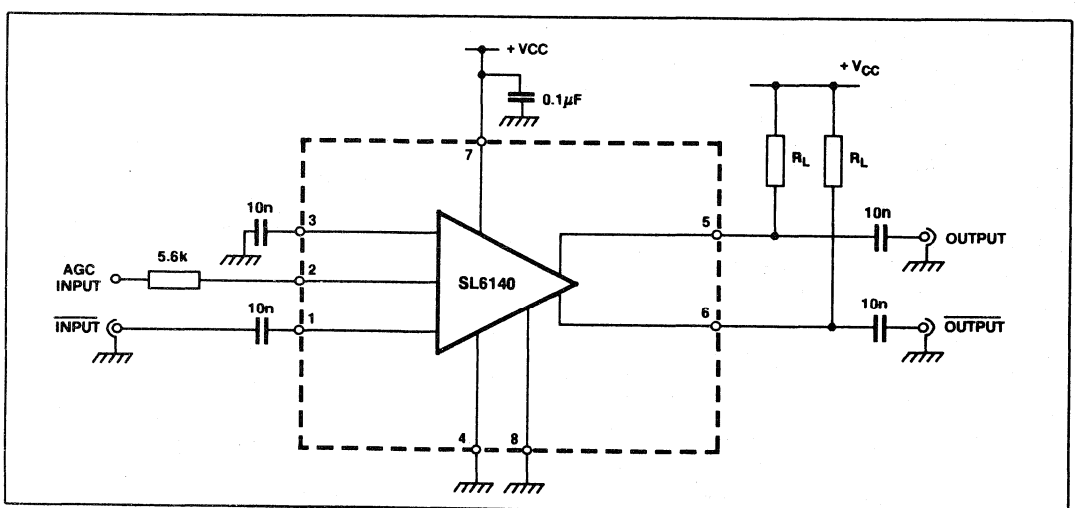


Fig.2 Typical wideband application (CM pinout)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 25°C$, $V_{CC} = +12V$

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	5,6,7	-	19	23	mA	
Output stage current	5,6 (sum)	5	7	9	mA	
Output current matching (magnitude of difference of output currents)	5,6	-	0.5	-	mA	
AGC range	2	60	75	-	dB	See Fig. 4 & Note 1
Voltage gain (single ended)	5,6	40	45	-	dB	$R_L = 1k\Omega$ See Fig.5 & Note 1
			55		dB	Tuned input and output
	5,6	-	15	-	dB	$R_L = 50\Omega$
Bandwidth (-3dB)	5,6	-	25	-	MHz	$R_L = 1k\Omega$ See Fig. 5
			400		MHz	$R_L = 50\Omega$
Maximum output level (single ended)						
0dB AGC	5,6	2.5	3.5	-	V p-p	Note 1
-30dB AGC	5,6	2.5	3.5	-	V p-p	$R_L = 1k\Omega$, Note 1

NOTE 1. Guaranteed but not tested for MP package

DESCRIPTION

The SL6140 (Fig.3) is a high gain amplifier with an AGC control capable of reducing the gain of the amplifier by over 70dB. The gain is adjustable by applying a voltage to the AGC input via an external resistor (R_{AGC}), the value of which adjusts the curve of gain reduction versus control voltage (see Fig. 4) As the output stage of the amplifier is an open collector the maximum voltage gain is determined by R_L. With load resistance of 1kΩ the single ended voltage gain is 45dB and with a load resistance of 50Ω the voltage gain is 15dB ($20\log_{10} V_{OUT}/V_{IN}$). Another parameter that depends on the load resistance is the bandwidth: 25MHz for $R_L = 1k\Omega$, as compared with 400MHz for $R_L = 50\Omega$. R_L is chosen to give either the required bandwidth or voltage gain for the circuit.

Fig. 7 shows the input impedance of the device. Accurate impedance matching to both inputs and outputs of this device (by resonant circuit or other means) can raise the gain to 55dB but for most circumstances a 50Ω source impedance is adequate.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+18V
Input voltage (differential)	+5V
AGC Supply	V_{CC}
Storage temperature	-55°C to +150°C
Operating temperature	
SL6140 MP	0°C to 70°C
SL6140 B CM	-40°C to +85°C
SL6140 A CM	-55°C to +125°C
Chip operating temperature	
SL6140 MP	+175°C
SL6140 (CM variants)	+150°C

THERMAL RESISTANCE

Chip-to-ambient	
SL6140 MP	225°C/W
SL6140 (CM variants)	163°C/W
Chip-to-case	
SL6140 MP	65°C/W
SL6140 (CM variants)	57°C/W

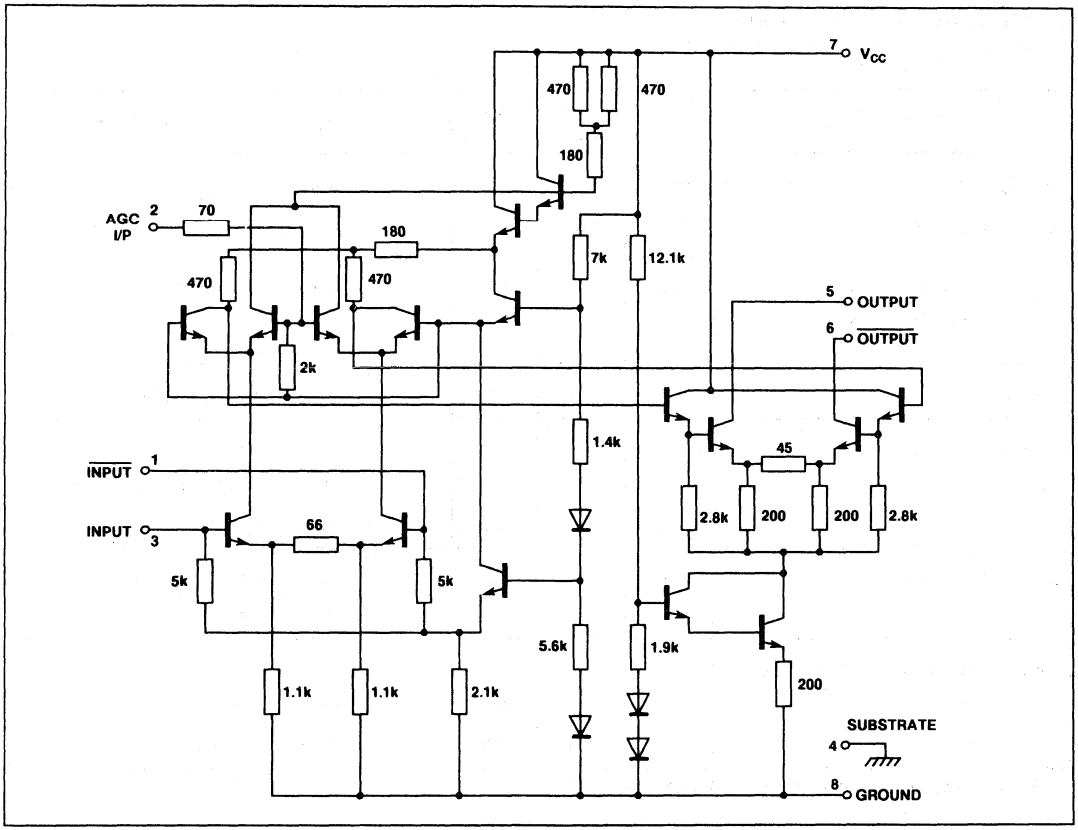


Fig. 3 - Full circuit diagram of SL6140 (CM pinout)

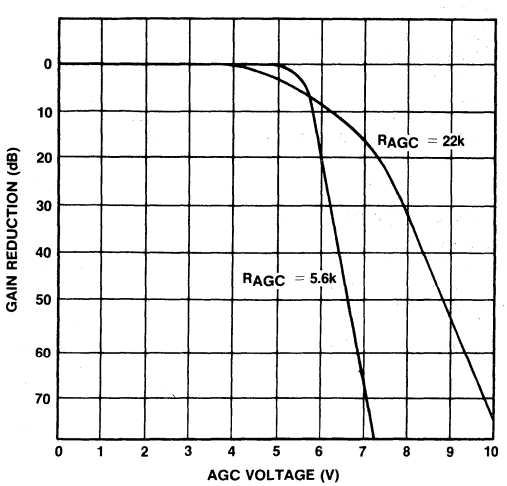


Fig.4 Gain reduction v. AGC voltage

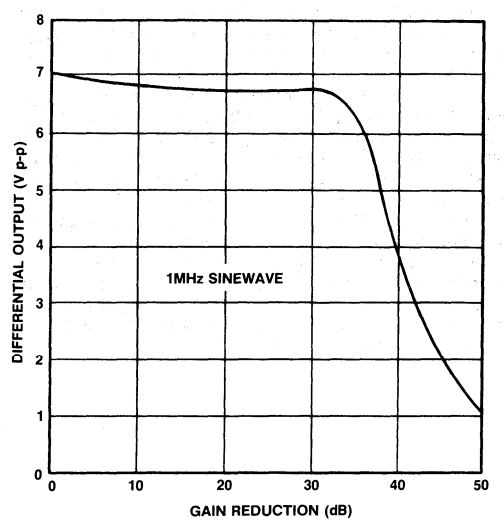


Fig.5 Voltage gain v. frequency

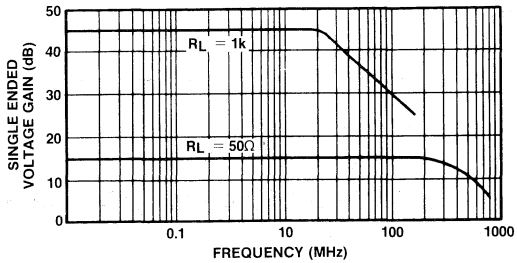


Fig.6 Maximum differential output v. gain reduction

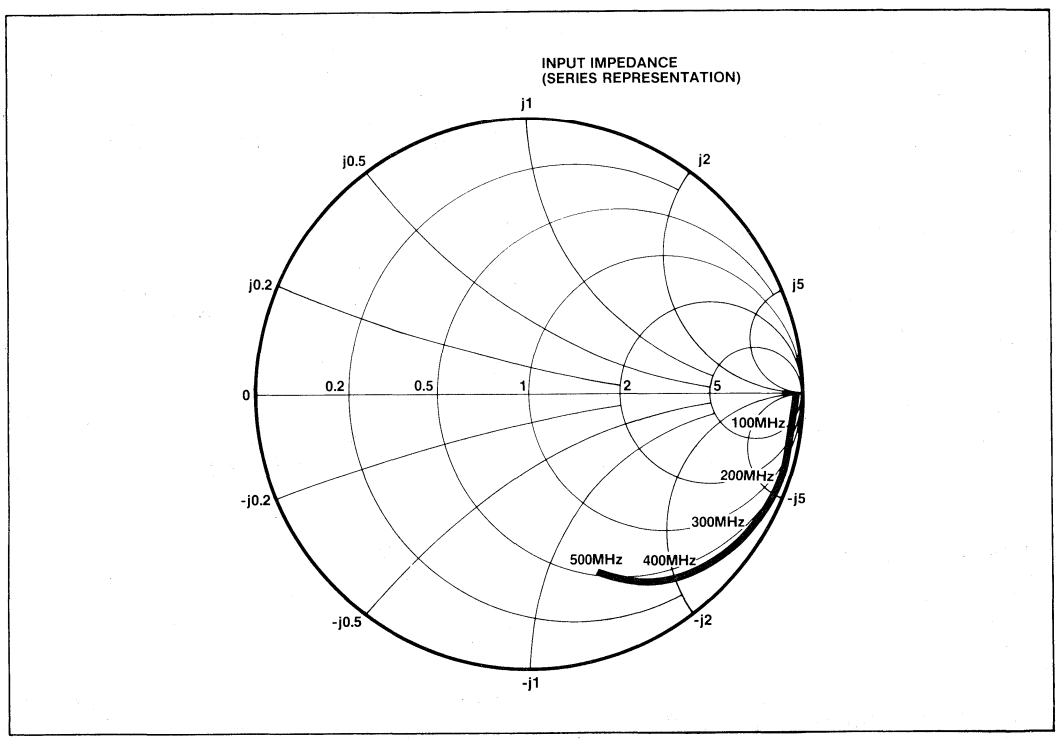


Fig.7 Input impedance of SL6140 (50Ω normalised)

SL6270

GAIN CONTROLLED MICROPHONE PREAMPLIFIER/VOGAD

The SL6270 is a silicon integrated circuit combining the functions of audio amplifier and voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 50dB range of input. The dynamic range, attack and decay times are controlled by external components.

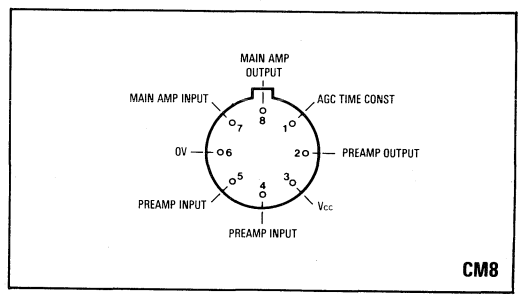


Fig.1 Pin connections, SL6270 - CM (bottom view)

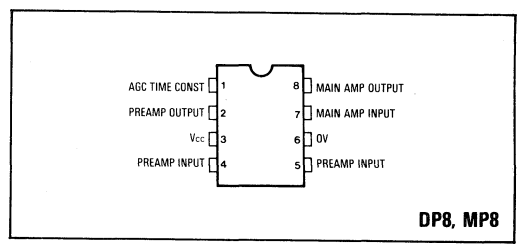


Fig.2 Pin connectons, SL6270 - DP (top view)

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Protection
- Tape Recorders

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 10V
- Voltage Gain: 52dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

ORDERING INFORMATION

SL6270 C CM
SL6270 C DP
SL6270 CB CM
SL6270 NA MP

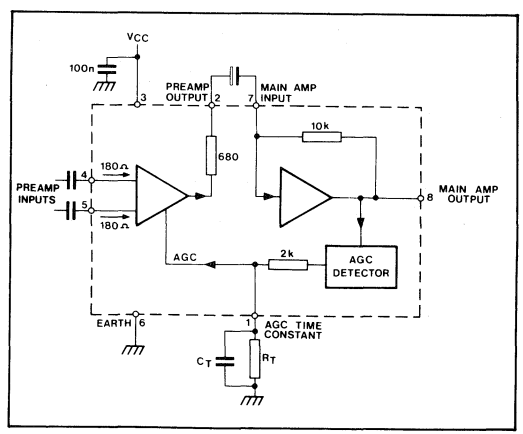
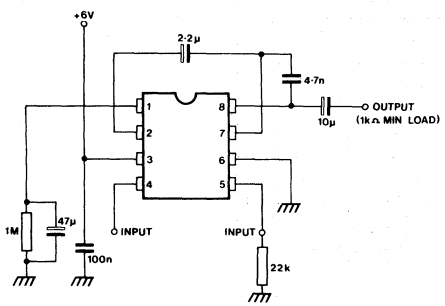


Fig.3 SL6270 block diagram

ELECTRICAL CHARACTERISTICS

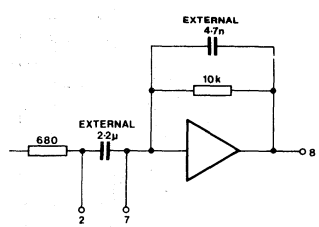
Test conditions (unless otherwise stated):
Supply voltage V_{CC}: 6V
Input signal frequency: 1kHz
Ambient temperature: −30°C to +85°C
Test circuit shown in Fig. 4

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5	10	mA	
Input impedance		150		Ω	Pin 4 or 5
Differential input impedance		300		Ω	
Voltage gain	40	52		dB	72μV rms input pin 4
Output level	55	90	140	mV rms	4mV rms input pin 4
THD		2	5	%	90mV rms input pin 4
Equivalent noise input voltage		1		μV	300Ω source, 400Hz to 25kHz bandwidth



N.B. If input not AC coupled the resistance between pins 4 and 5 must be less than 10 ohms.

Fig.4 SL6270 test and application circuit



$$\text{Voltage gain} = \frac{10k\Omega}{680\Omega}$$

Upper frequency response 10kΩ/4.7nF = 3kHz
Lower frequency response 680Ω/2.2μF = 300Hz

Fig.5 SL6270 frequency response

APPLICATION NOTES

Voltage gain

The input to the SL6270 may be single ended or differential but must be capacitor coupled. In the single-ended mode the signal can be applied to either input, the remaining input being decoupled to ground. Input signals of less than a few hundred microvolts rms are amplified normally but as the input level is increased the AGC begins to take effect and the output is held almost constant at 90mV rms over an input range of 50dB.

The dynamic range and sensitivity can be reduced by reducing the main amplifier voltage gain. The connection of a 1k resistor between pins 7 and 8 will reduce both by approximately 20dB. Values less than 680Ω are not advised.

Frequency response

The low frequency response of the SL6270 is determined by the input, output and coupling capacitors. Normally the coupling capacitor between pins 2 and 7 is chosen to give a -3dB point at 300Hz, corresponding to 2.2μF, and the other capacitors are chosen to give a response to 100Hz or less.

The SL6270 has an open loop upper frequency response of a few MHz and a capacitor should be connected between pins 7 and 8 to give the required bandwidth.

Attack and delay times

Normally the SL6270 is required to respond quickly by holding the output level almost constant as the input is increased. This 'attack time', the time taken for the output to return to within 10% of the original level following a 20dB increase in input level, will be approximately 20ms with the circuit of Fig.4. It is determined by the value of the capacitor connected between pin 1 and ground and can be calculated approximately from the formula:

$$\text{Attack time} = 0.4\text{ms}/\mu\text{F}$$

The decay time is determined by the discharge rate of the capacitor and the recommended circuit gives a decay rate of 20dB/second. Other values of resistance between pin 1 and ground can be used to obtain different results.

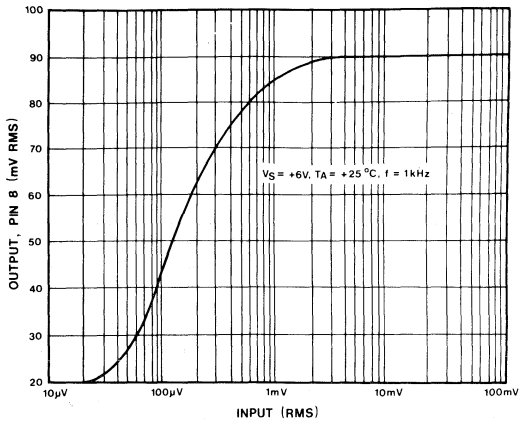


Fig. 6 Voltage gain (single ended input) (typical)

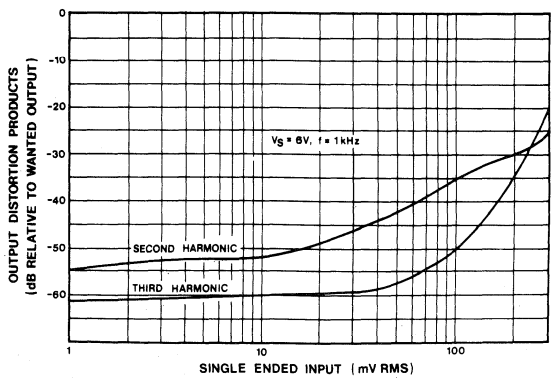


Fig. 7 Overload characteristics (typical)

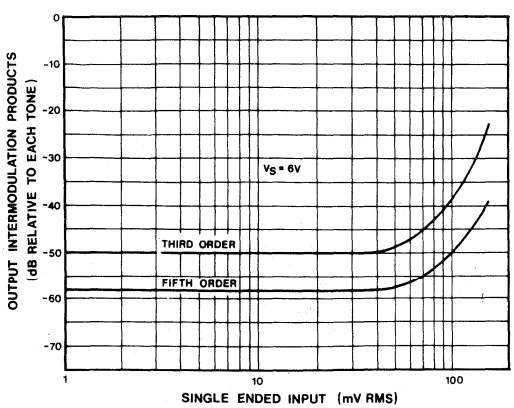


Fig. 8 Typical Intermodulation distortion (1.55 and 1.85kHz tones)

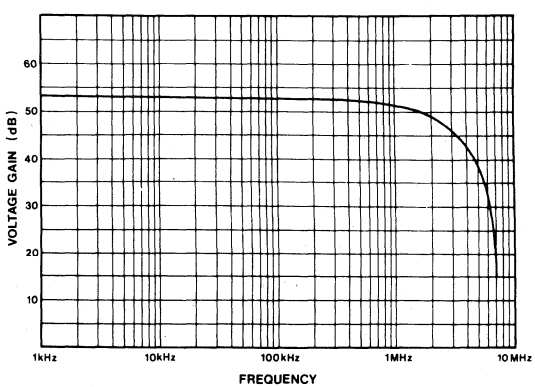


Fig. 9 Open loop frequency response (typical)

SL6310

500mW SWITCHABLE AUDIO AMPLIFIER/OP AMP

The SL6310C is a low power audio amplifier which can be switched off by applying a mute signal to the appropriate pin. Despite the low quiescent current consumption of 5mA (only 0.6mA when muted) a minimum output power of 400mW is available into an 8Ω load from a 9V supply.

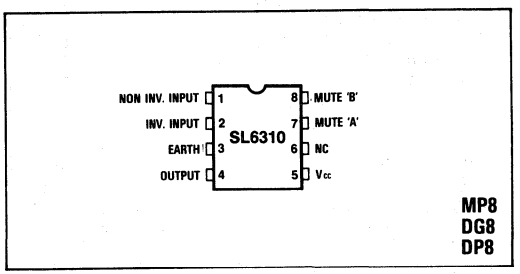


Fig.1 Pin connections SL6310 - (top view)

FEATURES

- Can be Muted with High or Low State Inputs
- Operational Amplifier Configuration
- Works Over Wide Voltage Range

APPLICATIONS

- Audio Amplifier for Portable Receivers
- Power Op. Amp
- High Level Active Filter

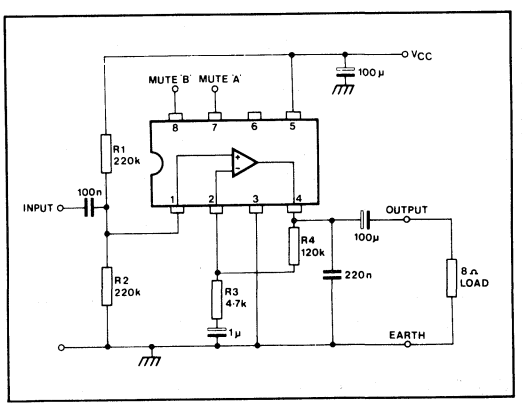


Fig.2 SL6310 test circuit

QUICK REFERENCE DATA

- Supply Voltage : 4.5V to 13.6V
- Voltage Gain : 70dB
- Output into 8Ω on 9V Supply : 400mW (min.)

ORDERING INFORMATION

SL6310 C DG
SL6310 C DP
SL6310 NA MP

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	15V
Storage temperature:	−55°C to + 125°C
Junction temperature:	175°C (DG), 150°C (DP & MP)
Thermal resistance, chip-to ambient	
MP package:	160°C/W
DP package:	100°C/W
DG package:	143°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage Vcc: 9V
Ambient temperature: −30°C to +85°C
Mute facility: Pins 7 and 8 open circuit frequency = 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.0	7.5	mA	
Supply current muted (A)		0.55	1	mA	Pin 7 via 470k to earth
Supply current muted (B)		0.6	0.9	mA	Pin 8 = Vcc
Input offset voltage		2	20	mV	Rs ⩽ 10k
Input offset current		50	500	nA	
Input bias current (Note 1)		0.2	1	μA	
Voltage gain	40	70		dB	
Input voltage range		2.1		V	Vcc = 4.5V
		10.6		V	Vcc = 13V
CMRR	40	60		dB	Rs⩽10k
Output power	400	500		mW	RL = 8Ω
THD		0.4	3	%	POUT = 400mW, gain = 28dB
Output power (Note 2)		250		mW	RL = 8Ω

NOTES
1. The input bias current flows **out** of pins 1 and 2 due to PNP input stage.
2. **Only** applies to MP package, where the power is limited by chip temperature considerations.

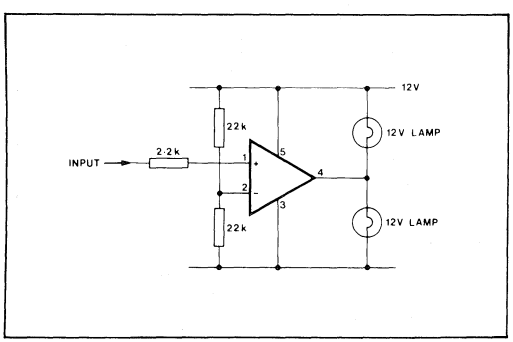


Fig.3 SL6310 lamp driver

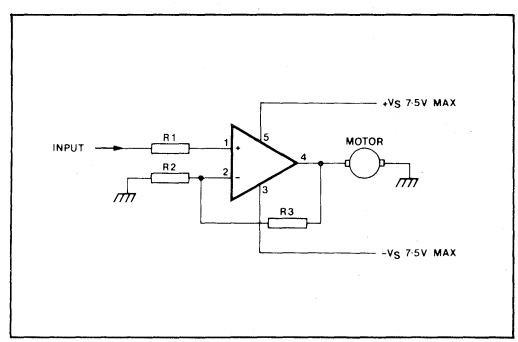


Fig.4 SL6310 servo amplifier

OPERATING NOTES

Mute facility

The SL6310 has twomute control pins to allow easy interfacing to inputs of high or low levels. Mute control 'A', pin 7, is left open circuit or connected to a voltage within 0.65 volt of Vcc (via a 100kΩ resistor) for normal operation. When the voltage on pin 7 is reduced to within 1 volt of earth (via a 100kΩ resistor) the SL6310 is muted.

Audio amplifier

As the SL6310 is an operational amplifier it is easy to obtain the voltage gain and frequency response required. To keep the input impedance high it is wise to feed the signal to the non-inverting input as shown in Fig.2. In this example the input impedance is approximately 100kΩ. The voltage gain is determined by the ratio (R3 + R4)/R3 and should be between 3 and 30 for best results. The capacitor in series with R3, together with the input and output coupling capacitors, determines the low frequency rolloff point. The upper frequency limit is set by the device but can be restricted by connecting a capacitor across R4.

Operational amplifier

It is impossible to list all the application possibilities in a single data sheet but the SL6310 offers considerable advantages over conventional devices in high output current applications such as lamp drivers (Fig.3) and servo amplifiers (Fig.4).

Buffer and output stages for signal generators are another possibility together with active filter sections requiring high output current.

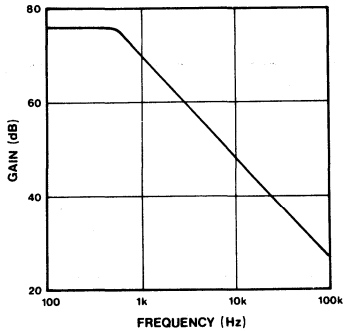


Fig.5 Gain v. frequency

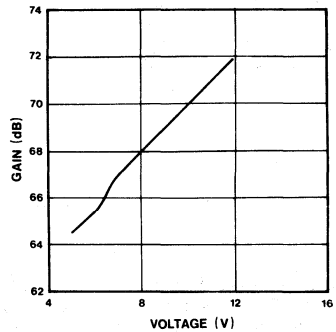


Fig.6 Gain v. supply voltage

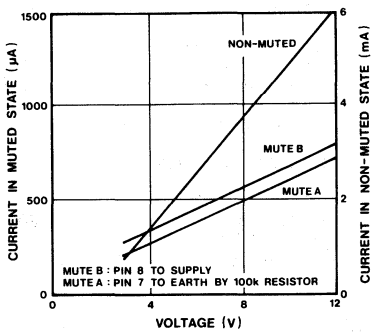


Fig.7 Supply current v. supply voltage

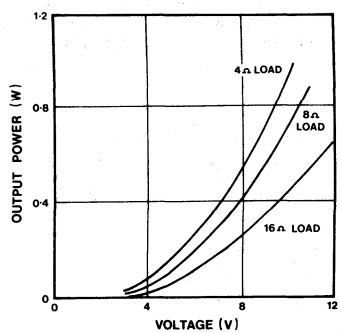


Fig.8 Output power v. supply voltage at 5% (max) distortion

SL6440

HIGH LEVEL MIXER

The SL6440 is a double balanced mixer intended for use in radio systems up to 150MHz. A special feature of the circuit allows external selection of the DC operating conditions by means of a resistor connected between pin 11 (bias) and Vcc. When biased for a supply current of 50mA the SL6440 offers a 3rd order intermodulation intercept point of typically +30dBm, a value previously unobtainable with integrated circuits. This makes the device suitable for many applications where diode ring mixers had previously been used and offers the advantages of a voltage gain, low local oscillator drive requirement and superior isolation.

FEATURES

- +30dBm Input Intercept Point
- +15dBm Compression Point (1dB)
- Programmable Performance
- Full Military Temperature Range (SL6440A)

APPLICATIONS

- Mixers in Radio Transceivers
- Phase Comparators
- Modulators

ORDERING INFORMATION

SL6440 A DG
SL6440 C DP

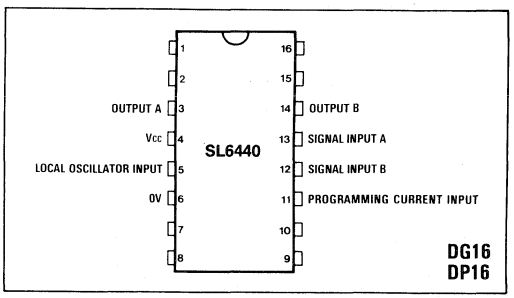


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage and output pins	15V
Maximum power dissipation	1200mW
(Derate above 25°C: 8mW/°C)	
Storage temperature range	-65°C to +150°C
Programming current into pin 11	50mA

THERMAL CHARACTERISTICS

Thermal resistance: θ_{JA}	125°C/W
θ_{JC}	40°C/W
Time constant: Junction-Ambient	1.9 mins
Maximum chip temperature	150°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC1} = 12V; V_{CC2} = 10V; I_P = 25mA; T_{amb} = -55°C to +125°C (SL6440A), -30°C to +85°C (SL6440C)
Local oscillator input level = 0dBm; Test circuit Fig.2.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Signal frequency 3dB point	100	150		MHz	
Oscillator frequency 3dB point	100	150		MHz	
3rd order input intercept point		+30		dBm	
Third order intermodulation distortion		-60		dB	Two 0dBm input
Second order intermodulation distortion		-75		dB	Signals
1dB compression point		15		dBm	V_{CC1} = 15V V_{CC2} = 12V
					V_{CC1} = 12V V_{CC2} = 10V
Noise figure		11		dB	Fig.8 test circuit
Conversion gain		-1		dB	50Ω load Fig.2
Carrier leak to signal input	-40			dB	Test circuit Fig.8
Level of carrier at IF output		-25		dBm	See applications information
Supply current		7		mA	I_P = 0
Supply current (total from V_{CC1} & V_{CC2})		60		mA	
Local oscillator input	100	250	500	mV rms	I_P = 35mA
Local oscillator input impedance		1.5		kΩ	
Signal input impedance		500		Ω	Single ended
		1000		Ω	Differential

NOTE Supply current in Pin 3 is equal to that in Pin 14 and is equal to I_P. See over. V_{pin11} 3 V_{be} 2.1V.

CIRCUIT DESCRIPTION

The SL6440 is a high level mixer designed to have a linear RF performance. The linearity can be programmed using the I_P pin (11).

The output pins are open collector outputs so that the conversion gain and output loads can be chosen for the specific application.

Since the outputs are open collectors they should be returned to a supply $V_{CC}1$ through a load.

The choice of $V_{CC}1$ is important since it must be ensured that the voltage on pins 3 and 14 is not low enough to saturate the output transistors and so limit the signal swing unnecessarily. If the voltage on pins 3 and 14 is always greater than $V_{CC}2$ the outputs will not saturate. The output frequency response will reduce as the output transistors near saturation.

Minimum $V_{CC}1$ = (I_P x RL) + V_S + $V_{CC}2$
where I_P = programmed current
RL = DC load resistance
V_S = max signal swing at output
if the signal swing is not known:
minimum $V_{CC}1$ = 2 (I_P x RL) + $V_{CC}2$

In this case the signal will be limiting at the input before the output saturates.

The device has a separate supply ($V_{CC}2$) for the oscillator buffer (pin 4).

The current (I_P) programmed into pin 11 can be supplied via a resistor from $V_{CC}1$ or from a current source.

The conversion gain is equal to

$$GdB = 20 \text{ Log } \frac{RL\ I_P}{56.61\ I_P + 0.0785} \text{ for single-ended output}$$

$$GdB = 20 \text{ Log } \frac{2\ RL\ I_P}{56.61\ I_P + 0.0785} \text{ for differential output}$$

Device dissipation is calculated using the formula

mW diss = 2 I_P V_O + V_P I_P + $V_{CC}2$ Diss
where V_O = voltage on pin 3 or pin 14
V_P = voltage on pin 11
I_P = programming current (mA)
$V_{CC}2$ Diss = dissipation obtained from graph (Fig.6)

As an example Fig. 7 shows typical dissipations assuming $V_{CC}1$ and V_O are equal. This may not be the case in practice and the device dissipation will have to be calculated for any particular application.

Fig.5 shows the intermodulation performance against I_P. The curves are independent of $V_{CC}1$ and $V_{CC}2$ but if $V_{CC}1$ becomes too low the output signal swing cannot be accommodated, and if $V_{CC}2$ becomes too low the circuit will not provide enough drive to sink the programmed current. Examples are shown of performance at various supply voltages.

The current in pin 14 is equal to the current in pin 3 which is equal to the current in pin 11.

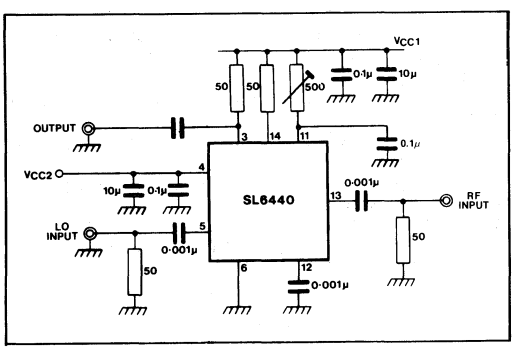


Fig.2 Typical application and test circuit

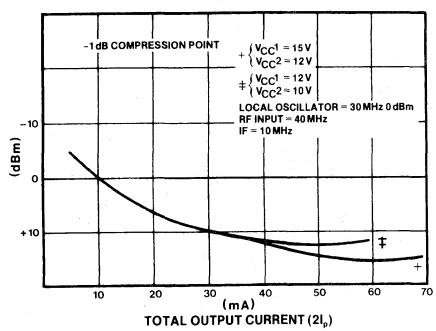


Fig.3 Compression point v. total output current

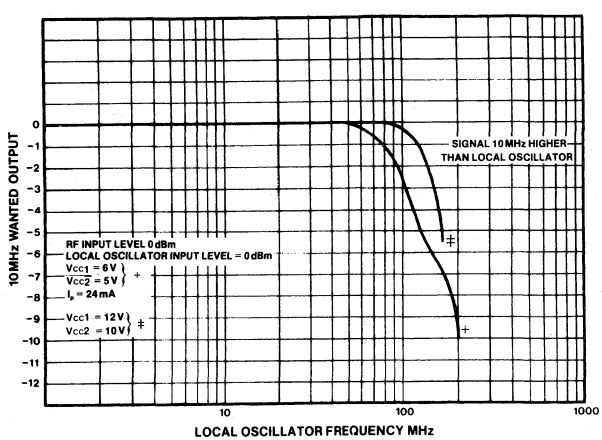


Fig.4 Frequency response at constant output IF

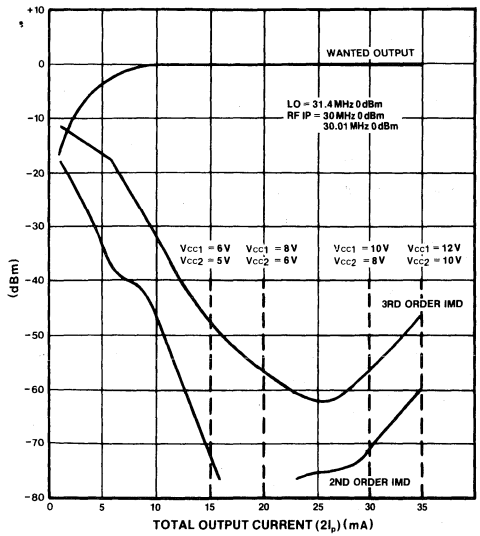


Fig.5 Intermodulation v. programming current

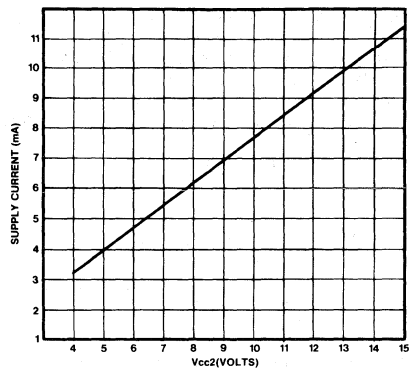


Fig.6 Supply current v. Vcc2 (Ip = 0)

APPLICATIONS

The SL6440 can be used with differential or single-ended inputs and outputs. A balanced input will give better carrier leak. The high input impedance allows step-up transformers to be used if desired, whilst high output impedance allows a choice of output impedance and conversion gain.

Fig. 2 shows the simplest application circuit. The input and output are single-ended and I_P is supplied from Vcc1 via a resistor. Increasing RL will increase the conversion gain, care being taken to choose a suitable value for Vcc1.

Fig. 8 shows an application with balanced input, for improved carrier leak, and balanced output for increased conversion gain. A lower Vcc1 giving lower device dissipation can be used with this arrangement.

DESIGN PROCEDURE

1. Decide on input configuration using local oscillator data. If using transformer on input, decide on ratio from noise considerations.
2. Decide on output configuration and value of conversion gain required.
3. Decide on value of I_P and Vcc2 using intermodulation and compression point graphs.
4. Using values of conversion gain, Vcc2, load and I_P already chosen, decide on value of Vcc1.
5. Calculate device dissipation and decide whether heatsink is required from maximum operating temperature considerations.

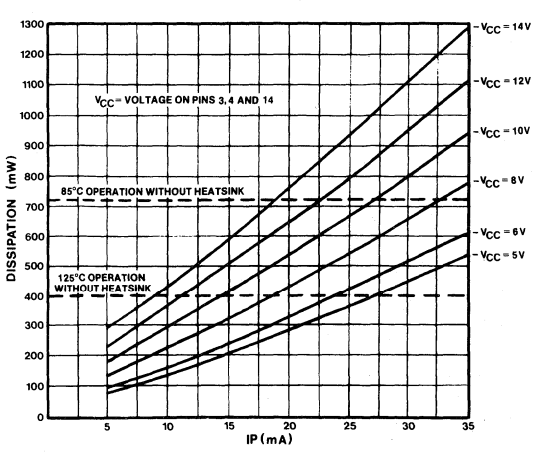


Fig.7 Device dissipation v. I_P

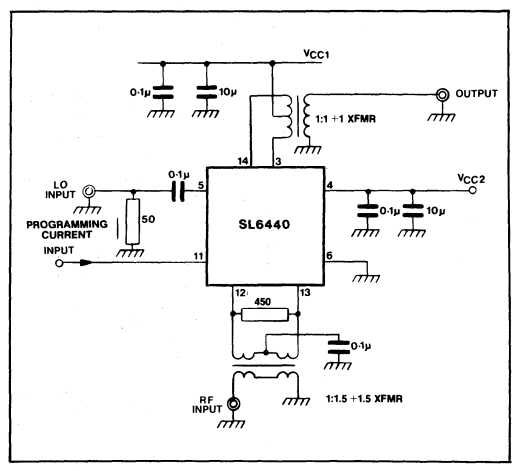


Fig.8 Typical application circuit for highest performance

GEC PLESSEY

SEMICONDUCTORS

SL6601

FM IF, PLL DETECTOR (DOUBLE CONVERSION) AND RF MIXER

The SL6601 is a straight through or single conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits, the SL6601 uses an advanced phase locked loop detector capable of giving superior signal-to-noise ratio with excellent co-channel interference rejection, and operates with an IF of less than 1MHz. Normally the SL6601 will be fed with an input signal of up to 17MHz: there is a crystal oscillator and mixer for conversion to the IF amplifier, a PLL detector and squelch system.

FEATURES

- High Sensitivity: 2μV Typical
- Low Power: 2·3mA Typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 100% Tested for SINAD

APPLICATIONS

- Low Power NBFM Receivers
- FSK Data Equipment
- Cellular Radio Telephones

QUICK REFERENCE DATA

- Supply Voltage 7V
- 50dB S/N Ratio

ORDERING INFORMATION

SL6601 C DG
SL6601 C DP
SL6601 C LC

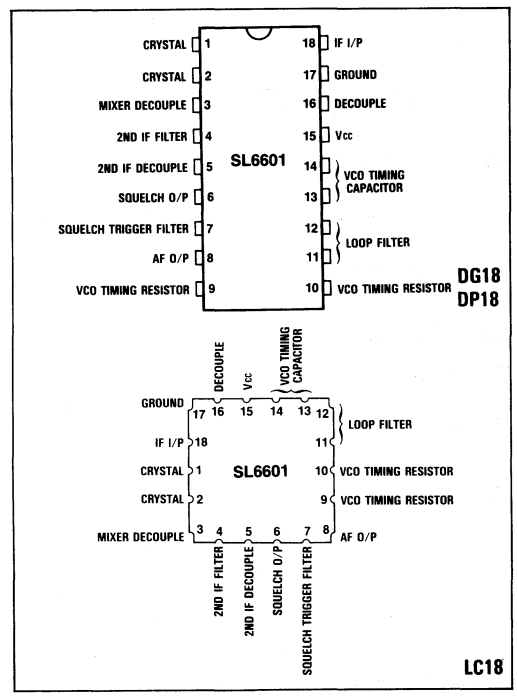


Fig.1 Pin connections - top view

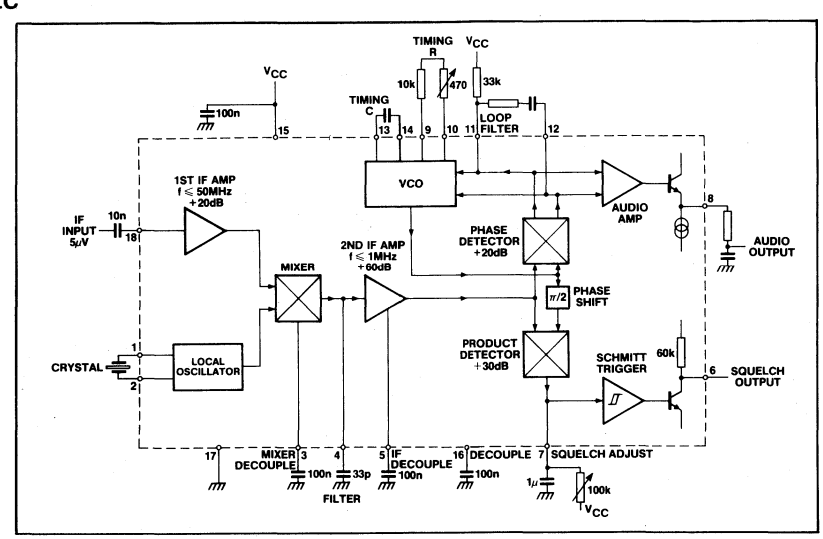


Fig.2 SL6601 block diagram

Example

A frequency modulated signal has a deviation of 10kHz and a maximum modulating frequency of 5kHz. The VCO frequency is 200kHz.

Let $f_n = 6kHz$ and $D = 0.5$

Then from the graph

$$\frac{\Phi_{efn}}{\Delta f} = 0.85$$

$$\Phi_e = \frac{0.85\Delta f}{f_n} = \frac{0.85 \times 10}{6} = 1.4 \text{ rads.}$$

This is too large, so increase f_n e.g. to 10kHz.

$$\frac{f_m}{f_n} = 0.5 \quad \frac{\Phi_{efn}}{\Delta f} = 0.45$$

$$\Phi_e = \frac{0.45 \times 10}{10} = 0.45$$

- which is somewhat low

Therefore set $f_n = 7.5kHz$

$$\frac{f_m}{f_n} = 0.666$$

$$\frac{\Phi_{efn}}{\Delta f} = 0.66$$

$$\Phi_e = \frac{0.66 \times 10}{7.5} = 0.88 \text{ rads.}$$

$$t_1 + t_2 = \frac{K_O K_D}{(2\pi f_n)^2}$$

$K_O K_D = 0.3 f_o$ where f_o is the VCO frequency

$$t_1 + t_2 = \frac{0.3 \times 200 \times 10^3}{(2\pi \times 7.5 \times 10^3)^2} = 27\mu s$$

$$t_2 = \frac{D}{\pi f_n} - \frac{1}{K_O K_D}$$

$$= \frac{0.5}{\pi \times 7.5 \times 10^3} - \frac{1}{0.3 \times 200 \times 10^3}$$

$$= 4.5\mu s$$

$$t_1 = 22.5\mu s$$

$$C = \frac{t_1}{20 \times 10^3} = \frac{22.5 \times 10^{-6}}{20 \times 10^3} = 1.125nF \text{ (use 1nF)}$$

$$R = \frac{t_2}{t_1} \times 20 \times 10^3$$

$$= \frac{4.5}{22.5} \times 20 \times 10^3$$

$$= 4k\Omega \text{ (use 3.9k)}$$

Actual loop parameters can now be recalculated

$t_1 = 20\mu s$ $t_2 = 3.9\mu s$

$$2\pi f_n = \frac{(K_O K_D)}{(t_1 \times t_2)} = \frac{(2 \times 10^5 \times 0.3)}{(23.9 \times 10^{-6})} = 50.1k \text{ rad/sec} = 7.97kHz$$

$$D = f_n(t_2 + \frac{1}{K_O K_D}) = \underline{0.515}$$

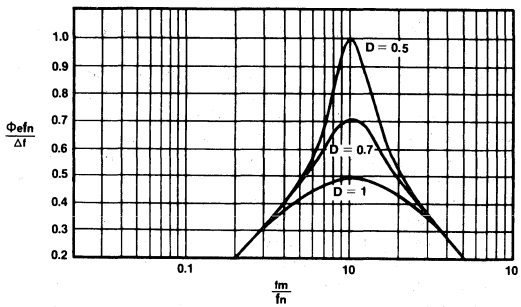


Fig.3 Damping factor

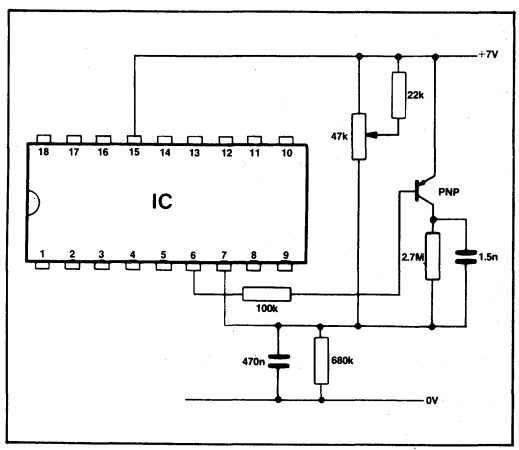


Fig.4 Using an external PNP in the squelch circuit

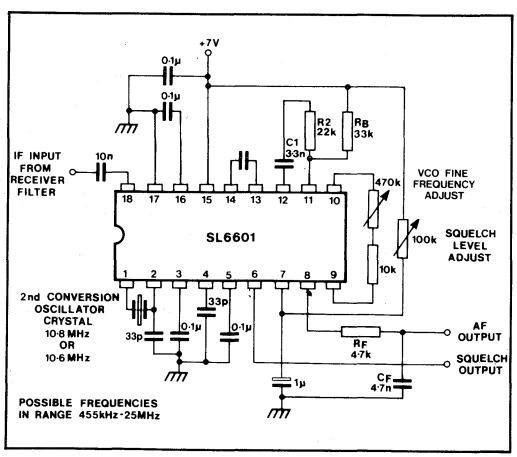


Fig.5 SL6601 application diagram
(1st IF = 10.7MHz, 2nd IF = 100kHz)

TYPICAL CHARACTERISTICS

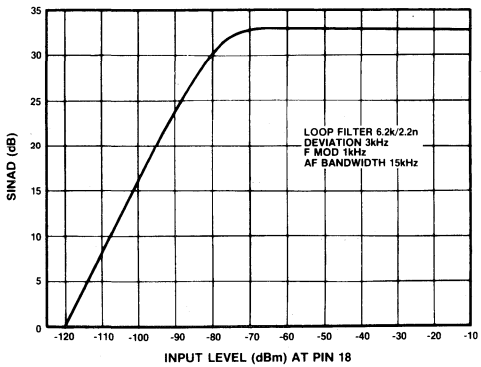


Fig.6 Typical SINAD
(signal + noise + distortion/noise + distortion)

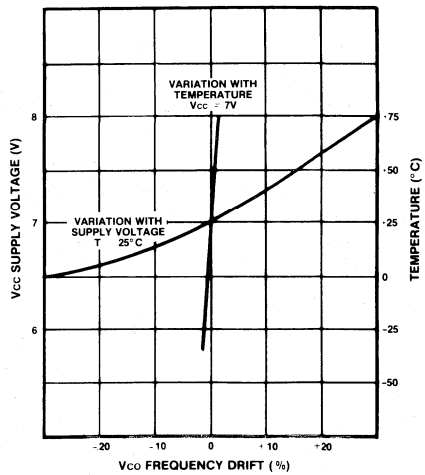


Fig.9 Typical VCO characteristics

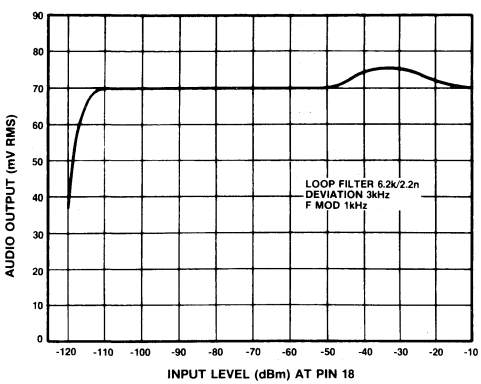


Fig.7 Typical recovered audio v. input level (3kHz deviation)

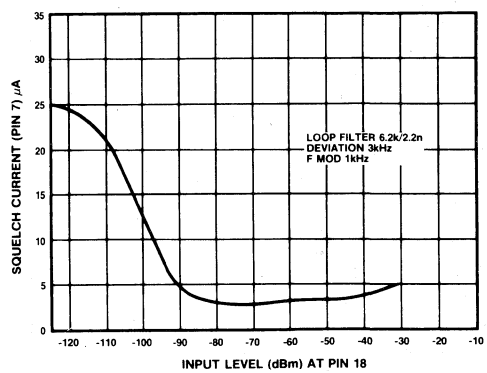


Fig.10 Typical squelch current v. input level

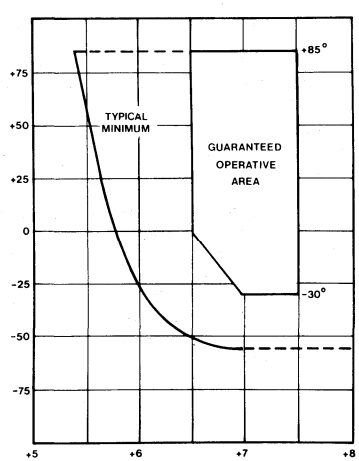


Fig.8 Supply voltage v. temperature

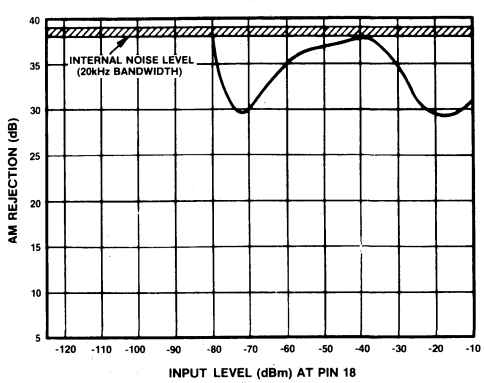


Fig.11 Typical AM rejection

(the ratio between the audio output produced by:
(a) a 3kHz deviation 1kHz modulation FM signal and
(b) a 30% modulated 1kHz modulation AM signal at the same input voltage level.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} : 7V
Input signal frequency: 10.7MHz, frequency modulated with a 1kHz tone with a ±2.5kHz frequency deviation
Ambient temperature: -30°C to +85°C; IF = 100kHz; AF bandwidth = 15kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		2.3	2.7	mA	
Input impedance	100		300	Ω	Source impedance = 200Ω
Input capacity	0.5	2.0	3.5	pF	
Maximum input voltage level	0.5			V rms	At pin 18
Sensitivity	5	2		μV rms	At pin 18 for S + N/N = 20dB
Audio output	35	90	140	mV rms	
Audio THD		1.3	3.0	%	1mV rms input at pin 18
S + N/N	30	50		dB	1mV rms input at pin 18
AM rejection	30	Note 1		dB	100μV rms input at pin 18, 30% AM
Squelch low level		0.2	0.5	V dc	20μV rms input at pin 18
Squelch high level	6.5	6.9		V dc	No input
Squelch hysteresis		1	6	dB	3μV input at pin 18
Noise figure		6		dB	50Ω source
Conversion gain		30		dB	Pin 18 to pin 4
Input gain compression		100		μV rms	Pin 18 to pin 4, 1dB compression
Squelch output load	250			kΩ	
Input voltage range	80	100		dB	At pin 8; above 20dB S + N/N
3rd order intercept point (input)		-38		dBm	Input pin 18, output pin 4
VCO frequency					
Grade 1	85		100	kHz	390pF timing capacitor, No input
Grade 2	95		110	kHz	390pF timing capacitor, No input
Grade 3	105		120	kHz	390pF timing capacitor, No input
Source impedance (pin 4)		25	40	kΩ	
AF output impedance		4	10	kΩ	
Lock-in dynamic range	±8			kHz	20μV to 1mV rms at pin 18
External LO drive level	50		250	mV rms	At pin 2
Crystal ESR			25	Ω	10.8MHz

APPLICATION NOTES

IF Amplifiers and Mixer

The SL6601 can be operated either in a 'straight through' mode with a maximum recommended input frequency of 800kHz or in a single conversion mode with an input frequency of 50MHz maximum and an IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IF's; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 17MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used, with some degradation in performance.

E.G. If an external oscillator is used the recommended level is 70mV rms and the unused pin should be left O/C. The input is AC coupled via a 0.01μF capacitor.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz; 6.8pF is advised for 455kHz.

Phase Locked Loop

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external capacitor equal to (40 ± 7)/f pF, where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine frequency adjustment by means of a variable resistor between the VCO output pins; a value of 470k has negligible effect while 6.8k (recommended minimum value) increases the frequency by approximately 20%.

Care should be taken to ensure that the free running VCO frequency is correct; because the VCO and limiting IF amplifier output produce square waves, it is possible to obtain lock with the VCO frequency fractionally related to the IF, e.g. IF = 100kHz, VCO = 150kHz. This condition can produce good SINAD ratios but poor squelch performance.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and V_{CC}.

The values of the filter resistor R2 and capacitor C1 must be chosen so that the natural loop frequency and damping factor are suitable for the FM deviation and modulation bandwidth required. The recommended values for various conditions are tabulated below:

Centre frequency kHz	Deviation kHz	Resistor kΩ	Capacitor pF
100	5	6.2	2200
100	10	5.6	1800
455	5	4.7	1500
455	10	3.9	1200

Note that the values of loop filter are not critical and in many cases may be omitted.

The AF output voltage depends upon the % deviation and so, for a given deviation, output is inversely proportional to centre frequency. As the noise is constant, the signal to noise ratio is also inversely proportional to centre frequency.

VCO Frequency Grading

The SL6601 is supplied in 3 selections of VCO centre frequency. This frequency is measured with a 390pF timing capacitor and no input signal.

Devices are coded 'SL6601C' and a '/1', '/2', '/3' to indicate the selection.

Frequency tolerances are:

/1 85 - 100kHz (or uncoded)
/2 95 - 110kHz
/3 105 - 120kHz

Note that orders cannot be accepted for any particular selection, but all devices in a tube will be the same selection.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. The feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and V_{CC} to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 10μF can be chosen to give the required characteristics.

Operation at signal to noise ratios outside the range 5-18dB is not recommended. Where the 'front end' noise is high (because of very high front end gain) the squelch may well never operate. This effect can be obviated by sensible receiver gain distribution.

The load on the squelch output (pin 6) should not be less than 250kΩ. Reduction of the load below this level leads to hysteresis problems in the squelch circuit.

The use of an external PNP transistor allows hysteresis to be increased. See Fig.4. The use of capacitors greater than 1000pF from pin 6 to ground is not recommended.

Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7kΩ and 4.7nF may be used.

Layout Techniques and Alignment

The SL6601 is not critical in PCB layout requirements except in the 'straight through' mode. In this mode, the input components and circuits should be isolated from the VCO components, as otherwise the VCO will attempt to 'lock' to itself, and the ultimate signal to noise ratio will suffer.

The recommended method of VCO adjustment is with a frequency measurement system on pin 9. The impedance must be high, and the VCO frequency is adjusted with no input signal.

LOOP FILTER DESIGN

The design of loop filters in PLL detectors is a straight forward process. In the case of the SL6601 this part of the circuit is non-critical, and in any case will be affected by variations in internal device parameters. The major area of importance is in ensuring that the loop bandwidth is not so low as to allow unlocking of the loop with modulation.

Damping Factor can be chosen for maximum flatness of frequency response or for minimum noise bandwidth, and values between 0.5 and 0.8 are satisfactory, 0.5 giving minimum noise bandwidth.

Design starts with an arbitrary choise of f_n, the natural loop frequency. By setting this at slightly higher than the maximum modulation frequency, the noise rejection can be slightly improved. The ratio f_m/f_n highest modulating frequency to loop frequency can then be evaluated.

From the graph, Fig.3 the value of the function

$$\frac{\Phi_e f_n}{\Delta f}$$

can be established for the desired damping factor.

Φ_e - peak phase error

f_n - loop natural frequency

Δf - maximum deviation of the input signal

and as f_n and Δf are known, Φ_e is easily calculated. Values for Φ_e should be chosen such that the error in phase is between 0.5 and 1 radian. This is because the phase detector limits at $\pm\pi/2$ radians and is non linear approaching these points. Using a very small peak phase error means that the output from the phase detector is low, and thus impairs the signal to noise ratio. Thus the choice of a compromise value, and 0.5 to 1 radian is used. If the value of Φ_e achieved is far removed from this value, a new value of f_n should be chosen and the process repeated.

With f_n and D established, the time constants are derived from

$$t_1 + t_2 = \frac{K_O K_D}{(2\pi f_n)^2}$$

$$\text{and } t_2 = \frac{D}{\pi f_n} - \frac{1}{K_O K_D}$$

$K_O K_D$ is $0.3f_o$, where f_o is the operating frequency of the VCO. t_1 is fixed by the capacitor and an internal 20kΩ resistor: t_2 is fixed by the capacitor and external resistor.

$$\text{so } C = \frac{t_1}{2C \times 10^3}$$

$$\text{and } R_{ext} = \frac{t_2 \times 20 \times 10^3}{t_1}$$

In order that standard values may be used, it is better to establish a value of C and use the next lowest standard value e.g. $C_{calc} = 238pF$, use 220pF, as it is better to widen the loop bandwidth rather than narrow it.

The value of R_{ext} is then 'rounded up' by a similar process. It is, however, better to increase R_{ext} to the nearest preferred value as loop bandwidth is proportional $(R_{ext}) - \frac{1}{2}$ while damping factor is proportional to R: thus damping factor is increasing more quickly which gives a more level response.

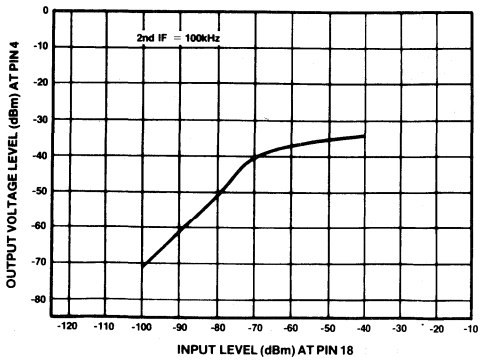


Fig.12 Typical conversion gain (to pin 4)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	9V
Storage temperature	-55° C to +125° C (DP package)
	-55° C to +150° C (DG)
Operating temperature	-55° C to +125° C
(see Electrical Characteristics)	
Input voltage	1V RMS at pin 18

SL6700

IF AMPLIFIER AND AM DETECTOR WITH NOISE BLANKER

The SL6700A is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6700A will be fed with a first IF signal of 10.7MHz or 21.4MHz; there is a mixer for conversion to the first or second IF, a detector, an AGC generator with optional delayed output and a noise blanker monostable. This device is characterised for operation from -55°C to +125°C.

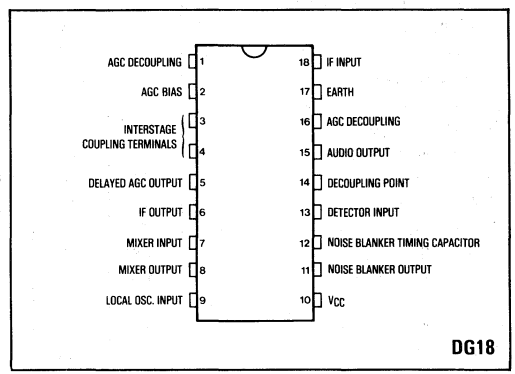


Fig.1 Pin connections (top view)

FEATURES

- High Sensitivity: 10μV Minimum
- Low Power: 8mA Typical at 6V
- Linear Detector
- Full MIL Temperature Range

APPLICATIONS

- Low Power AM/SSB Receivers

QUICK REFERENCE DATA

- Supply Voltage: 4.5V
- Input Dynamic Range: 100dB Typical

ORDERING INFORMATION

SL6700 A DG
SL6700 AB DG

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7.5V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C

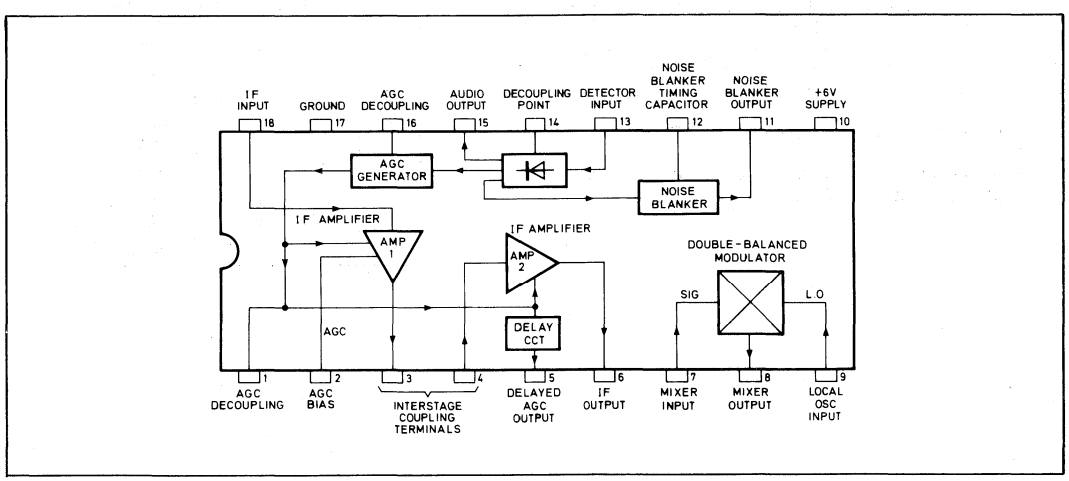


Fig.2 SL6700A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} -55°C to +125°C Test circuit Fig.6. Modulation frequency 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4		7	V	Optimum performance at 4.5V
Supply current		3.5	7	mA	
S/N ratio		40		dB	1mV input 80% modulation
TH distortion		3	5	%	**1mV input 30% modulation**
Sensitivity	10	5		μV	**10dB S + N/N ratio, 30%**
Audio output level change		6	10	dB	**10μV to 50mV input 80%**
AGC threshold		5		μV	
AGC range		80		dB	
AF output level	20	40		mV rms	30% modulation 1mV input
Delayed AGC threshold		10		mV rms	80% modulation
Dynamic range		100		dB	Noise floor to overload
IF frequency response	15	25		MHz	3dB gain reduction
IF amplifier gain	40	50	60	dB	10.7MHz (both amplifiers cascaded)
Detector gain	40	46	55	dB	455kHz 80% AM
Detector Z_{in} pin 13	2	4	6.8	kΩ	
IF amplifier Z_{in} pin 18	1.8	3	4.5	kΩ	
Noise blank level	4.0			V	Logic 1
			0.3	V	Logic 0
Noise blank duration	300	400	500	μs	C pin 12 = 30nF,R pin 12-11 = 18k
Mixer conversion gain	1.0R	1.2R	1.5R	kΩ	R is load resistor in kΩ
Mixer Z_{in} (Signal)	2	3	5	kΩ	
Mixer Z_{in} (L.O.)	3	5	8	kΩ	
Mixer L.O. injection	50	100	150	mV rms	fc = 10.245MHz
Detector output voltage change	6	8	8.2	dB	1mV rms input, modulation increased from 30% to 80%

OPERATING NOTES

The noise blank duration can be varied from the suggested value of 30μs using the formula: Duration time = 0.7CR, where R is value of resistor between pins 11 and 12 and C is value of capacitor from pin 12 to ground.

There is no squelch in the SL6700A and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system.

The mixer may also be used as a product detector. Further application information is available on request.

TYPICAL DC PIN VOLTAGES

(Supply 4.5V, Input 1mV)

Pin	Voltage	Pin	Voltage
1	2.25V	10	4.5V
2	2.09V	11	3.7V
3	3.68V	12	0V
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

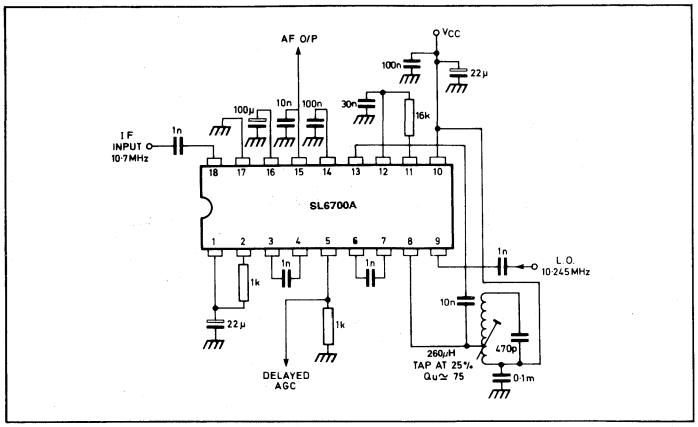


Fig.3 SL6700A AM double conversion receiver with noise blanker

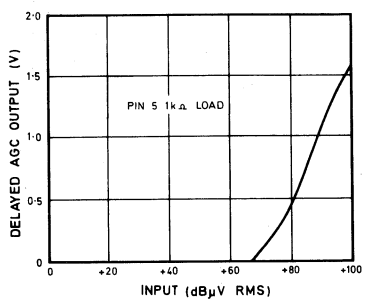


Fig.4 Typical delayed AGC output variation with input signal (f = 10.7MHz, 30% modulation)

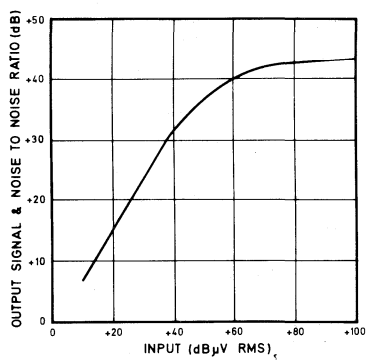


Fig.5 Typical signal to noise ratio (S + N/N) with input signal (f = 10.7MHz, 30% modulation)

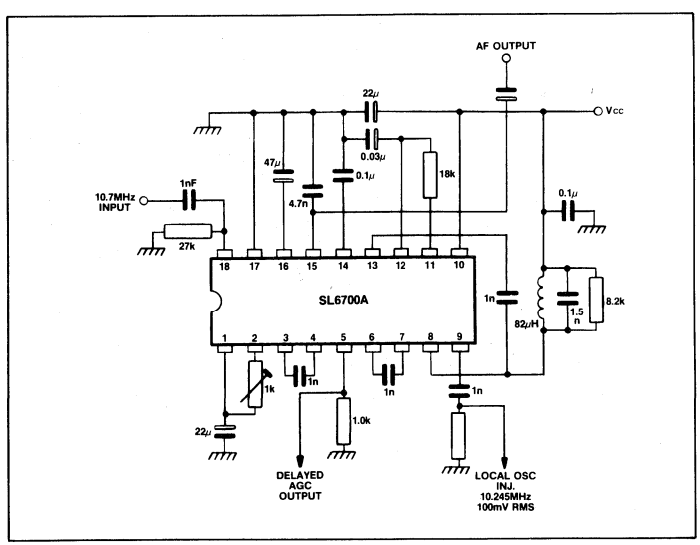


Fig.6 Test circuit

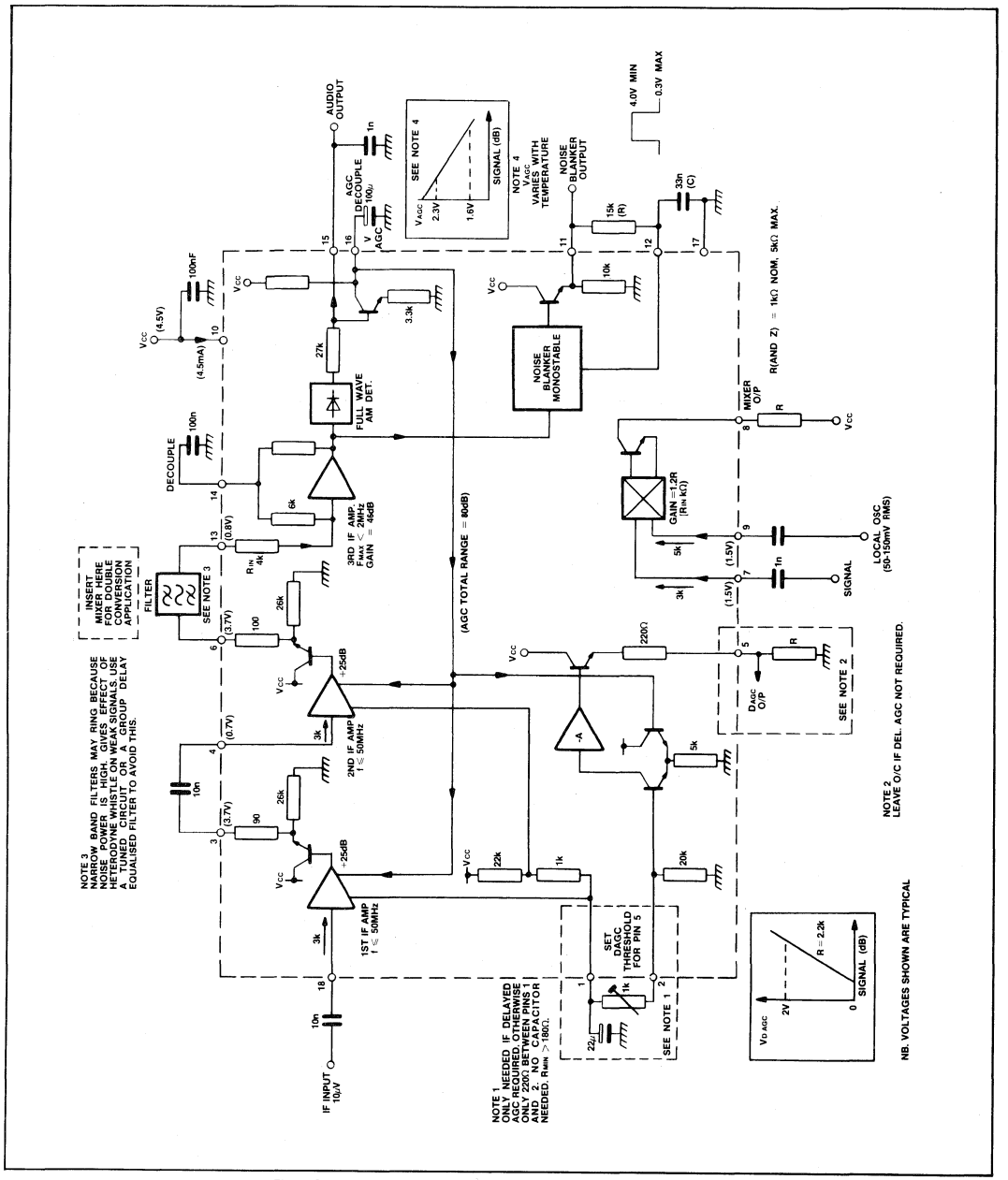


Fig.7 SL6700A Typical application circuit showing interfacing

GEC PLESSEY

SEMICONDUCTORS

SL6701

AM IF AND DETECTOR (DOUBLE CONVERSION)

The SL6701A is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6701A will be fed with a first IF signal of 10.7MHz or 21.4MHz; there is a mixer for conversion to the first or second IF, a detector and an AGC generator with optional delayed output. This device is characterised for operation from -55°C to +125°C.

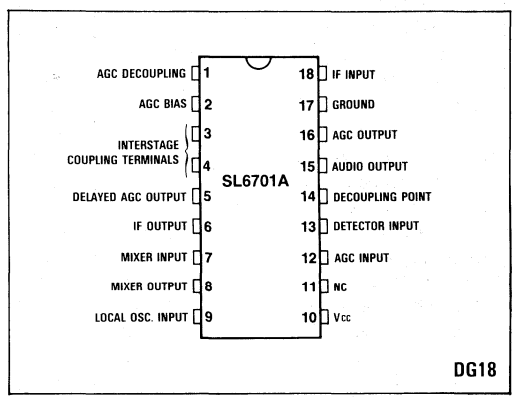


Fig.1 Pin connections - top view

FEATURES

- High Sensitivity: 10uV Minimum
- Low Power: 8mA Typical at 6V
- Linear Detector
- Full MIL Temperature Range

APPLICATIONS

- Low Power AM/SSB Receivers

QUICK REFERENCE DATA

- Supply Voltage: 4.5V
- Input Dynamic Range: 100dB Typical

ORDERING INFORMATION

SL6701 A DG
SL6701 AB DG

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7.5V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C

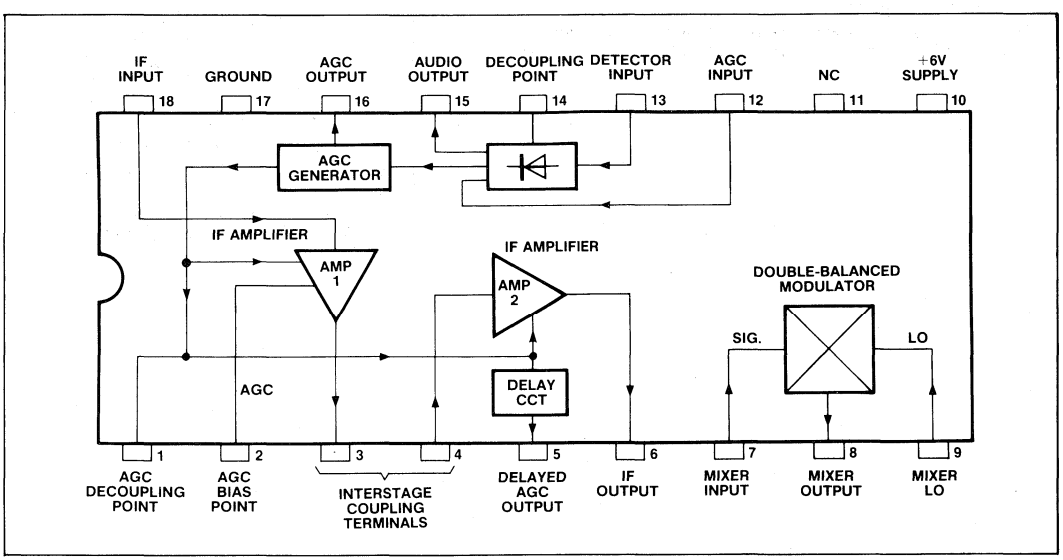


Fig.2 SL6701A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = -55°C to +125C Test circuit Fig.6. Modulation frequency 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4		7	V	Optimum performance at 4.5V
Supply current		3.5	7	mA	
S/N ratio		40		dB	1mV input 80% modulation
TH distortion		3	5	%	1mV input 30% modulation
Sensitivity	10	5		μV	10dB S + N/N ratio, 30%
Audio output level change		6	10	dB	10μV to 50mV input 80%
AGC threshold		5		μV	
AGC range		80		dB	
AF output level	20	40		mV rms	30% modulation 1mV input
Delayed AGC threshold		10		mV rms	80% modulation
Dynamic range		100		dB	Noise floor to overload
IF frequency response	15	25		MHz	3dB gain reduction
IF amplifier gain	40	50	60	dB	10.7MHz (both amplifiers cascaded)
Detector gain	40	46	55	dB	455kHz 80% AM
Detector Z_{in} pin 13	2	4	6.8	kΩ	
IF amplifier Z_{in} pin 18	1.8	3	4.5	kΩ	
Mixer conversion gain	1.0R	1.2R	1.5R	kΩ	R is load resistor in kΩ
Mixer Z_{in} (Signal)	2	3	5	kΩ	
Mixer Z_{in} (LO)	3	5	8	kΩ	
Mixer LO injection	50	100	150	mV rms	fc = 10.245MHz
Detector output voltage change	6	8	8.2	dB	1mV rms input, modulation increased from 30% to 80%

OPERATING NOTES

There is no squelch in the SL6701A and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system.

The mixer may also be used as a product detector. Further application information is available on request.

TYPICAL DC PIN VOLTAGES

(Supply 4.5V, Input 1mV)

Pin	Voltage	Pin	Voltage
1	2.25V	10	4.5V
2	2.09V	11	2.5V*
3	3.68V	12	
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

* Pins 11 and 12 connected together

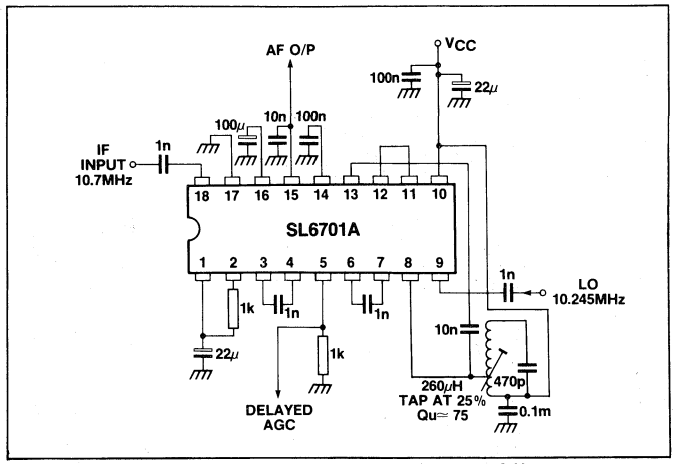


Fig.3 SL6701A AM double conversion receiver with noise blanker

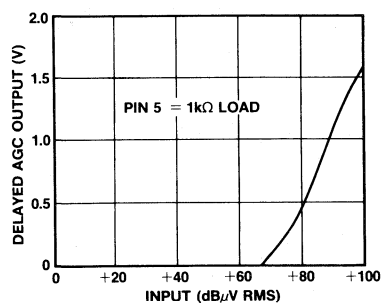


Fig.4 Typical delayed AGC output variation with input signal (f = 10.7MHz, 30% modulation)

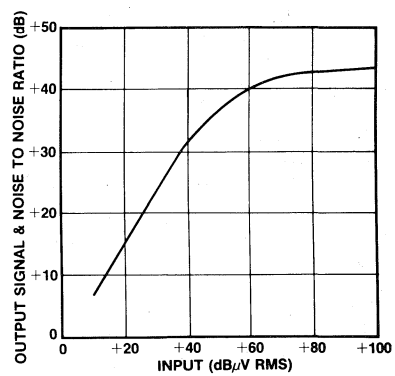


Fig.5 Typical signal to noise ratio (S + N/N) with input signal (f = 10.7MHz, 30% modulation)

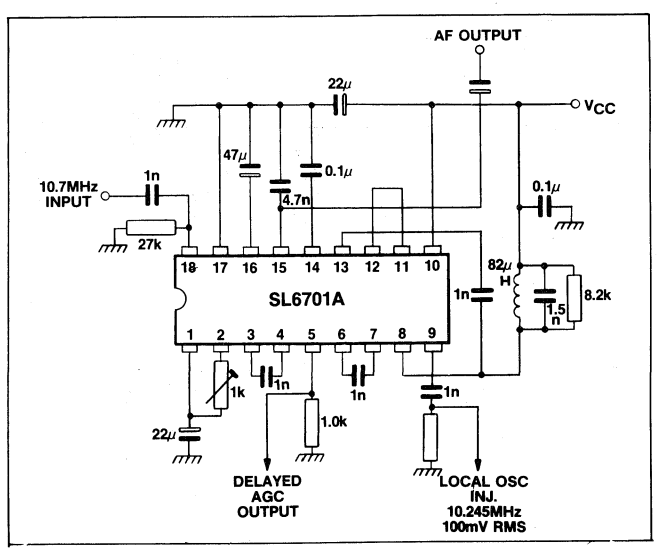


Fig.6 Test circuit

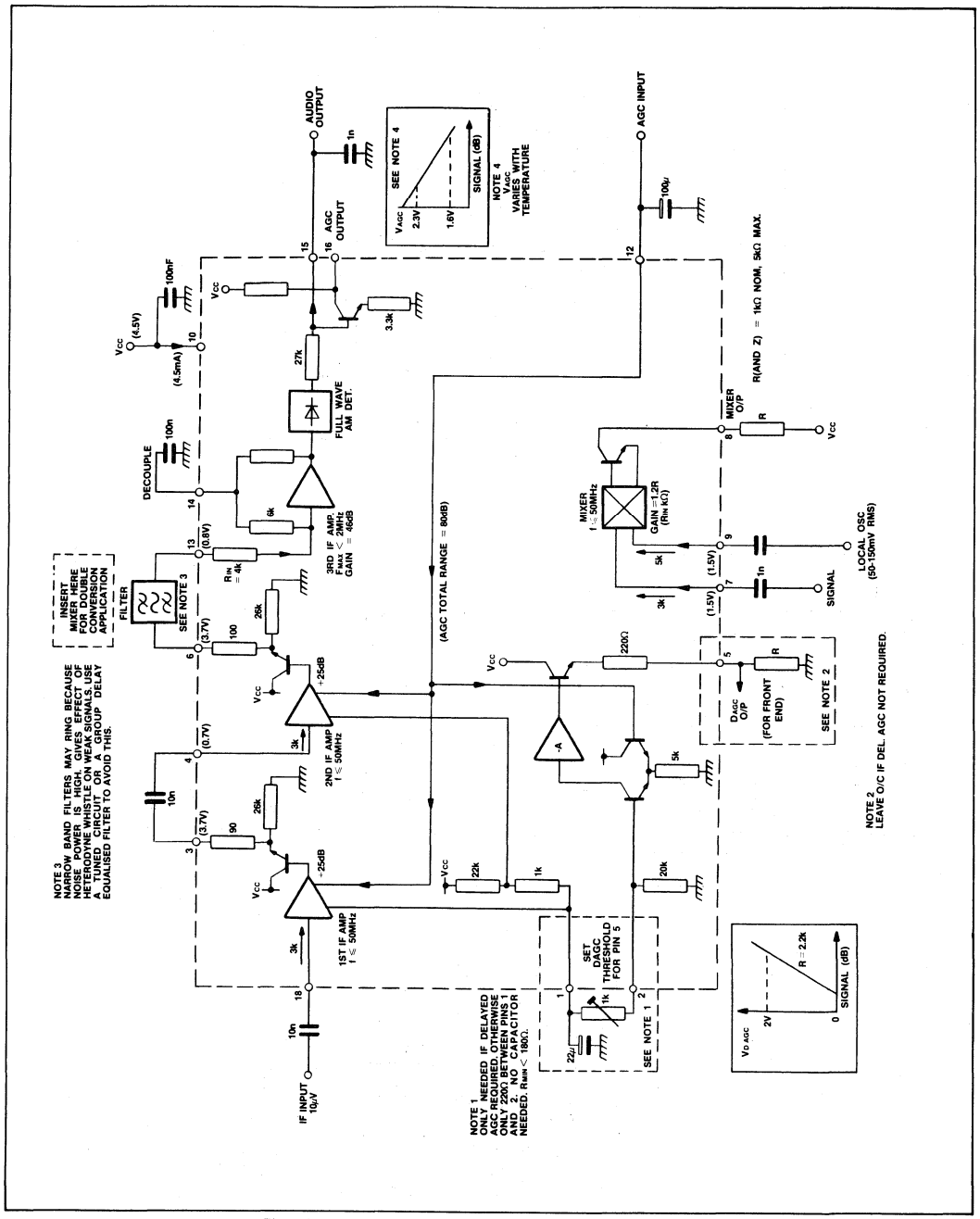


Fig.7 SL6701A typical application circuit showing interfacing

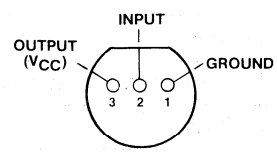
ZN414Z, ZN415E, ZN416E

AM RADIO RECEIVERS

FEATURES

- Single cell operation (1.1 to 1.6 volt operating range)
- Low current consumption
- 150kHz to 3MHz frequency range (i.e. full coverage of medium and long wavebands)
- Easy to assemble, no alignment necessary
- Simple and effective AGC action
- Will drive crystal earphone direct (ZN414Z)
- Will drive headphones direct (ZN415E and ZN416E)
- Excellent audio quality
- Typical power gain of 72dB (ZN414Z)
- Minimum of external components required

ZN414Z



PLASTIC (TO-92)

ZN415E
ZN416E

DP8

GENERAL DESCRIPTION

The ZN414Z is a 10 transistor tuned radio frequency (TRF) circuit packaged in a 3-pin TO-92 plastic package for simplicity and space economy.

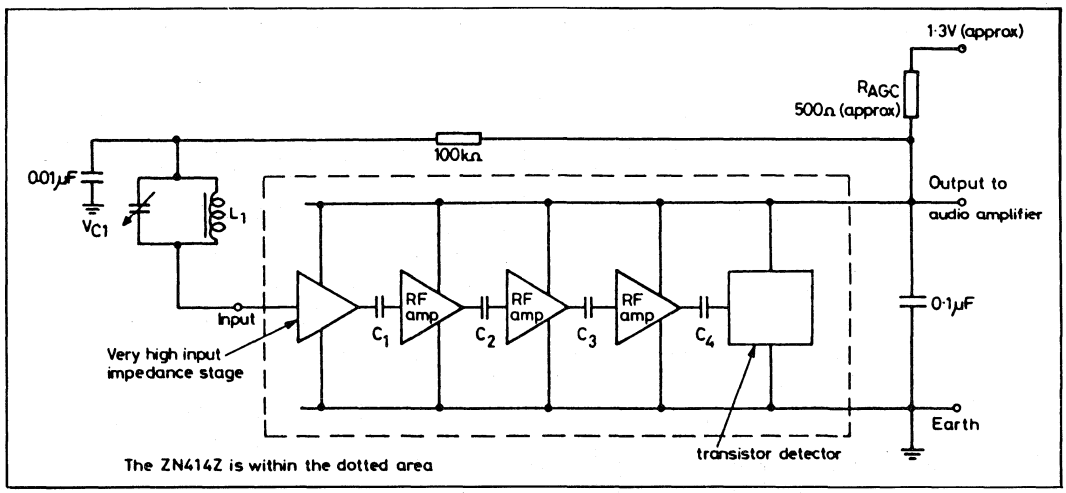
The circuit provides a complete R.F. amplifier, detector and AGC circuit which requires only six external components to give a high quality A.M. tuner. Effective AGC action is available and is simply adjusted by selecting one external resistor value. Excellent audio quality can be achieved, and current consumption is extremely low. No setting-up or alignment is required and the circuit is completely stable in use.

The ZN415E retains all the features of the ZN414Z but also incorporates a buffer stage giving sufficient output to drive headphones directly from the 8 pin DIL.

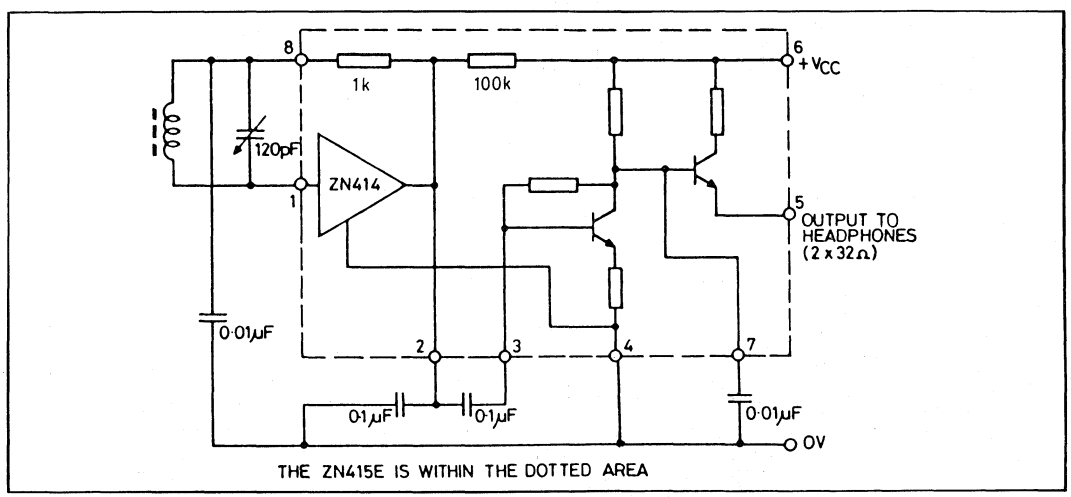
Similarly the ZN416E is a buffered output version of the ZN414Z giving typically 120mV (r.m.s.) output into a 64Ω load. The same package and pinning is used for the ZN416E as the ZN415E.

DEVICE SPECIFICATIONS $T_{amb} = 25°C$, $V_{CC} = 1.4V$. Parameters apply to all types unless otherwise stated.

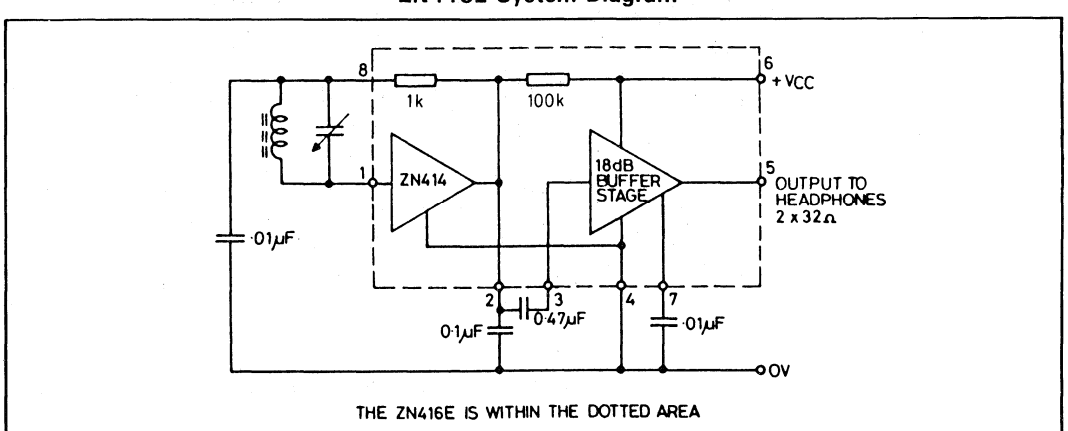
Parameter		Min.	Typ	Max.	Units
Supply voltage, V_{CC}		1.1	1.3	1.6	volts
Supply current, I_S with 64Ω headphones	ZN414Z	-	0.3	0.5	mA
	ZN415E		2.3	3	
	ZN416E		4	5	
Input frequency range		0.15	-	3.0	MHz
Input resistance		-	4.0	-	MΩ
Threshold sensitivity (Dependant on Q of coil)			50		μV
Selectivity		-	4.0	-	kHz
Total harmonic distortion		-	3.0	-	%
AGC range		-	20	-	dB
Power gain (ZN414Z)			72		dB
Voltage gain of output stage	ZN415E	-	6	-	dB
	ZN416E		18		
Output voltage into 64Ω load before clipping	ZN414Z	-	60	-	mVpp
	ZN415E		120		
	ZN416E		340		
Upper cut-off frequency of output stage, No capacitor, (ZN415E and ZN416E)		20	-	-	kHz
With 0.01μF between pin 7 and 0V (ZN415E)		-	6	-	kHz
With 0.01μF between pin 7 and 0V (ZN416E)		-	10	-	kHz
Lower cut-off frequency of output stage 0.1μF between pins 2 and 3 for ZN415E 0.47μF between pins 2 and 3 for ZN416E		-	50	-	Hz
Quiescent output voltage	ZN414Z	-	40	-	mV
	ZN415E		80		
	ZN416E		200		
Operating temperature range		0	-	70	°C
Maximum storage temperature		−65	-	125	°C



ZN414Z System Diagram



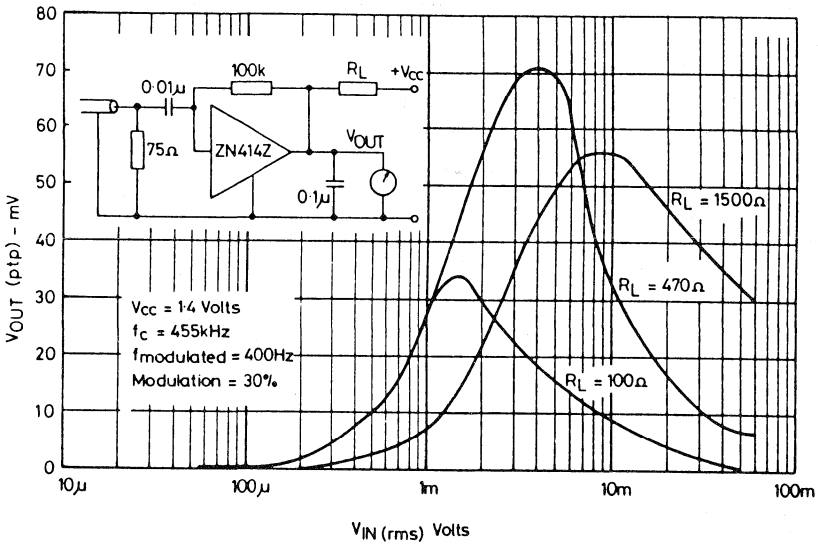
ZN415E System Diagram



ZN416E System Diagram

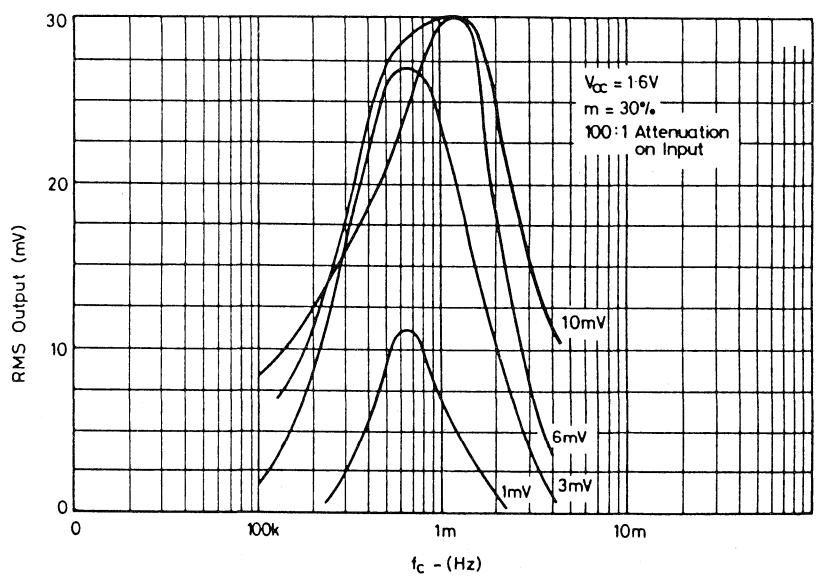
ZN414Z CHARACTERISTICS – All measurements performed with 30% modulation, $F_M = 400Hz$

Gain and AGC characteristics



See operating notes for explanation of AGC action.

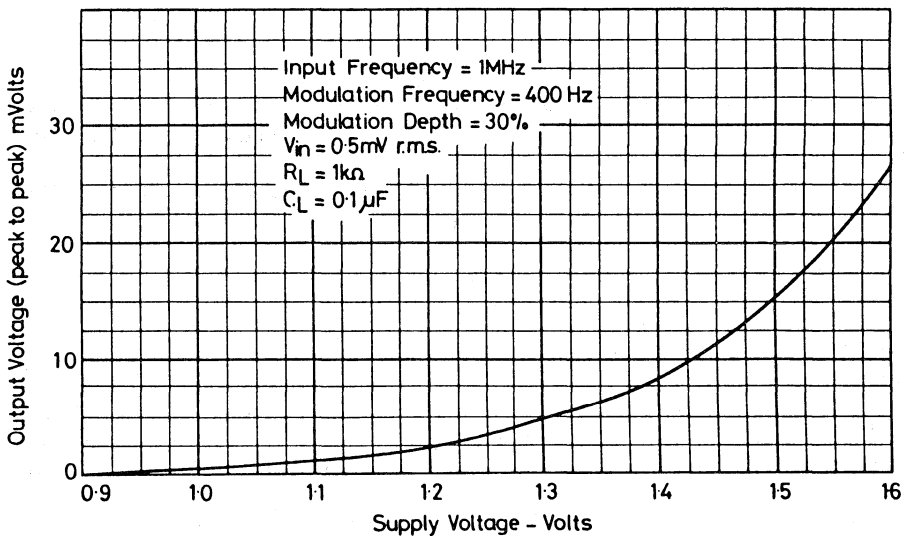
Frequency response of the ZN414Z



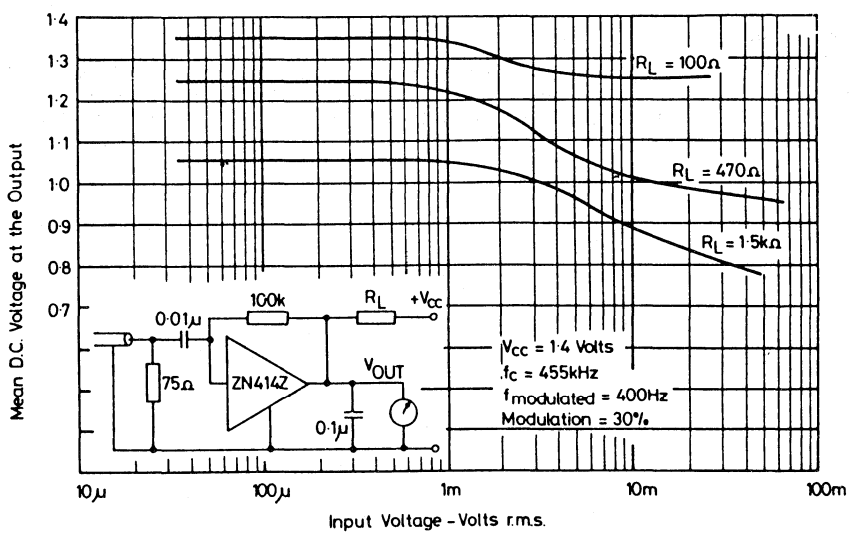
Note that this graph represents the chip response, and not the receiver bandwidth.

ZN414Z CHARACTERISTICS – *(Continued)*

Gain variation with supply volts.



D.C. level at output



LAYOUT REQUIREMENTS

As with any high gain R.F. device, certain basic layout rules must be adhered to if stable and reliable operation is to be obtained. These are listed below:

1. The output decoupling capacitor should be soldered as near as possible to the output and earth leads of the ZN414Z. Furthermore, its value together with the AGC resistor (R_{AGC}) should be calculated at $\approx$4kHz, i.e.:

$$C \text{ (farads)} = \frac{1}{2\pi \cdot R_{AGC} \cdot 4 \cdot 10^3}$$

2. All leads should be kept as short as possible, especially those in close proximity to the ZN414Z.
3. The tuning assembly should be some distance from the battery, loudspeaker and their associated leads.
4. The 'earthy' side of the tuning capacitor should be connected to the junction of the 100kΩ resistor and the 0.01μF capacitor.

OPERATING NOTES

(a) Selectivity

To obtain good selectivity, essential with any T.R.F. device, the ZN414Z must be fed from an efficient, high 'Q' coil and capacitor tuning network. With suitable components the selectivity is comparable to superhet designs, except that a very strong signal in proximity to the receiver may swamp the device unless the ferrite rod aerial is rotated to "null-out" the strong signal.

Two other factors affect the apparent selectivity of the device. Firstly, the gain of the ZN414Z is voltage sensitive (see previous page) so that, in strong signal areas, less supply voltage will be needed to obtain correct AGC action. Incorrect adjustment of the AGC causes a strong station to occupy a much wider bandwidth than necessary and in extreme cases can cause the RF stages to saturate before the AGC can limit RF gain. This gives the effect of swamping together with reduced AF output. All the above factors have to be considered if optimum performance is to be obtained.

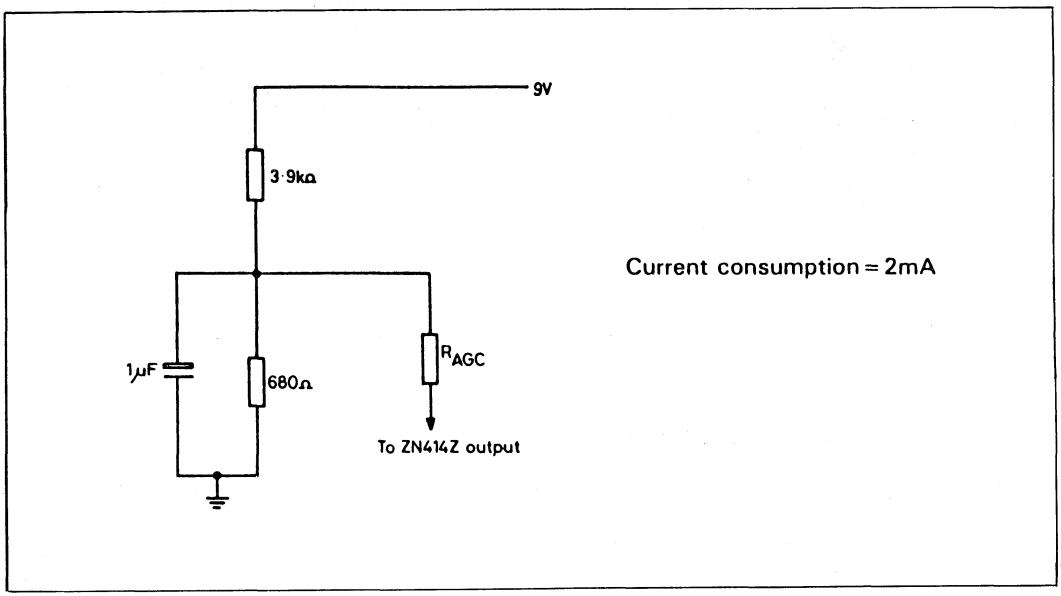
(b) Ferrite aerial size

Because of the gain variation available by altering supply voltage, the size of the ferrite rod is relatively unimportant. However, the ratio of aerial rod length to diameter should ideally be large to give the receiver better directional properties. Successful receivers have been constructed with ferrite rod aerials of 4cm (1.5") and up to 20cm (8").

DRIVE CIRCUITS

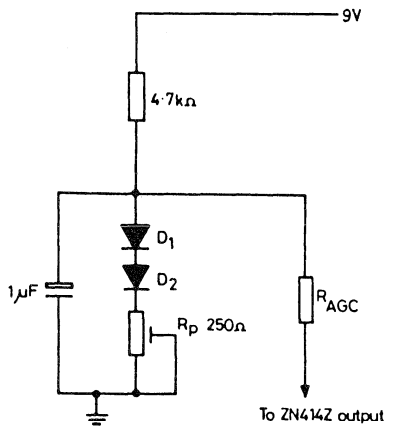
Three types of drive circuit are shown, each has been used successfully. The choice is largely an economic one, but circuit 3 is recommended wherever possible, having several advantages over the other circuits. Values for 9V supplies are shown, simple calculations will give values for other supplies.

1. Resistive Divider (ZN414Z)



Note: Replacing the 680Ω resistor with a 500Ω resistor and a 250Ω preset, sensitivity may be adjusted and will enable optimum reception to be realised under most conditions.

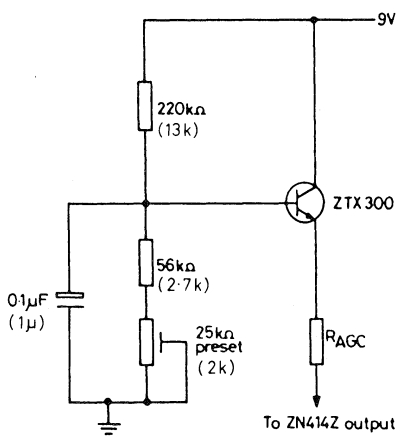
2. Diode Drive (ZN414Z)



$D_1 = D_2$ = Any general purpose silicon diode
R_p = Optional sensitivity control, a recommended value being 250Ω.

Current consumption ≈ 1.5mA

3. Transistor Drive (ZN414Z and ZN415E)

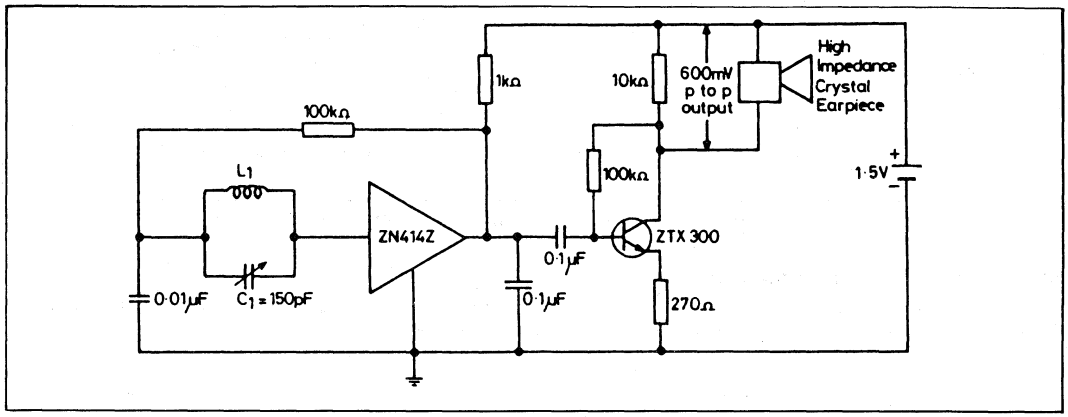


Current consumption is virtually that which is taken by the ZN414Z (0.3mA) or the ZN415E (2.3mA).
Component values shown in brackets are for the ZN415E.

RECOMMENDED CIRCUITS

(a) Earphone radio

The ZN414Z will drive a sensitive earpiece directly. In this case, an earpiece of equivalent impedance to R_{AGC} is substituted for R_{AGC} in the basic tuner circuit. Unfortunately, the cost of a sensitive earpiece is high, and unless an ultra-miniature radio is wanted, it is considerably cheaper to use a low cost crystal earpiece and add a single gain stage. One further advantage of this technique is that provision for a volume control can be made. A suitable circuit is shown below.

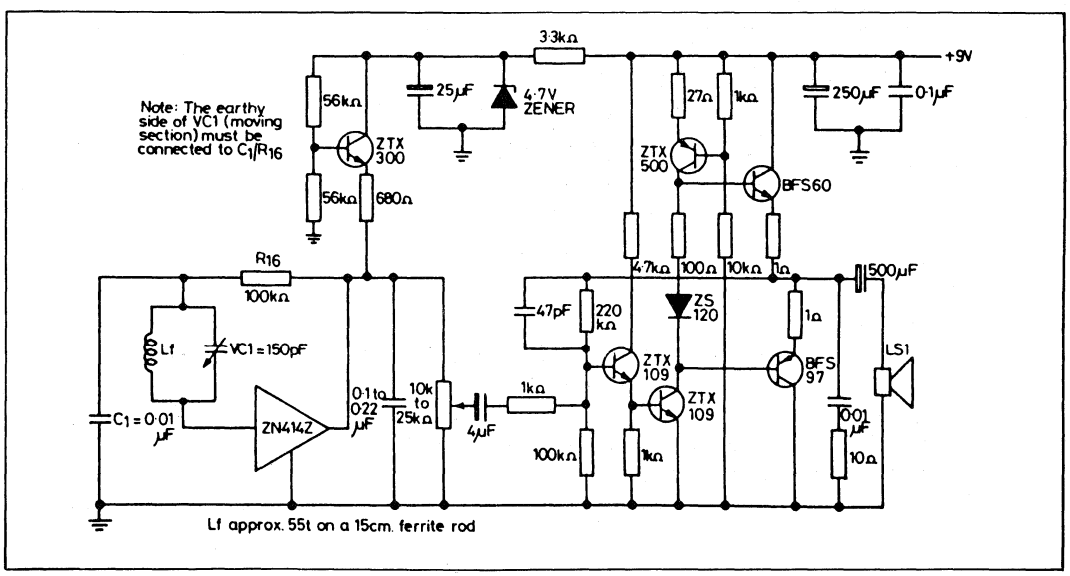


$L_1 \approx 80$ turns of 0.3mm dia. enamelled copper wire on a 5cm or 7.5cm long ferrite rod. Do not expect to adhere rigidly to the coil-capacitor details given. Any value of L_1 and C_1 which will give a high 'Q' at the desired frequency may be used.

Volume Control: a 250Ω potentiometer in series with a 100Ω fixed resistor substituted for the 270Ω emitter resistor provides an effective volume control.

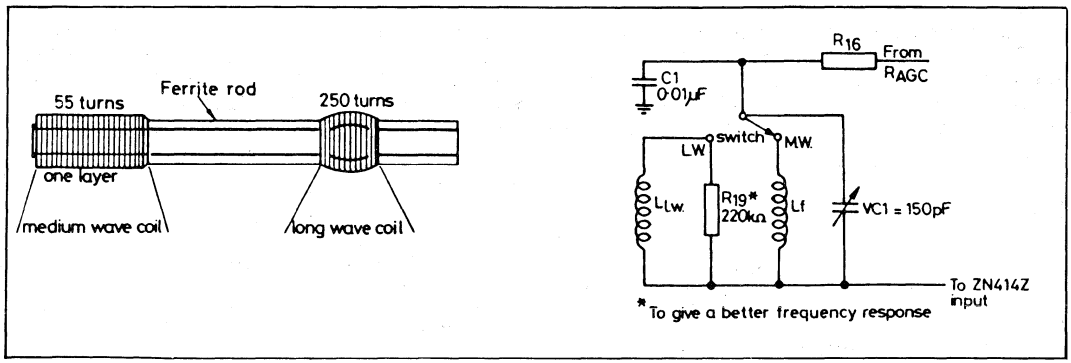
(b) Domestic portable receiver

The circuit shown is capable of excellent quality, and its cost relative to conventional designs is much lower.



The complete circuit diagram of the Triffid receiver

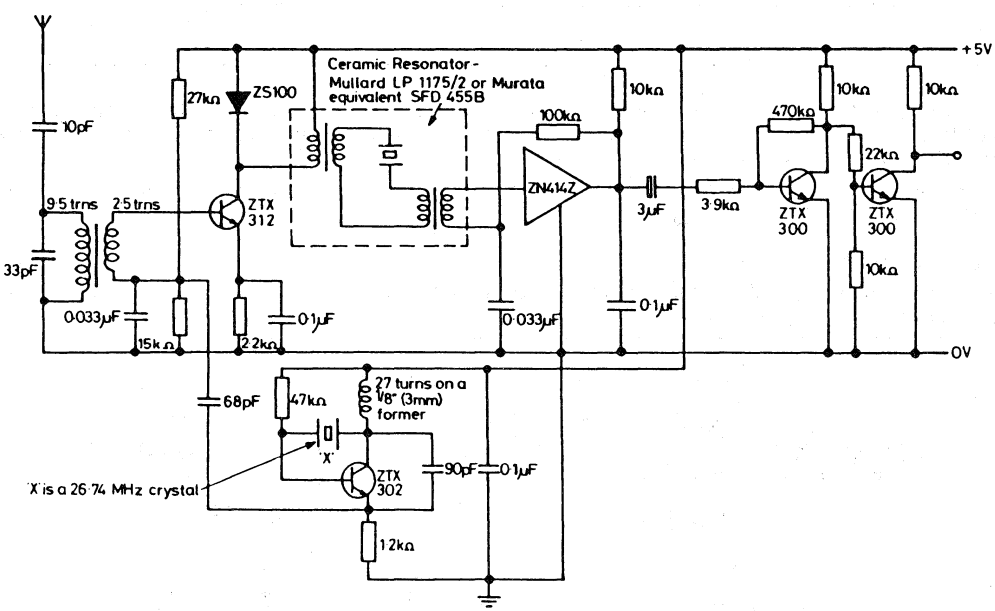
(b)i



Coil winding details and waveband selection

(c) Use in model control receiver

The circuit below shows a ZN414Z used as an I.F. amplifier for a 27MHz superhet receiver.



Performance Details:

Sensitivity = 2.5μV for a 5V p.t.p. output measured at f_C = 27.21MHz, 100% modulated with 100Hz square wave.

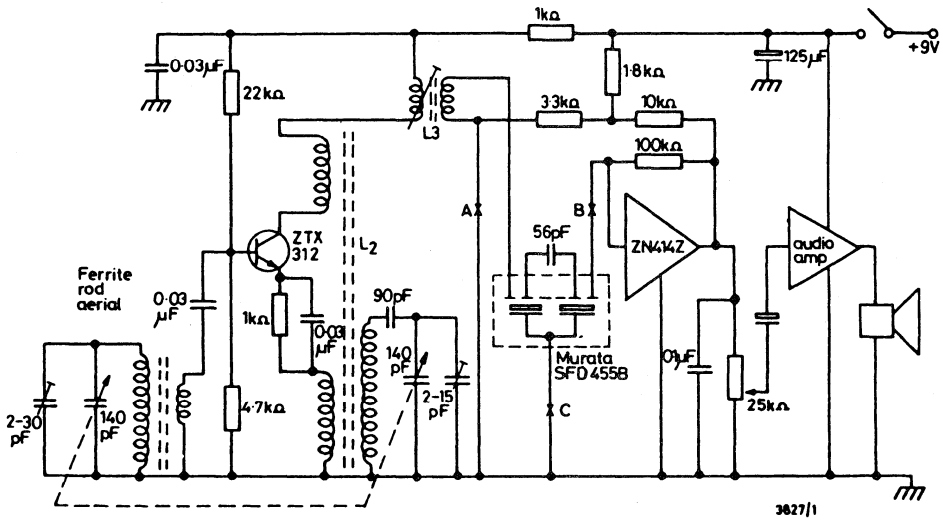
Selectivity: ±5kHz for <100mV p.t.p. output.

Input Signal Range: 2.5μV to 25mV (i.e. 80dB)

Supply Current: ≈4.5mA.

(d) Broadcast band superhet using ZN414Z

The ZN414Z coupled with the modern ceramic resonators offers a very good I.F. amplifier at modest cost, whilst maintaining simplicity and minimal alignment requirements. A typical circuit is shown below:



– 6dB Bandwidth = 6kHz
– 30dB Bandwidth = 8kHz
AGC Range ≈ 40dB
(For 10dB change in A.F. output).

FURTHER APPLICATIONS

The ZN414Z is an extremely versatile device and, in a data sheet, it is not possible to show all its varied applications. A comprehensive applications note on the device is available which gives full details of various radio receivers, I.F. amplifiers and frequency standards together with comprehensive technical information.

Section 2

Technical Data: Frequency synthesisers

MIL-STD-883C Class B

Many of the integrated circuits detailed in this section are available screened in conformance with MIL-STD-883C Class B and are identified in their ordering codes by the letters **AC** immediately following the device type number. Separate data sheets for these circuits are available from your local GEC Plessey Semiconductors Sales Office.

SP8853

1.3 / 1.5 GHz LOW POWER SINGLE-CHIP FREQUENCY SYNTHESISER

(Supersedes September 1990 Edition)

The SP8853 is a low power single chip synthesiser intended for professional radio applications, and contains all the elements (apart from the loop amplifier) to fabricate a PLL frequency synthesis loop.

The device is serially programmable by a three wire data highway and contains three independent buffers to store one reference divider word and two local oscillator divider words. A digital comparator, with two charge pumps, programmable in phase and gain are provided to improve lock up performance. The preset tandem operation of the charge pumps can be overwritten or the comparison frequencies switched to output ports under control of the divider word. The dual modulus ratio and so operating range is also programmable through the same word.

A power down mode is incorporated as a battery economy feature.

The part is specified to 1.5GHz at +85°C and to 1.3GHz at +125°C in the DG package. In the HC package the part is specified to 1.3GHz at +85°C and +125°C.

FEATURES

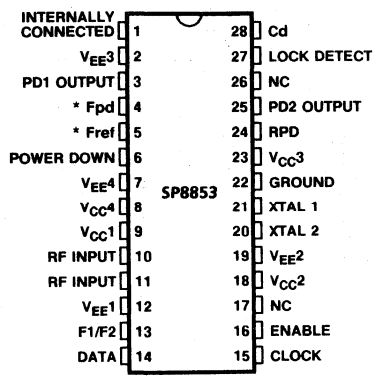
- Improved Digital Phase Detector to Eliminate 'Dead Band' Effects
- Low Operating Power, Typically 175mW
- 1.5GHz Operating Frequency (DG package)
- Complete Phase Locked Loop
- High Input Sensitivity
- Programmed through Three Wire Data Bus
- Wide Range of Reference Division Ratios
- Local Storage for Two Frequency Words giving Rapid Frequency Toggling
- Programmable Phase Detector Gain
- Power Down Mode
- ESD Protection on all Pins

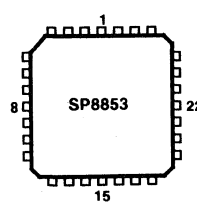
ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.3V to 7V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C
Prescaler input voltage	2.5V p-p

ORDERING INFORMATION

SP8853 A DG
SP8853 B DG
SP8853 A HC
SP8853 B HC
SP8853 AC DG
SP8853 AC HC





1	IC	15	CLOCK
2	$V_{EE}3$	16	ENABLE
3	PD1 OUTPUT	17	NC
4	* Fpd	18	$V_{CC}2$
5	* Fref	19	$V_{EE}2$
6	POWER DOWN	20	XTAL 2
7	$V_{EE}4$	21	XTAL 1
8	$V_{CC}4$	22	GROUND
9	$V_{CC}1$	23	$V_{CC}3$
10	RF INPUT	24	RPD
11	RF INPUT	25	PD2 OUTPUT
12	VEE1	26	NC
13	F1/F2	27	LOCK DETECT
14	DATA	28	Cd

* Fpd and Fref outputs are reversed by the phase detector sense bit in the programming word. Diagram above is correct when sense bit is low.

$V_{CC}1$, $V_{EE}1$ - Preamp and Prescaler
$V_{CC}2$, $V_{EE}2$ - Oscillator Supplies
$V_{CC}3$, $V_{EE}3$ - Charge Pump 2 Supplies
$V_{CC}4$, $V_{EE}4$ - ECL Supplies

Fig.1 Pin connections-top view

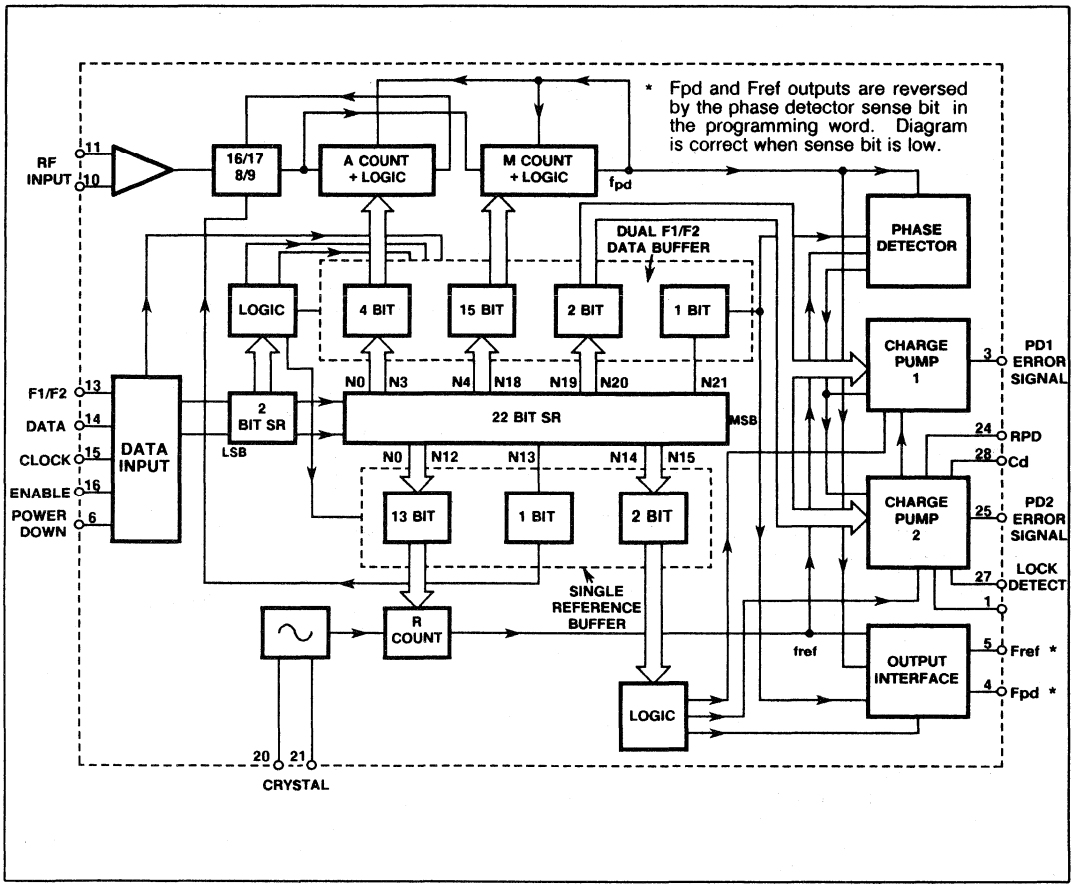


Fig. 2 SP8853 block diagram

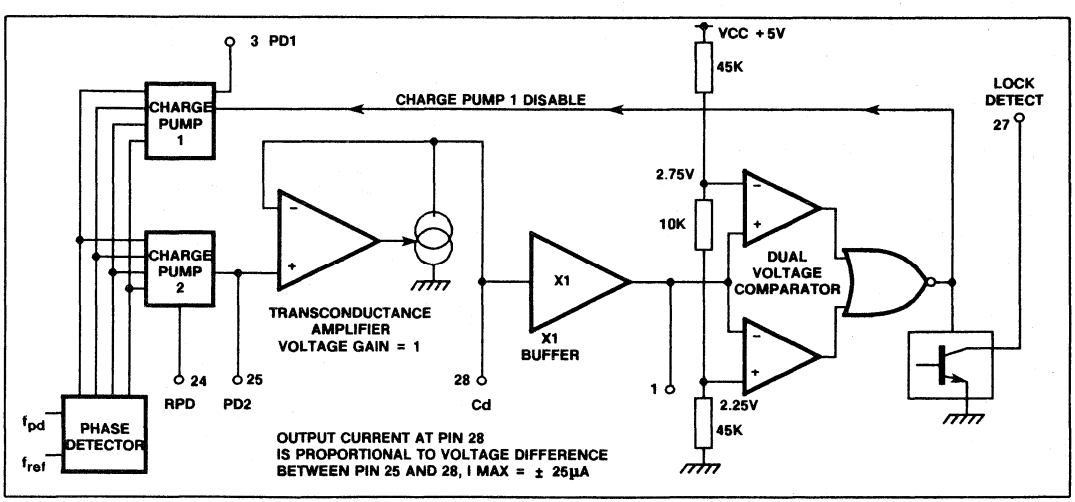


Fig. 3 Detailed Block Diagram of Lock Detect Circuit

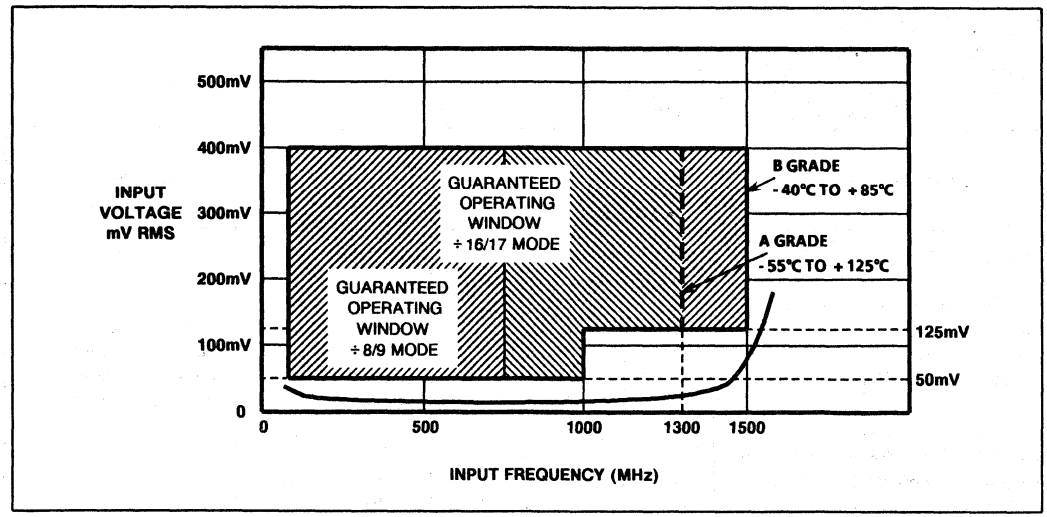


Fig. 4a Typical input characteristics and input drive requirements (DG package)

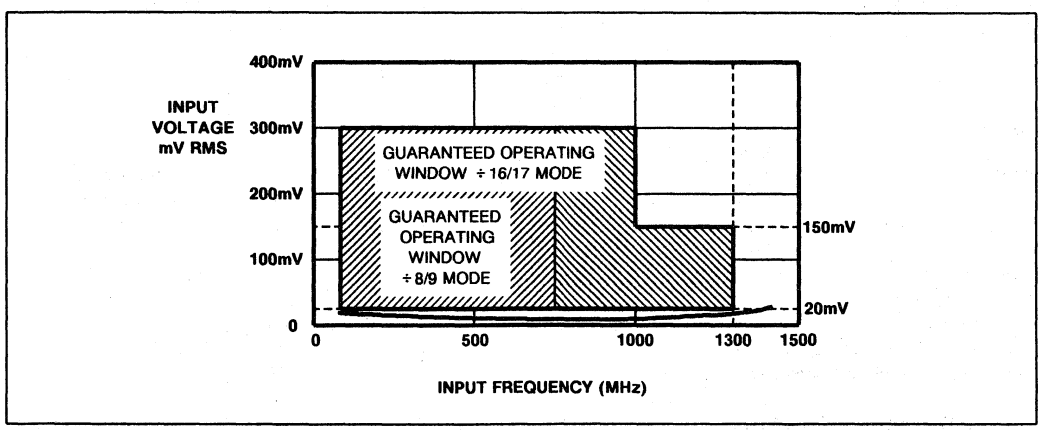


Fig. 4b Typical input characteristics and input drive requirements (HG package)

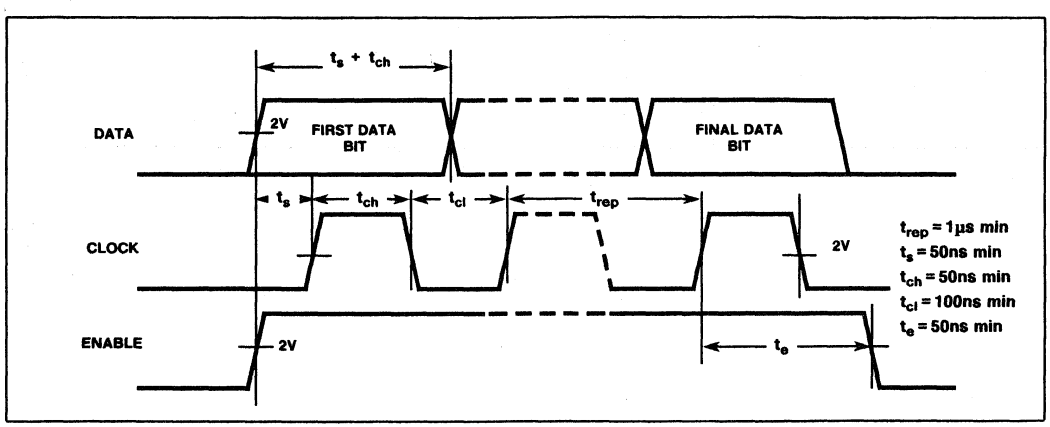


Fig. 5 Data and clock timing requirements

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = +4.75V to +5.25V
Temperature: A Grade T_{amb} = -55°C to + 125°C
B Grade T_{amb} = -40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	8,9					
	18,23		33	40	mA	
Supply Current in Power Down Mode	8		4.5	6	mA	
Input Sensitivity	10,11					See Figs. 4a and b
Input Overload	10,11					See Figs. 4a and b
RF Input Division Ratio	10,11,4	256		524287		With 16/17 selected
		56		262143		With 8/9 selected
Comparison Frequency	4,5			5	MHz	
Reference Oscillator Input Frequency	20,21	4		20	MHz	
External Reference Input Voltage	20	10		500	mVrms	
Reference Division Ratio	20,5	1		8191		
Data Clock Repetition Rate t_{rep}	15			1	μs	See Fig. 5
Minimum Set up Time t_s	14,15	50			ns	See Fig. 5
Data Input High	14	0.6Vcc		Vcc	V	
Low	14	Vee		0.3Vcc	V	
Clock Input High	15	0.6Vcc		Vcc	V	
Low	15	Vee		0.3Vcc	V	
Data Enable High	16	0.6Vcc		Vcc	V	
Low	16	Vee		0.3Vcc	V	
F1/F2 Input High	13	0.6Vcc		Vcc	V	F1 buffer selected
Low	13	Vee		0.3Vcc	V	F2 buffer selected
Power Down Input High	6	0.6Vcc		0.9Vcc	V	
Low	6	Vee		0.3Vcc	V	
F1/F2 Input Current	13			5	μA	V Pin 13 = 5.0V
Power Down Input Current	6			5	μA	v Pin 6 = 4.5V
RPD External Resistance	24	68		330	kΩ	
Lock Detect Output Voltage 'in lock'	27			1	V	I pin 27 = 1mA
Lock Detect Switching Voltage High	25	2.7			V	Vcc = 5V
Low	25			2.3	V	Vcc = 5V
Fpd and Fref Output Voltage Swing			0.9		V	Vcc = 5V. External pull down may be required

DESCRIPTION

Prescaler and A M counter

The programmable divider chain is of A M counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi-modulus division. A programmable divider of this construction has a division ratio of MN + A and a minimum integer steppable division ratio of N(N-1).

In the SP8853 the dual modulus front end prescaler is a dual N ratio device capable of being statically switched between 16/17 and 8/9 ratios. The controlling A counter is of four bit design enabling a maximum count sequence of 15, (2^4-1) which begins with the start of the M counter sequence and stops when it has counted by the preloaded number of cycles. Whilst the A counter is counting the dual modulus prescaler is held in the N + 1 mode, then relaxes back to the N mode at the completion of the sequence. The M counter is a 15-bit asynchronous divider which counts with a ratio set by a control word. In both A and M counters the controlling data from the F1/F2 buffer is loaded in sequence with every M count cycle. The N ratio of the dual modulus prescaler is selected by a one bit word in the reference divider buffer and, when a ratio of 8/9 is selected the A counter requires only three programming bits, having an impact on the frequency bit allocation as described in the data entry section.

Reference source and divider

The reference source in the SP8853 is obtained from an on board oscillator, frequency controlled by an external crystal. The oscillator can also function as a buffer amplifier allowing the use of an external reference source. In this mode the source is simply AC coupled into the oscillator transistor base on pin 20.

The oscillator output is coupled to a programmable reference divider whose output is the reference for the phase detector. The reference divider is a fully programmable 13-bit asynchronous design and can be set to any division ratio between 1 and 8191. The actual division ratio is controlled by a data word stored in the internal reference buffer.

Phase comparator

The SP8853 is provided with a digital phase comparator feeding two charge pump circuits. Charge pump 1 has preset currents programmable as shown in table 1. Charge pump 2 has a current level set by an external resistor: the current is multiplied by a factor determined by the F1 or F2 word (see table 1).

A lock detect circuit is connected to the output of charge pump 2. When the voltage level at pin 25 is between approximately 2.25 and 2.75 volts, pin 27 will be low and charge pump 1 disabled depending on the PD1 and PD2 programming bits as shown in table 4.

The output signals from the reference and M counters are available on pins 4 and 5 when programmed by the reference programming word: the various options are shown in table 4. An external phase detector may be connected to pins 4 and 5 and may be used independently or in conjunction with the on chip detector.

To allow for control direction changes introduced by the design of the control loop, a programming bit in the F1/F2 programming word interchanges the inputs to the on chip phase detector and reverses the functions on pins 4 and 5.

F1 OR F2 WORD G2	G1	CHARGE PUMP 1 CURRENT	CHARGE PUMP 2 MULTIPLIER
0	0	50µA	1
1	0	75µA	1.5
0	1	125µA	2.5
1	1	200µA	4

Table 1 Charge pump currents

Note: ***Charge pump 2*** *is pin 24 current × multiplication factor.* $I_{pin\ 24} = \frac{VCC-1.5V}{RPD}$

Data entry and storage

The data section of the SP8853 consists of a data input interface, an internal data shift register and three internal data buffers.

Data is entered to the data input interface by a three wire data highway with data, clock and chip enable inputs. The input interface then routes this data to a 24-bit shift register with bus connections to three data buffers. Data entered via the serial bus is transfered to the appropriate data buffer on the negative transition of the chip enable input according to the two final data bits as shown in Table 3. The MSB of the data is entered first.

The dual F1/F2 buffer can receive two 22-bit words and controls the programmable divider A and M counters using 19-bits, the phase detector gain with two bits and the phase detector sense with one bit. A fourth input from the synthesiser control system selects the active buffer.

OUTPUT FOR RF PHASE LAG	
Sense Bit	Pins 3 and 25
0	Current source
1	Current sink

Table 2

The third buffer contains only 16 bits, 13 being used to set the reference counter division ratio, and 2 to control the phase comparator enable logic. The remaining bit sets the dual modulus prescaler N ratio.

2 Bit S.R. Contents	Buffer Loaded
00	F1
10	F2
01	Active A *
11	Reference

Table 3

** Transfer of A counter bits into buffer controlling the programmable counter*

The data words may be entered in any individual multiple sequence and the shift register can be updated whilst the data buffers retain control of the synthesiser with the previously loaded data. This enables four unique data words to be stored in the device, with three in the data buffers and a fourth in the shift register, whilst the chip is enabled. F1 word may also be updated whilst F2 is controlling the programmable divider and vice versa.

The dual F1/F2 buffer enables the device to be toggled between two frequencies using the F1/F2 select input at a rate determined by the comparasion frequency

and also enables random frequency hopping at a rate determined by a byte load period, since the loop can be locked to F1 whilst F2 is updated by entering new data via the shift register. The F1/F2 input is high to select F1.

An F1 or F2 update cycle will consist of a byte containing 24 bits, whereas the reference byte will contain 18 bits. The device requires 3 bytes, each with a chip select sequence, totalling 66 bits to fully program.

When the dual modulus counter (A count) is set to ÷8/9, the data required to set the counter is reduced by one bit, leaving an unused bit in the 22-bit' F1/F2 buffer. this bit must always be set to zero when ÷8/9 mode is required. Various programming sequences are shown in Fig. 7

The data entry and storage registers are always powered up, making it possible to enter data when the device is in the powered down state.

PD2	PD1	
0	0	Fref and Fpd outputs off, charge pump 1 and 2 on
0	1	Fref and Fpd outputs on, charge pump 1 off. Charge pump 2 on
1	0	Fref and Fpd outputs off, charge pump 1 disabled by lock detect. Charge pump 2 on
1	1	Fref and Fpd outputs on, charge pump 1 disabled by lock detect. Charge pump 2 on

Table 4

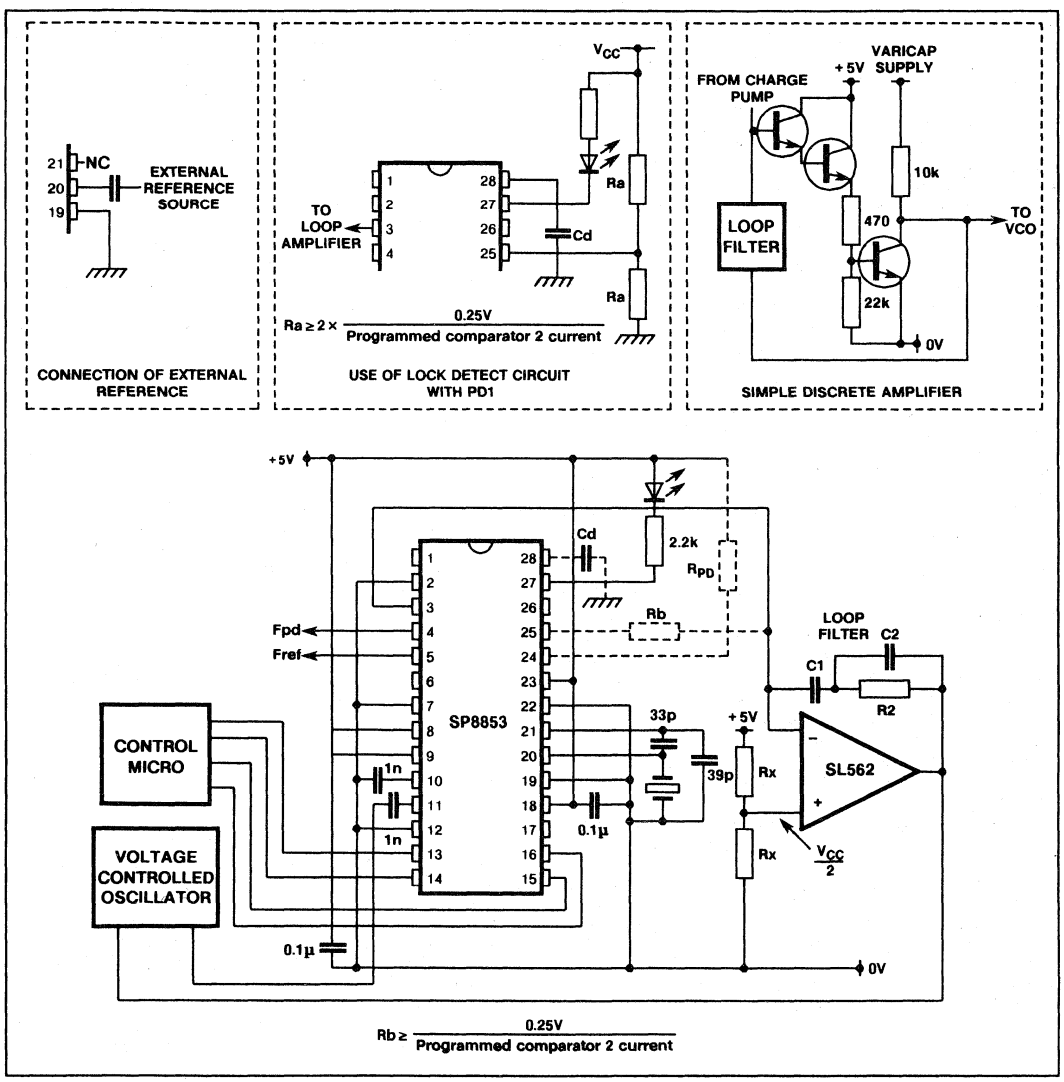


Fig. 6 Typical application diagram

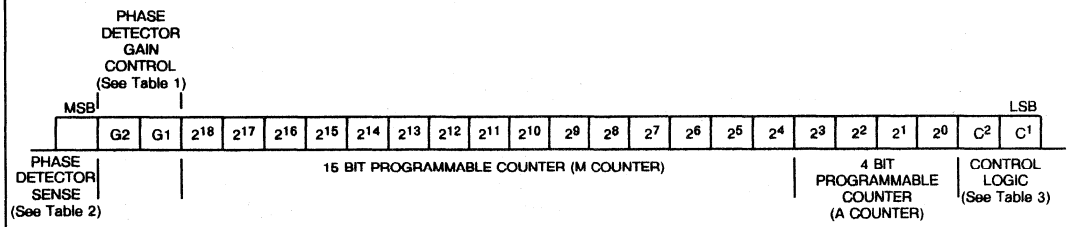


FIG.7(a) F1 or F2 word, bit allocation with 16/17 selected

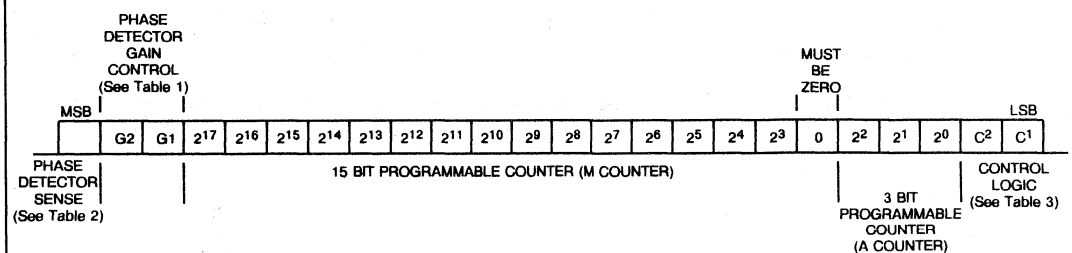


FIG.7(b) F1 or F2 word, bit allocation with 8/9 selected

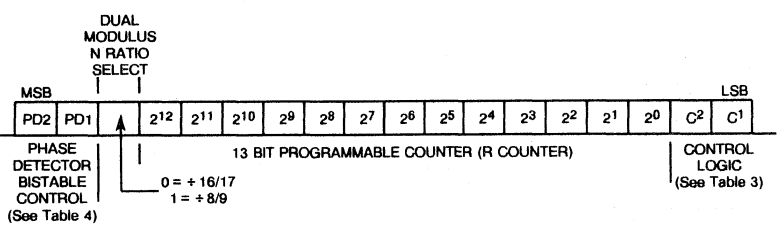


FIG.7(c) reference word bit allocation

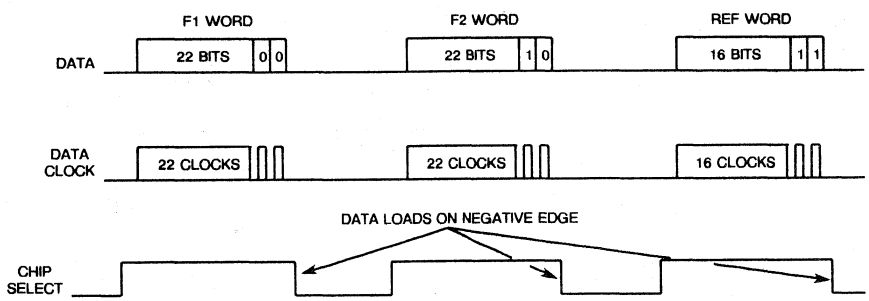


Fig.7(d) Typical data load sequence

Fig. 7 Data format diagrams

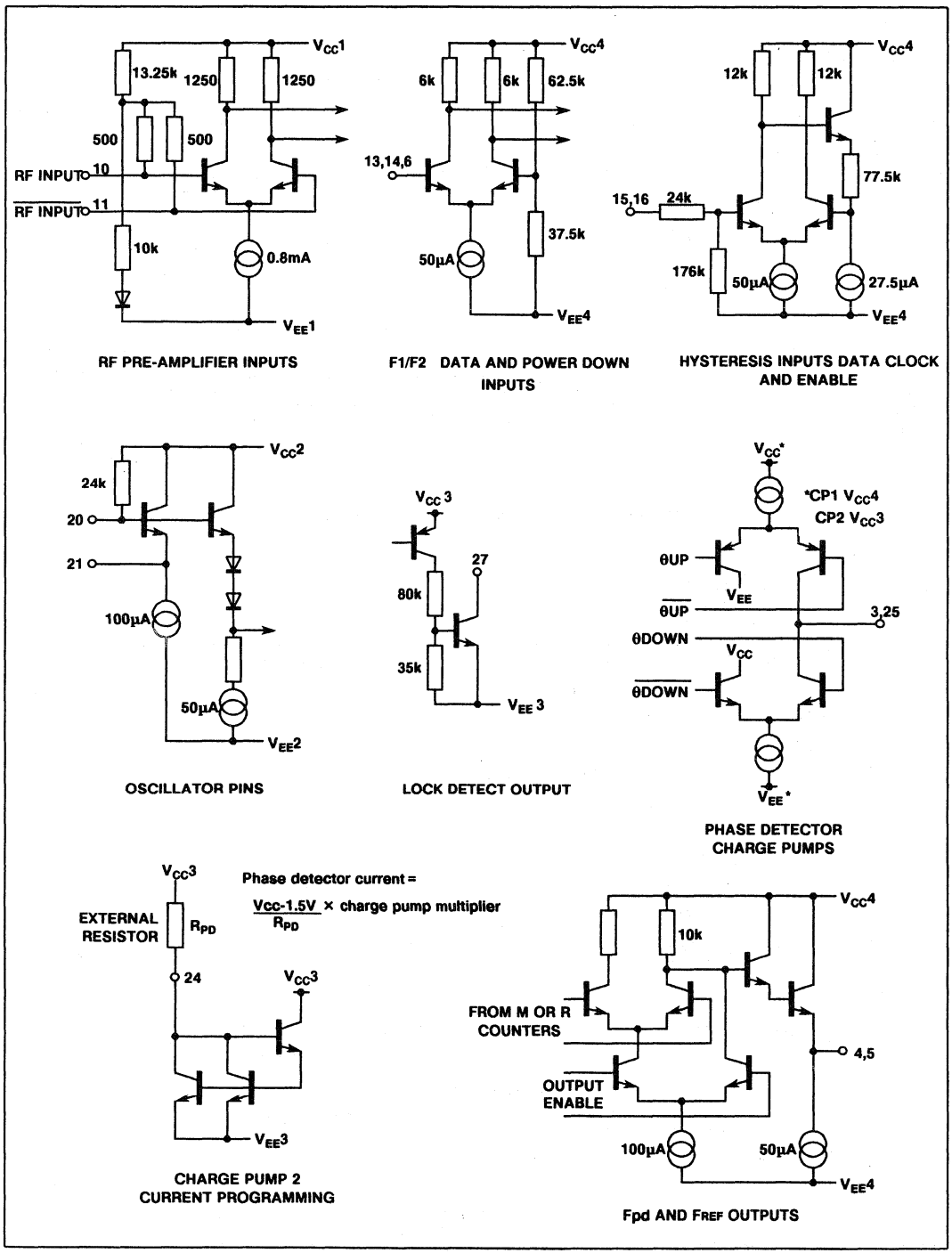


Fig. 8 Input and output interface diagrams

APPLICATIONS

A basic application using a single phase comparator is shown in Fig.6. The SP8853 is a 1.5 GHz part, so good RF design techniques should be employed, including the use of a ground plane and suitable high frequency capacitors at the RF input and for power supply decoupling.

The RF input should be coupled to either pin 10 or 11, and the other pin decoupled to ground. The reference oscillator is of conventional Colpitts type with two capacitors required to provide a low impedance tap for the feedback signal to the transistor emitter. Typical values are shown in Fig.6, although these may be varied to suit the loading requirements of particular crystals. Where a suitable reference signal already exists or where a very stable source is required, it is possible to apply an external reference as shown inset in Fig.6. The amplitude should be kept below 0.5V RMS to avoid forward biasing the transistor collector-base junction.

In some systems, it is useful to have an indication of phase lock. The output from pin 27 goes low when the output of charge pump 2 is between 2.25 and 2.75V and can be used to operate an LED to give visual indication of phase lock. Alternatively a pull-up resistor may be connected to V_{CC} and the output used to signal to the control microprocessor that the loop is locked, thus speeding up system operation. The output current available from pin 27 is limited to 1.5mA. If this current is exceeded the logic low level will be uncertain.

The circuit diagram shown in Fig.6 is a basic application with minimum component count which is nevertheless perfectly adequate for many applications. Charge pump 1 on pin 3 is used to drive the loop amplifier, which provides the control voltage for the local oscillator. When charge pump 1 is used in this mode, the PD1 and PD2 bits in the reference programming word must be set to enable charge pump 1 continuously. This application could also use charge pump 2 output on pin 25 or, if a higher phase comparator gain is required, pins 3 and 25 could be connected in parallel to use the combined output current from both charge pumps.

The lock detect circuit can be programmed to disable charge pump 1 automatically as shown in Table 4. This feature can be used to reduce the system lock up time by connecting the charge pump outputs in parallel to the loop amplifier with a resistor, Rb, in series with charge pump 2. This connection allows a relatively high current to be used from charge pump 1 to give short lock up time, and a low current to be set on charge pump 2 giving low reference frequency sidebands. The degree of lock up time improvement depends on the ratio of charge pump 1 to charge pump 2 currents.

When the loop is out of lock, both charge pumps will be enabled and will feed current to the loop amplifier to bring the oscillator to phase lock. The current from charge pump 2 will produce a voltage drop across Rb, allowing operation of the lock detect circuit and enabling charge pump 1. The resistor must be chosen to give a voltage drop greater than 0.25V at the current level programmed for charge pump 2. When phase lock is achieved, there will be no charge pump current and therefore the voltage at pin 25 will be equal to that on the virtual earth point of the loop amplifier (2.5V), disabling charge pump 1.

Charge pump 1 should not be left open circuit when enabled as this prevents correct operation of the phase detector. The output on pin 3 should be biased to half supply with a pair of 4.7kΩ resistors connected between supplies.

When charge pump 2 is used to drive the loop amplifier, the lock detect circuit will only give an out of lock indication when large frequency changes are made or when a frequency outside the range of the local oscillator is programmed. At other times the loop amplifier input is maintained at 2.5V by the action of the loop filter components. Again, resistor Rb connected between pin 25 and the loop amplifier, producing a voltage drop greater than 0.25V at the charge pump current programmed, will allow sensitive out of lock detection.

When phase lock detection is required using comparator 1 only (see inset Fig.6), charge pump 2 output (pin 25) should be biased to 2.5V using two equal value resistors, Ra, across the supply. The values should be chosen to give a voltage change greater than 0.25V at the programmed comparator 2 charge pump current. A small capacitor, Cd, connected from pin 28 to ground may be used to reduce chatter at the lock detect output. A detailed block diagram showing the lock detect circuit is shown in Fig 3.

An amplifier is required to convert the current pulses from the phase comparator into a voltage of suitable magnitude to drive the chosen VCO. The choice of amplifier must be determined by the voltage swing required at the VCO to achieve the necessary frequency range, and in most cases an operational amplifier will be used to provide the essential characteristics of high input impedance, high gain and low output impedance required in this application.

Although it is expected that an operational amplifier will be used in most cases, a simple discrete design can be used and a suitable design is shown inset in Fig.6. This arrangement can be particularly useful when the minimum VCO control voltage must be close to ground and where negative supplies are inconvenient. This form of amplifier is not suitable for use with charge pump 2 when the lock detect circuit is required.

When an operational amplifier is used in the inverting configuration shown in Fig.6, the charge pump output is connected directly to the virtual earth point and will therefore operate at a voltage similar to that set on the non-inverting input. Normally this operating point should be set at half supply using a potentiometer of two equal resistors, Rx, but if necessary this voltage can be set up to 1V higher or lower than half supply without detrimental effect. When the lock detect function is required on charge pump 2, the non inverting input must be at half supply.

The digital phase comparator and charge pump used on the SP8853 produces bi-directional current pulses in order to correct errors between the reference and VCO divider outputs. Once synchronisation is achieved, in theory no further output from the charge pump should be required, but in practice, due to leakage currents and particularly the input current of the amplifier, the capacitors forming the loop filter around the amplifier will gradually discharge, modifying the VCO voltage and requiring further outputs from the charge pump to restore the charge. The effect of this continuous correction of the local oscillator frequency is to frequency-modulate the VCO and thus produce sidebands at the reference frequency. In order to reduce this effect to a minimum, an amplifier with low input bias current is essential.

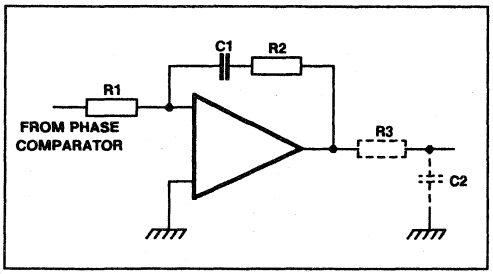


Fig. 9 Standard Form of Second Order Loop Filter

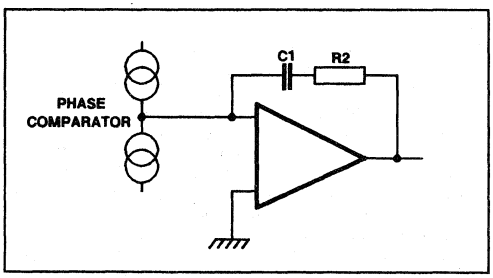


Fig.10 Modified Second Order Loop Filter

Loop calculations

Many frequency synthesiser designs use a second order loop with a loop filter of the form shown in Fig.9.

In practice an additional RC time constant (shown dotted in Fig.9) is often added to reduce noise from the amplifier. In addition any feedthrough capacitor or local decoupling at the VCO will be added to the value of C2. These additional components in fact form a third order loop, and if the values are chosen correctly, the additional filtering provided can considerably reduce the level of reference frequency sidebands and noise without adversly affecting the loop settling time. The calculation of values for both forms of loop is shown below.

Second Order Loop.

For this filter two equations are required to determine the time constants τ_1 and τ_2 where:

$$\tau_1 = C_1 R_1$$
$$\tau_2 = C_1 R_2$$

The equations are:

$$\tau_1 = \frac{K_\theta K_0}{\omega_n^2 N} \quad \ldots(1)$$

$$\tau_2 = \frac{2\zeta}{\omega_n} \quad \ldots(2)$$

where:

- K_θ is the phase detector gain factor in V/Radian
- K_0 is the VCO gain factor in radians second /Volt
- N is the division ratio from VCO to reference frequency
- ω_n is the natural loop bandwidth
- ζ is the damping factor: normaly 0.7071

The SP8853 phase comparator is a current source rather than a conventional voltage source and has a gain factor specified in µA/radian. Since the equations deal with a filter where R_1 is feeding the virtual earth point of an operational amplifier from a voltage source, R_1 sets the input current to the filter. This is similar to the circuit shown in Fig.10, where a current source phase comparator is connected directly to the virtual earth point of the operational amplifier.

The equivalent voltage gain of the phase comparator can be calculated by assuming a value for R_1 and calculating a gain in volts/radian which would produce the set current.

The digital phase comparator used in the SP8853 is linear over a range of 2π radians and therefore the phase comparator gain is given by:

$$\frac{\text{phase comparator current setting}}{2\pi} \text{ µA/Radian.}$$

The phase comparator gain in V/radian is therefore:

$$\frac{50\,\mu A}{2\pi} \times 1k\Omega$$

assuming a value of 1kΩ for R_1 and 50µA for the phase comparator current setting, these values can now be inserted in equation (1) to obtain values for C_1 and equation (2) used to determine a value for R_2.

Example:

Calculate values for a second order loop with the following parameters.

Frequency to be synthesised	800Mhz
Reference frequency	100kHz
Division ratio N	$\frac{800MHz}{100kHz}$ = 8000
Natural loop frequency ω_n	500Hz
VCO gain factor K_0	2π x 10MHz/Volt
Damping factor ζ	0.7071
Phase comparator current setting	50µA

Assuming R_1 is 1kΩ, then the equivalent phase comparator gain K_θ in V/radian $= \frac{50\mu A}{2\pi} \times 1000$

$$K_\theta = 0.00796 \text{V/radian.}$$

$$\text{From equation 1} \quad \tau_1 \frac{0.00796 \times 2 \times \pi \times 10MHz}{(2 \times \pi \times 500)^2 \times 8000}$$

$$\tau_1 = 6.334 \times 10^{-6}$$

$$\text{From equation 2} \quad \tau_2 = \frac{2 \times 0.7071}{2 \times \pi \times 500}$$

$$\tau_2 = 4.50 \times 10^{-4}$$

$$\text{Now} \quad \tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{6.334 \times 10^{-6}}{1k\Omega}$$

1K is chosen value for R_1

$$C_1 = 6.33nF$$

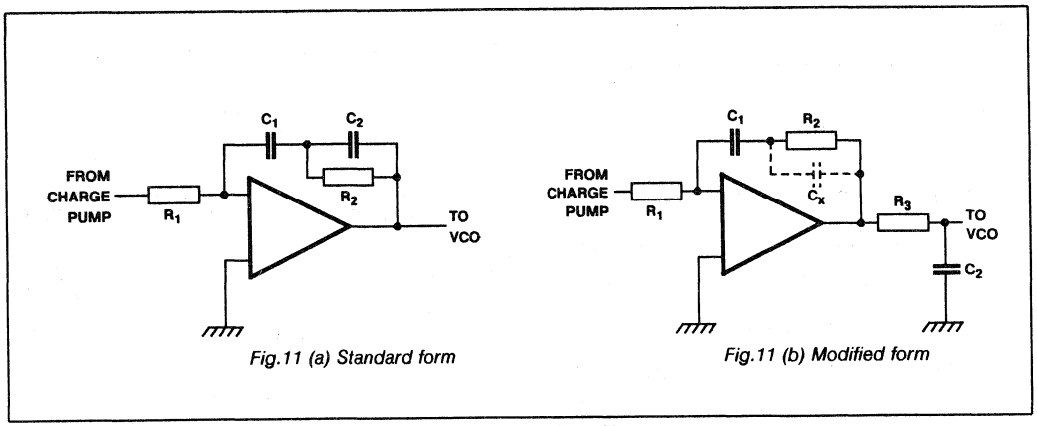


Fig.11 (a) Standard form

Fig.11 (b) Modified form

Fig.11 Third order loop filter

$$\tau_2 = C_1 R_2 \therefore \frac{4.50\times10^{-4}}{6.33\times10^{-9}} = R_2$$

$$R_2 = 71000\ \Omega$$

Third Order Loop

The third order loop filter is normally shown as in Fig.11a. Fig.11b shows the circuit redrawn to use an RC time constant after the amplifier, allowing any feedthrough capacitance on the VCO line to be included in the loop calculations. Where the modified form in Fig.11b is used it is advantageous to connect a small capacitor Cx of typically 100pF (shown dotted), across the amplifier to reduce sidebands caused by the amplifier being forced into non-linear operation by the phase comparator pulses.

Three equations are required to determine the time constants, τ_1, τ_2 and τ_3 where :

for Fig.11a:
$$\tau_1 = C_1 R_1$$
$$\tau_2 = R_2 (C_1 + C_2)$$
$$\tau_3 = C_2 R_2$$

and for Fig.11b:
$$\tau_1 = C_1 R_1$$
$$\tau_2 = C_1 R_2$$
$$\tau_3 = C_2 R_3$$

The equations are:

$$\tau_1 = \frac{K_\theta K_0}{N\omega_n^2}\left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]^{\frac{1}{2}} \quad \ldots(3)$$

$$\tau_2 = \frac{1}{\omega_n^2 \tau_3} \quad \ldots(4)$$

$$\tau_3 = \frac{-\tan\phi_0 + \frac{1}{\cos\phi_0}}{\omega_n} \quad \ldots(5)$$

Where:

K_θ is the phase detector gain factor in V/Radian
K_0 is the VCO gain factor in radians second/Volt
N is the total division ratio from VCO to reference frequency
ω_n is the natural loop bandwidth
ϕ_0 is the Phase margin normaly set to 45°

As in the second order filter example a value for R1 can be assumed and an equivalent gain K_θ in V/radian calculated from:

$$\frac{\text{phase comparator current setting } \mu\text{A/radian} \times 1\text{k}}{2\pi}$$

Where 1kΩ is the assumed value for R_1

These values can now be substituted in equation (3) to obtain a value for C_1 and equations (4) and (5) used to determine values for C_2 and R_2.

EXAMPLE

Calculate values for a loop with the following parameters.

Frequency to be synthesised:	800MHz
Reference frequency	100kHz
Division ratio	$\frac{800\text{MHz}}{100\text{kHz}} = 8000$
ω_n natural loop frequency	500Hz
K_0 VCO gain factor	2π x 10MHz/Volt
ϕ_0 phase margin	45°
Phase comparator current	50µA

assuming R_1 is 1kΩ, then the equivalent phase comparator gain K_θ in V/radian is:

$$\frac{50\mu A}{2\pi} \times 1000 = 0.00796 \text{ V/Radian}$$

From equation (3):

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{500\text{Hz} \times 2\pi} = \frac{0.4142}{3141.6}$$

$$\tau_3 = 1.318 \times 10^{-4}$$

From equation (4):

$$\tau_2 = \frac{1}{(500 \times 2 \times \pi)^2 \times 1.318 \times 10^{-4}}$$

$$\tau_2 = 7.687 \times 10^{-4}$$

Using these values in equation (3):

$$\tau_1 = \frac{7.96 \times 10^{-3} \times 2 \times \pi \times 10\text{MHz/V}}{8000 \times (2\pi \times 500)^2} \left[A\right]^{\frac{1}{4}}$$

Where A is:

$$\frac{1+\omega_n^2 \tau_2^2}{1+\omega_n^2 \tau_3^2} = \frac{1+(2\pi \times 500)^2 \times (7.687 \times 10^{-4})^2}{1+(2\pi \times 500)^2 \times (1.318 \times 10^{-4})^2}$$

$$\tau_1 = \frac{500141.6}{7.896 \times 10^{10}} \left[\frac{6.832}{1.1714}\right]^{\frac{1}{4}}$$

$$\tau_1 = 6.334 \times 10^{-6} \times 2.415$$

$$\tau_1 = 1.53 \times 10^{-5}$$

now $\tau_1 = C_1 R_1$

$$\therefore C_1 = \frac{1.53 \times 10^{-5}}{1\text{k}\Omega} \quad (R_1 \text{ is chosen as } 1\text{k}\Omega)$$

$$C_1 = 0.0153\mu\text{F}$$

for Fig.11a: $\tau_2 = R_2 (C_1 + C_2)$

for Fig.11b: $\tau_3 = C_2 R_2$

substituting for C_2

$$\tau_2 = R_2 \left[C_1 + \frac{\tau_3}{R_2}\right] \quad \therefore \tau_2 = R_2 C_1 + \tau_3$$

$$\therefore R_2 = \frac{\tau_2 - \tau_3}{C_1} = \frac{7.687 \times 10^{-4} - 1.318 \times 10^{-4}}{0.0153 \times 10^{-6}}$$

$$R_2 = 41627\Omega$$

$$\tau_3 = C_2 R_2 \quad \therefore C_2 = \frac{\tau_3}{R_2} = \frac{1.318 \times 10^{-4}}{41627}$$

$$C_2 = 3.17\text{nF}$$

for Fig.11b: $\tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{1.53 \times 10^{-5}}{1\text{k}}$

$$C_1 = 0.0153\mu\text{F}$$

$$\tau_2 = C_1 R_2 \quad \therefore R_2 = \frac{7.687 \times 10^{-4}}{1.53 \times 10^{-8}}$$

$$R_2 = 50.242\text{k}\Omega$$

$$\tau_3 = C_2 R_3$$

Since both values are independent of the other components, either C2 or R3 can be chosen and the other calculated.

assume $R_3 = 1\text{k}\Omega \quad \therefore C_2 = \frac{1.318 \times 10^{-4}}{1000}$

$$C_2 = 1.318 \times 10\text{-}7$$

$$C_2 = 0.1318\mu\text{F}$$

SP8861

1.3 GHz LOW POWER SINGLE-CHIP FREQUENCY SYNTHESISER

(Supersedes September 1990 Edition)

The SP8861 is a low power single chip synthesiser intended for professional radio applications, and contains all the elements (apart from the loop amplifier) to fabricate a PLL frequency synthesis loop.

The device is serially programmable by a three wire data highway and contains three independent buffers to store one reference divider word and two local oscillator divider words. A digital comparator, with two charge pumps, programmable in phase and gain are provided to improve lock up performance. The preset tandem operation of the charge pumps can be overwritten or the comparison frequencies switched to output ports under control of the divider word. The dual modulus ratio and so operating range is also programmable through the same word.

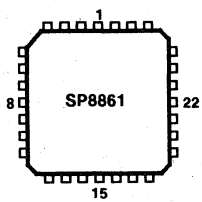
A power down mode is incorporated as a battery economy feature.

FEATURES

- Improved Digital Phase Detector to Eliminate 'Dead Band' Effects
- Low Operating Power, Typically 175mW
- 1.3GHz Operating Frequency
- Complete Phase Locked Loop
- High Input Sensitivity
- Programmed through Three Wire Data Bus
- Wide Range of Reference Division Ratios
- Local Storage for Two Frequency Words giving Rapid Frequency Toggling
- Programmable Phase Detector Gain
- Power Down Mode
- ESD Protection on all Pins

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.3V to 7V
Storage temperature	-55°C to +150°C
Operating temperature	-40°C to +85°C
Prescaler input voltage	2.5V p-p



HP28

1	IC	15	CLOCK
2	$V_{EE}3$	16	ENABLE
3	PD1 OUTPUT	17	NC
4	* Fpd	18	$V_{CC}2$
5	* Fref	19	$V_{EE}2$
6	POWER DOWN	20	XTAL 2
7	$V_{EE}4$	21	XTAL 1
8	$V_{CC}4$	22	GROUND
9	$V_{CC}1$	23	$V_{CC}3$
10	RF INPUT	24	RPD
11	RF INPUT	25	PD2 OUTPUT
12	VEE1	26	NC
13	F1/F2	27	LOCK DETECT
14	DATA	28	Cd

* Fpd and Fref outputs are reversed by the phase detector sense bit in the programming word. Diagram above is correct when sense bit is low.

$V_{CC}1$, $V_{EE}1$ - Preamp and Prescaler
$V_{CC}2$, $V_{EE}2$ - Oscillator Supplies
$V_{CC}3$, $V_{EE}3$ - Charge Pump 2 Supplies
$V_{CC}4$, $V_{EE}4$ - ECL Supplies

Fig.1 Pin connections-top view

ORDERING INFORMATION

SP8861 NA HP

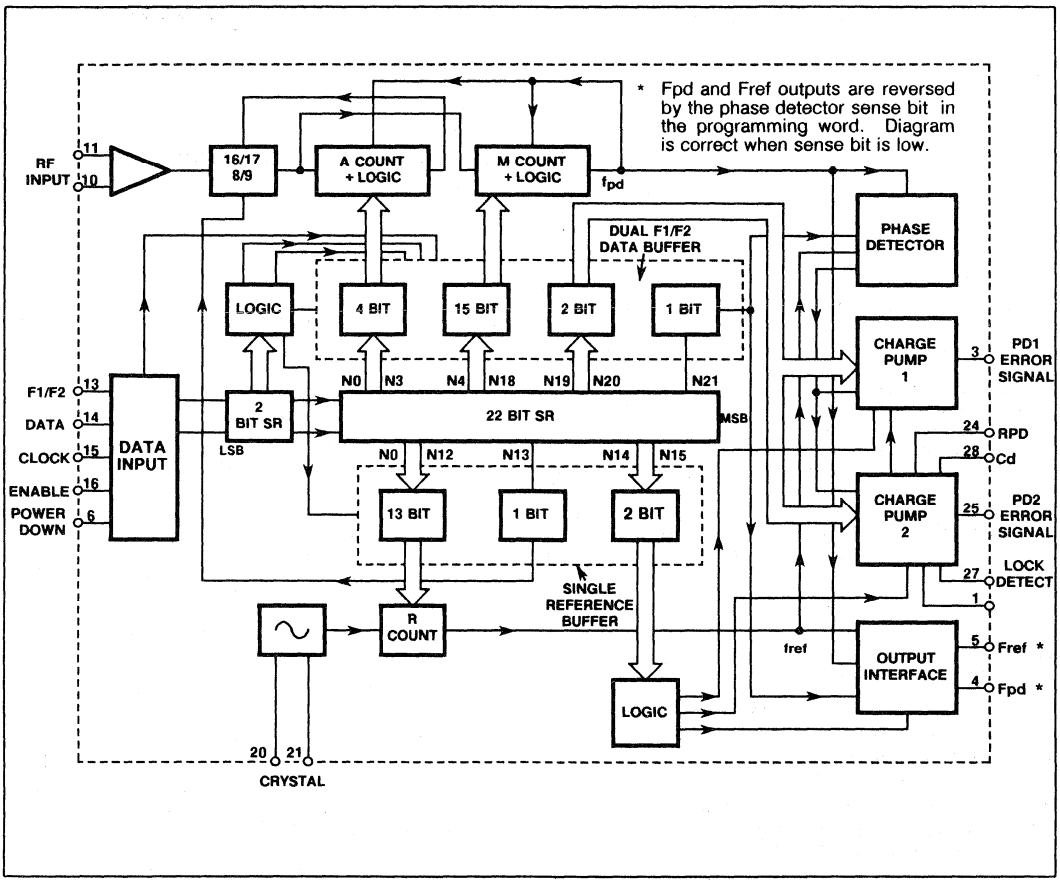


Fig. 2 SP8861 block diagram

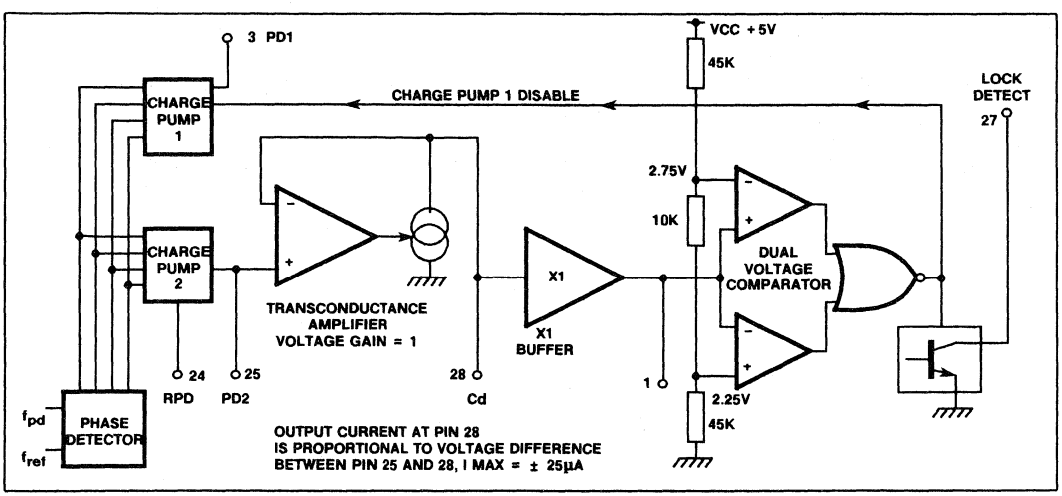


Fig. 3 Detailed Block Diagram of Lock Detect Circuit

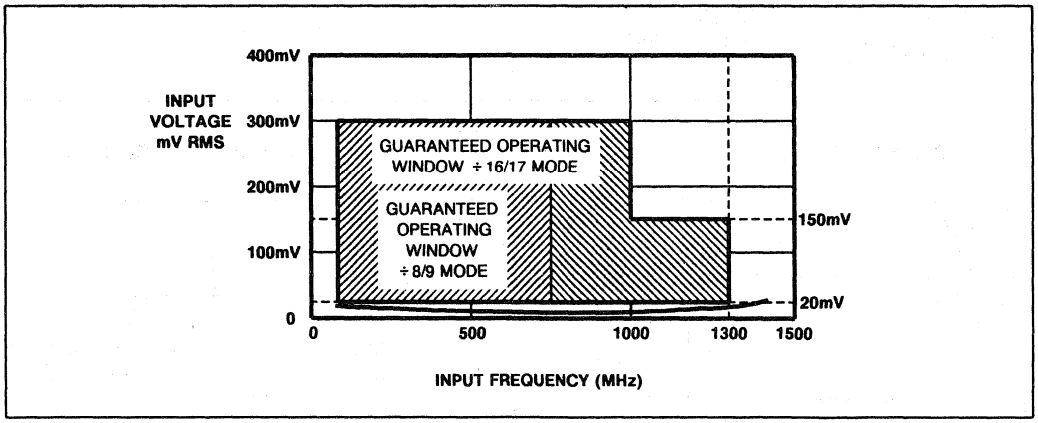


Fig. 4 Typical input characteristics and input drive requirements

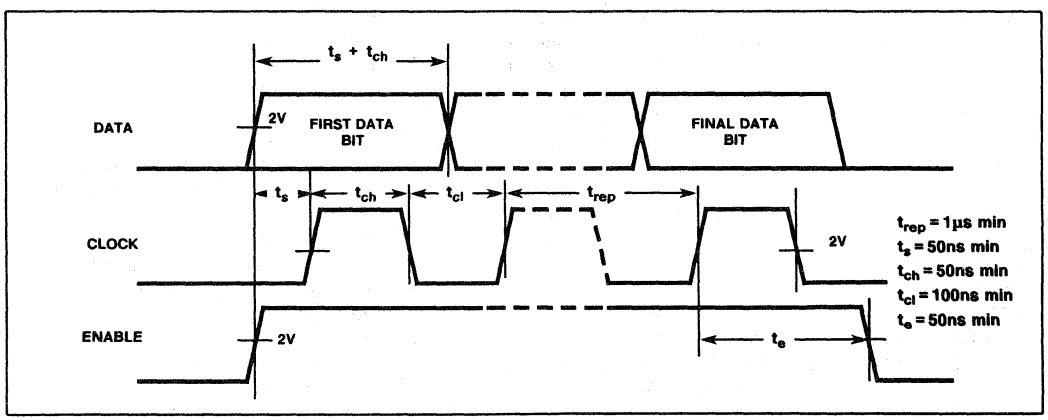


Fig. 5 Data and clock timing requirements

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = +4.75V to +5.25V
Temperature: T_{amb} = 25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	8,9					
	18,23		33	40	mA	
Supply Current in Power Down Mode	8		4.5	6	mA	
Input Sensitivity	10,11					See Fig. 4
Input Overload	10,11					See Fig. 4
RF Input Division Ratio	10,11,4	256		524287		With 16/17 selected
		56		262143		With 8/9 selected
Comparison Frequency	4,5			5	MHz	
Reference Oscillator Input Frequency	20,21	4		20	MHz	
External Reference Input Voltage	20	10		500	mVrms	
Reference Division Ratio	20,5	1		8191		
Data Clock Repetition Rate t_{rep}	15			1	μs	See Fig. 5
Minimum Set up Time t_s	14,15	50			ns	See Fig. 5
Data Input High	14	0.6Vcc		Vcc	V	
Low	14	Vee		0.3Vcc	V	
Clock Input High	15	0.6Vcc		Vcc	V	
Low	15	Vee		0.3Vcc	V	
Data Enable High	16	0.6Vcc		Vcc	V	
Low	16	Vee		0.3Vcc	V	
F1/F2 Input High	13	0.6Vcc		Vcc	V	F1 buffer selected
Low	13	Vee		0.3Vcc	V	F2 buffer selected
Power Down Input High	6	0.6Vcc		0.9Vcc	V	
Low	6	Vee		0.3Vcc	V	
F1/F2 Input Current	13			5	μA	V Pin 13 = 5.0V
Power Down Input Current	6			5	μA	V Pin 6 = 4.5V
RPD External Resistance	24	68		330	kΩ	
Lock Detect Output Voltage 'in lock'	27			1	V	I pin 27 = 1mA
Lock Detect Switching Voltage High	25	2.7			V	Vcc = 5V
Low	25			2.3	V	Vcc = 5V
Fpd and Fref Output Voltage Swing			0.9		V	Vcc = 5V. External pull down may be required

DESCRIPTION

Prescaler and A M counter

The programmable divider chain is of A M counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi-modulus division. A programmable divider of this construction has a division ratio of MN + A and a minimum integer steppable division ratio of N(N-1).

In the SP8861 the dual modulus front end prescaler is a dual N ratio device capable of being statically switched between 16/17 and 8/9 ratios. The controlling A counter is of four bit design enabling a maximum count sequence of 15, (2^4-1) which begins with the start of the M counter sequence and stops when it has counted by the preloaded number of cycles. Whilst the A counter is counting the dual modulus prescaler is held in the N + 1 mode, then relaxes back to the N mode at the completion of the sequence. The M counter is a 15-bit asynchronous divider which counts with a ratio set by a control word. In both A and M counters the controlling data from the F1/F2 buffer is loaded in sequence with every M count cycle. The N ratio of the dual modulus prescaler is selected by a one bit word in the reference divider buffer and, when a ratio of 8/9 is selected the A counter requires only three programming bits, having an impact on the frequency bit allocation as described in the data entry section.

Reference source and divider

The reference source in the SP8861 is obtained from an on board oscillator, frequency controlled by an external crystal. The oscillator can also function as a buffer amplifier allowing the use of an external reference source. In this mode the source is simply AC coupled into the oscillator transistor base on pin 20.

The oscillator output is coupled to a programmable reference divider whose output is the reference for the phase detector. The reference divider is a fully programmable 13-bit asynchronous design and can be set to any division ratio between 1 and 8191. The actual division ratio is controlled by a data word stored in the internal reference buffer.

Phase comparator

The SP8861 is provided with a digital phase comparator feeding two charge pump circuits. Charge pump 1 has preset currents programmable as shown in table 1. Charge pump 2 has a current level set by an external resistor: the current is multiplied by a factor determined by the F1 or F2 word (see table 1).

A lock detect circuit is connected to the output of charge pump 2. When the voltage level at pin 25 is between approximately 2.25 and 2.75 volts, pin 27 will be low and charge pump 1 disabled depending on the PD1 and PD2 programming bits as shown in table 4.

The output signals from the reference and M counters are available on pins 4 and 5 when programmed by the reference programming word: the various options are shown in table 4. An external phase detector may be connected to pins 4 and 5 and may be used independently or in conjunction with the on chip detector.

To allow for control direction changes introduced by the design of the control loop, a programming bit in the F1/F2 programming word interchanges the inputs to the on chip phase detector and reverses the functions on pins 4 and 5.

F1 OR F2 WORD G2	G1	CHARGE PUMP 1 CURRENT	CHARGE PUMP 2 MULTIPLIER
0	0	50µA	1
1	0	75µA	1.5
0	1	125µA	2.5
1	1	200µA	4

Table 1 Charge pump currents

Note: ***Charge pump 2** is pin 24 current × multiplication factor.* $I \text{ pin } 24 = \frac{VCC-1.5V}{RPD}$

Data entry and storage

The data section of the SP8853 consists of a data input interface, an internal data shift register and three internal data buffers.

Data is entered to the data input interface by a three wire data highway with data, clock and chip enable inputs. The input interface then routes this data to a 24-bit shift register with bus connections to three data buffers. Data entered via the serial bus is transfered to the appropriate data buffer on the negative transition of the chip enable input according to the two final data bits as shown in Table 3. The MSB of the data is entered first.

The dual F1/F2 buffer can receive two 22-bit words and controls the programmable divider A and M counters using 19-bits, the phase detector gain with two bits and the phase detector sense with one bit. A fourth input from the synthesiser control system selects the active buffer.

OUTPUT FOR RF PHASE LAG	
Sense Bit	Pins 3 and 25
0	Current source
1	Current sink

Table 2

The third buffer contains only 16 bits, 13 being used to set the reference counter division ratio, and 2 to control the phase comparator enable logic. The remaining bit sets the dual modulus prescaler N ratio.

2 Bit S.R. Contents	Buffer Loaded
00	F1
10	F2
01	Active A *
11	Reference

Table 3

** Transfer of A counter bits into buffer controlling the programmable counter*

The data words may be entered in any individual multiple sequence and the shift register can be updated whilst the data buffers retain control of the synthesiser with the previously loaded data. This enables four unique data words to be stored in the device, with three in the data buffers and a fourth in the shift register, whilst the chip is enabled. F1 word may also be updated whilst F2 is controlling the programmable divider and vice versa.

The dual F1/F2 buffer enables the device to be toggled between two frequencies using the F1/F2 select input at a rate determined by the comparasion frequency

and also enables random frequency hopping at a rate determined by a byte load period, since the loop can be locked to F1 whilst F2 is updated by entering new data via the shift register. The F1/F2 input is high to select F1.

An F1 or F2 update cycle will consist of a byte containing 24 bits, whereas the reference byte will contain 18 bits. The device requires 3 bytes, each with a chip select sequence, totalling 66 bits to fully program.

When the dual modulus counter (A count) is set to ÷8/9, the data required to set the counter is reduced by one bit, leaving an unused bit in the 22-bit F1/F2 buffer. this bit must always be set to zero when ÷8/9 mode is required. Various programming sequences are shown in Fig. 7

The data entry and storage registers are always powered up, making it possible to enter data when the device is in the powered down state.

PD2	PD1	
0	0	Fref and Fpd outputs off, charge pump 1 and 2 on
0	1	Fref and Fpd outputs on, charge pump 1 off. Charge pump 2 on
1	0	Fref and Fpd outputs off, charge pump 1 disabled by lock detect. Charge pump 2 on
1	1	Fref and Fpd outputs on, charge pump 1 disabled by lock detect. Charge pump 2 on

Table 4

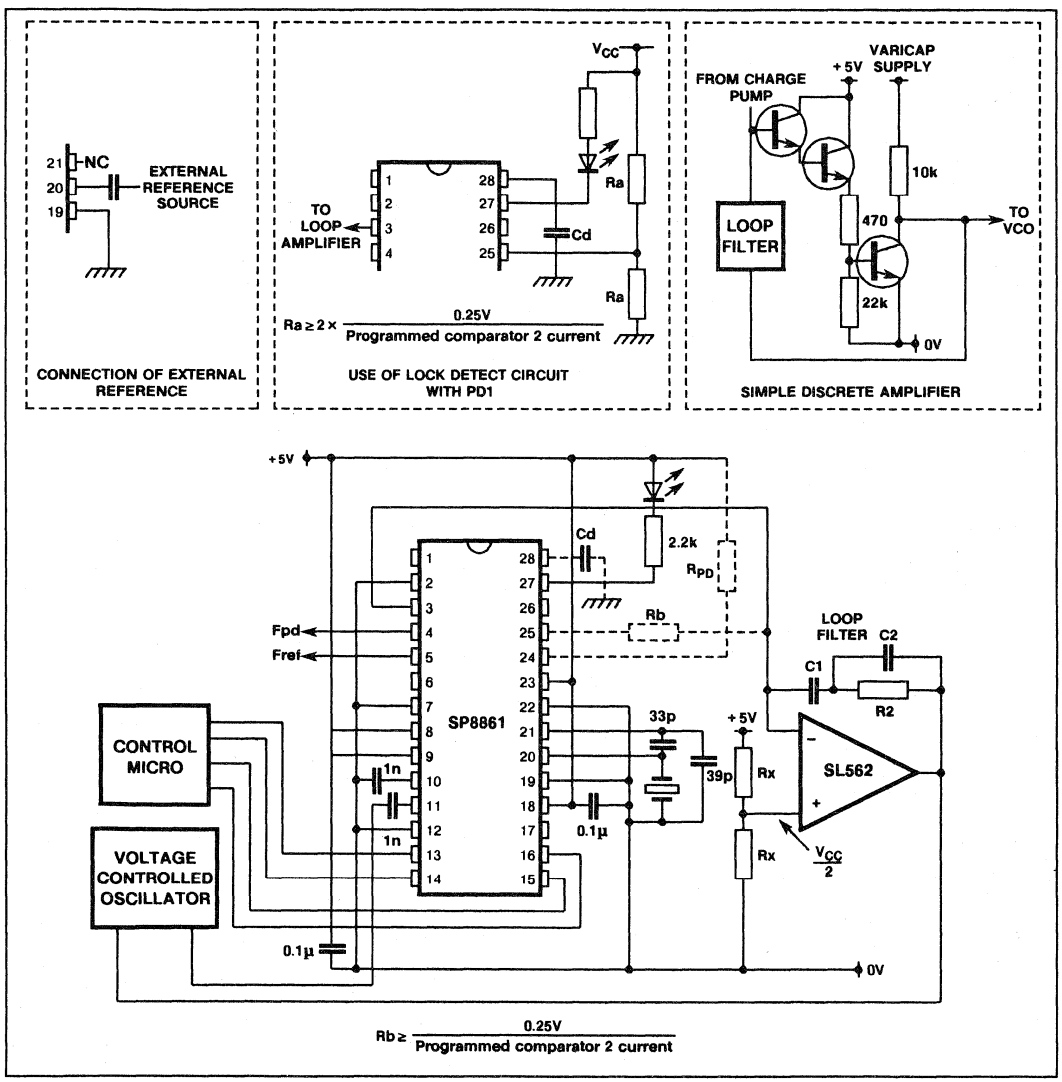


Fig. 6 Typical application diagram

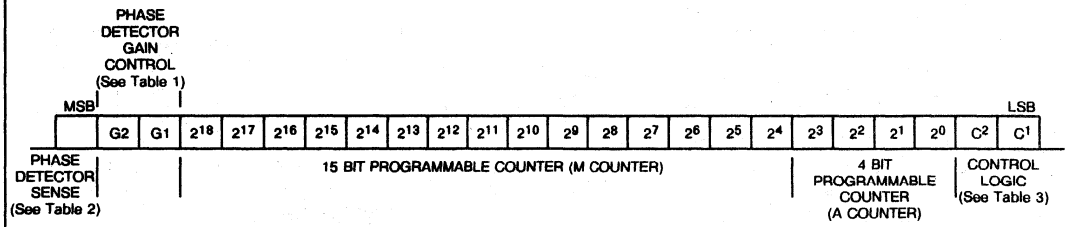


FIG.7(a) F1 or F2 word, bit allocation with 16/17 selected

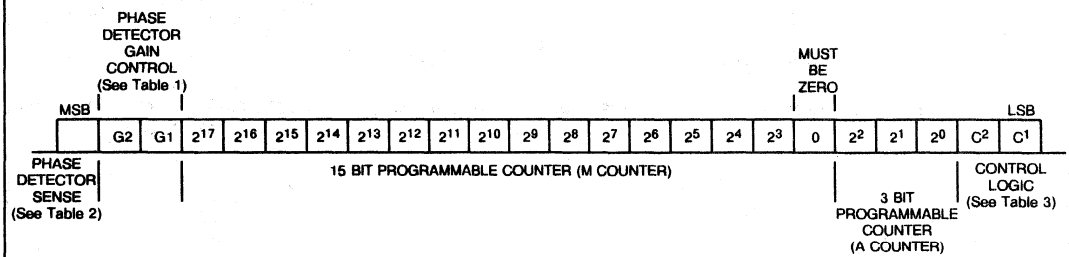


FIG.7(b) F1 or F2 word, bit allocation with 8/9 selected

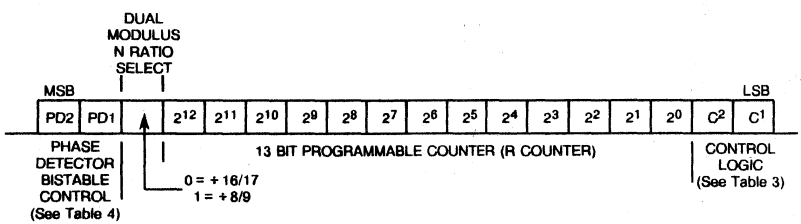


FIG.7(c) reference word bit allocation

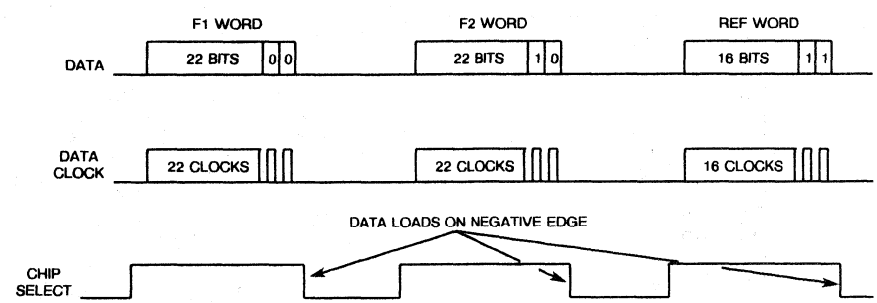


Fig.7(d) Typical data load sequence

Fig. 7 Data format diagrams

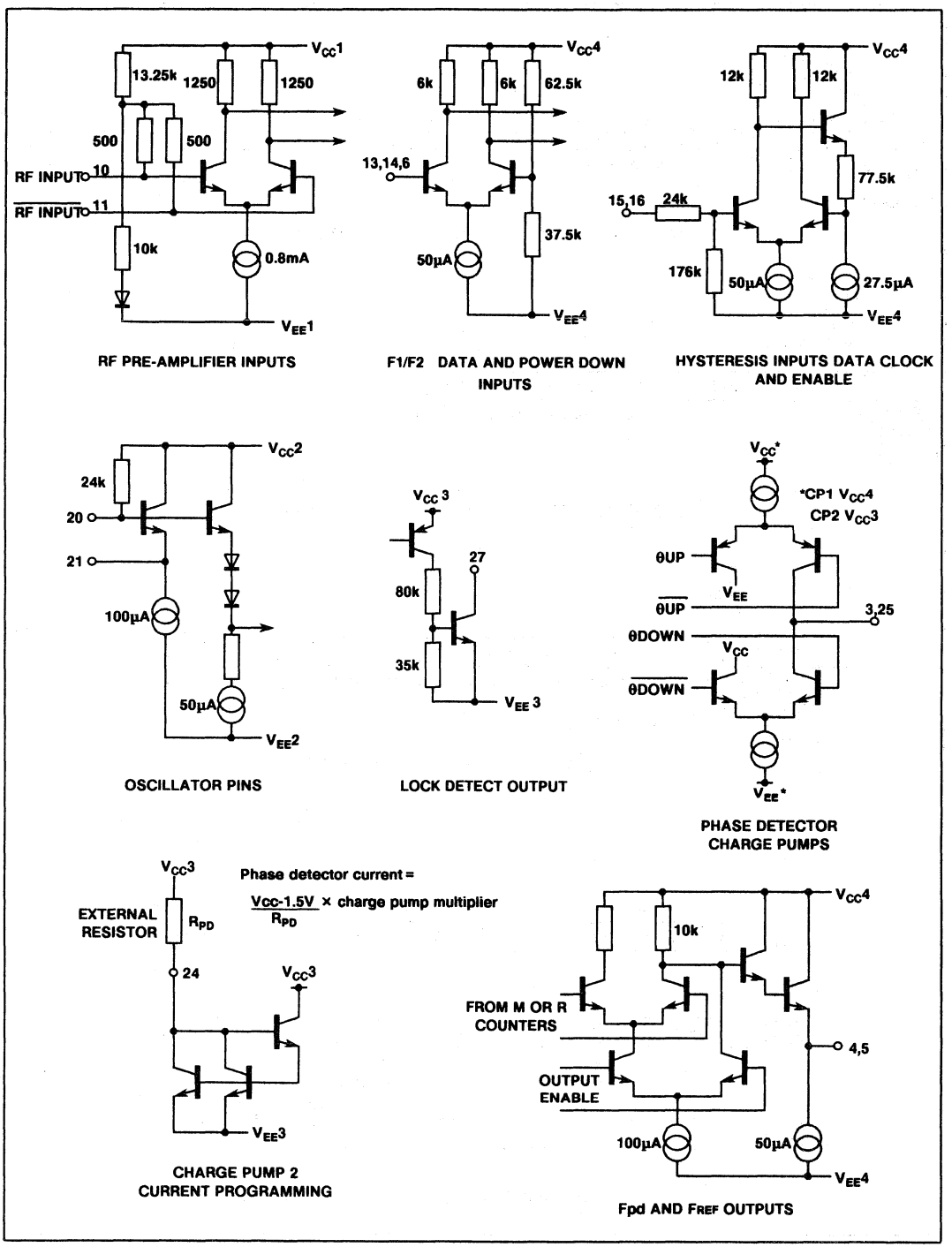


Fig. 8 Input and output interface diagrams

APPLICATIONS

A basic application using a single phase comparator is shown in Fig.6. The SP8861 is a 1.3 GHz part, so good RF design techniques should be employed, including the use of a ground plane and suitable high frequency capacitors at the RF input and for power supply decoupling.

The RF input should be coupled to either pin 10 or 11, and the other pin decoupled to ground. The reference oscillator is of conventional Colpitts type with two capacitors required to provide a low impedance tap for the feedback signal to the transistor emitter. Typical values are shown in Fig.6, although these may be varied to suit the loading requirements of particular crystals. Where a suitable reference signal already exists or where a very stable source is required, it is possible to apply an external reference as shown inset in Fig.6. The amplitude should be kept below 0.5V RMS to avoid forward biasing the transistor collector-base junction.

In some systems, it is useful to have an indication of phase lock. The output from pin 27 goes low when the output of charge pump 2 is between 2.25 and 2.75V and can be used to operate an LED to give visual indication of phase lock. Alternatively a pull-up resistor may be connected to V_{CC} and the output used to signal to the control microprocessor that the loop is locked, thus speeding up system operation. The output current available from pin 27 is limited to 1.5mA. If this current is exceeded the logic low level will be uncertain.

The circuit diagram shown in Fig.6 is a basic application with minimum component count which is nevertheless perfectly adequate for many applications. Charge pump 1 on pin 3 is used to drive the loop amplifier, which provides the control voltage for the local oscillator. When charge pump 1 is used in this mode, the PD1 and PD2 bits in the reference programming word must be set to enable charge pump 1 continuously. This application could also use charge pump 2 output on pin 25 or, if a higher phase comparator gain is required, pins 3 and 25 could be connected in parallel to use the combined output current from both charge pumps.

The lock detect circuit can be programmed to disable charge pump 1 automatically as shown in Table 4. This feature can be used to reduce the system lock up time by connecting the charge pump outputs in parallel to the loop amplifier with a resistor, Rb, in series with charge pump 2. This connection allows a relatively high current to be used from charge pump 1 to give short lock up time, and a low current to be set on charge pump 2 giving low reference frequency sidebands. The degree of lock up time improvement depends on the ratio of charge pump 1 to charge pump 2 currents.

When the loop is out of lock, both charge pumps will be enabled and will feed current to the loop amplifier to bring the oscillator to phase lock. The current from charge pump 2 will produce a voltage drop across Rb, allowing operation of the lock detect circuit and enabling charge pump 1. The resistor must be chosen to give a voltage drop greater than 0.25V at the current level programmed for charge pump 2. When phase lock is achieved, there will be no charge pump current and therefore the voltage at pin 25 will be equal to that on the virtual earth point of the loop amplifier (2.5V), disabling charge pump 1.

Charge pump 1 should not be left open circuit when enabled as this prevents correct operation of the phase detector. The output on pin 3 should be biased to half supply with a pair of 4.7kΩ resistors connected between supplies.

When charge pump 2 is used to drive the loop amplifier, the lock detect circuit will only give an out of lock indication when large frequency changes are made or when a frequency outside the range of the local oscillator is programmed. At other times the loop amplifier input is maintained at 2.5V by the action of the loop filter components. Again, resistor Rb connected between pin 25 and the loop amplifier, producing a voltage drop greater than 0.25V at the charge pump current programmed, will allow sensitive out of lock detection.

When phase lock detection is required using comparator 1 only (see inset Fig.6), charge pump 2 output (pin 25) should be biased to 2.5V using two equal value resistors, Ra, across the supply. The values should be chosen to give a voltage change greater than 0.25V at the programmed comparator 2 charge pump current. A small capacitor, Cd, connected from pin 28 to ground may be used to reduce chatter at the lock detect output. A detailed block diagram showing the lock detect circuit is shown in Fig 3.

An amplifier is required to convert the current pulses from the phase comparator into a voltage of suitable magnitude to drive the chosen VCO. The choice of amplifier must be determined by the voltage swing required at the VCO to achieve the necessary frequency range, and in most cases an operational amplifier will be used to provide the essential characteristics of high input impedance, high gain and low output impedance required in this application.

Although it is expected that an operational amplifier will be used in most cases, a simple discrete design can be used and a suitable design is shown inset in Fig.6. This arrangement can be particularly useful when the minimum VCO control voltage must be close to ground and where negative supplies are inconvenient. This form of amplifier is not suitable for use with charge pump 2 when the lock detect circuit is required.

When an operational amplifier is used in the inverting configuration shown in Fig.6, the charge pump output is connected directly to the virtual earth point and will therefore operate at a voltage similar to that set on the non-inverting input. Normally this operating point should be set at half supply using a potentiometer of two equal resistors, Rx, but if necessary this voltage can be set up to 1V higher or lower than half supply without detrimental effect. When the lock detect function is required on charge pump 2, the non inverting input must be at half supply.

The digital phase comparator and charge pump used on the SP8861 produces bi-directional current pulses in order to correct errors between the reference and VCO divider outputs. Once synchronisation is achieved, in theory no further output from the charge pump should be required, but in practice, due to leakage currents and particularly the input current of the amplifier, the capacitors forming the loop filter around the amplifier will gradually discharge, modifying the VCO voltage and requiring further outputs from the charge pump to restore the charge. The effect of this continuous correction of the local oscillator frequency is to frequency-modulate the VCO and thus produce sidebands at the reference frequency. In order to reduce this effect to a minimum, an amplifier with low input bias current is essential.

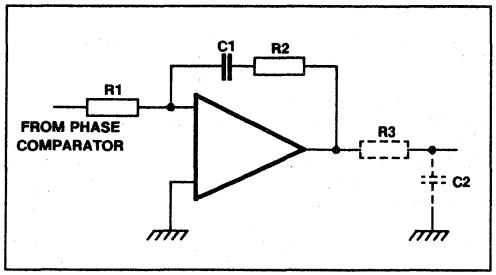


Fig. 9 Standard Form of Second Order Loop Filter

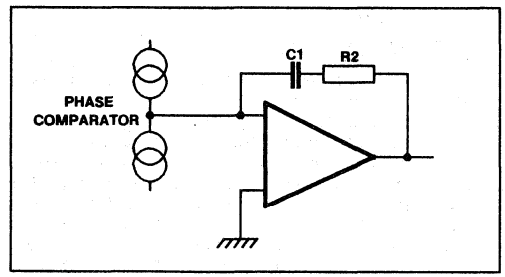


Fig.10 Modified Second Order Loop Filter

Loop calculations

Many frequency synthesiser designs use a second order loop with a loop filter of the form shown in Fig.9.

In practice an additional RC time constant (shown dotted in Fig.9) is often added to reduce noise from the amplifier. In addition any feedthrough capacitor or local decoupling at the VCO will be added to the value of C2. These additional components in fact form a third order loop, and if the values are chosen correctly, the additional filtering provided can considerably reduce the level of reference frequency sidebands and noise without adversly affecting the loop settling time. The calculation of values for both forms of loop is shown below.

Second Order Loop.

For this filter two equations are required to determine the time constants τ_1 and τ_2 where:

$$\tau_1 = C_1 R_1$$
$$\tau_2 = C_1 R_2$$

The equations are:

$$\tau_1 = \frac{K_\theta K_0}{\omega_n^2 N} \quad \ldots (1)$$

$$\tau_2 = \frac{2\zeta}{\omega_n} \quad \ldots (2)$$

where:

K_θ is the phase detector gain factor in V/Radian
K_0 is the VCO gain factor in radians second /Volt
N is the division ratio from VCO to reference frequency
ω_n is the natural loop bandwidth
ζ is the damping factor: normaly 0.7071

The SP8853 phase comparator is a current source rather than a conventional voltage source and has a gain factor specified in µA/radian. Since the equations deal with a filter where R_1 is feeding the virtual earth point of an operational amplifier from a voltage source, R_1 sets the input current to the filter. This is similar to the circuit shown in Fig.10, where a current source phase comparator is connected directly to the virtual earth point of the operational amplifier.

The equivalent voltage gain of the phase comparator can be calculated by assuming a value for R_1 and calculating a gain in volts/radian which would produce the set current.

The digital phase comparator used in the SP8861 is linear over a range of 2π radians and therefore the phase comparator gain is given by:

$$\frac{\text{phase comparator current setting}}{2\pi} \text{ µA/Radian.}$$

The phase comparator gain in V/radian is therefore:

$$\frac{50\,\mu A}{2\pi} \times 1k\Omega$$

assuming a value of 1kΩ for R_1 and 50µA for the phase comparator current setting, these values can now be inserted in equation (1) to obtain values for C_1 and equation (2) used to determine a value for R_2.

Example:

Calculate values for a second order loop with the following parameters.

Frequency to be synthesised	800Mhz
Reference frequency	100kHz
Division ratio N	$\frac{800MHz}{100kHz} = 8000$
Natural loop frequency ω_n	500Hz
VCO gain factor K_0	2π x 10MHz/Volt
Damping factor ζ	0.7071
Phase comparator current setting	50µA

Assuming R_1 is 1kΩ, then the equivalent phase comparator gain K_θ in V/radian $= \frac{50\mu A}{2\pi} \times 1000$

$$K_\theta = 0.00796 \text{V/radian.}$$

From equation 1 $$\tau_1 \frac{0.00796 \times 2 \times \pi \times 10MHz}{(2 \times \pi \times 500)^2 \times 8000}$$

$$\tau_1 = 6.334 \times 10^{-6}$$

From equation 2 $$\tau_2 = \frac{2 \times 0.7071}{2 \times \pi \times 500}$$

$$\tau_2 = 4.50 \times 10^{-4}$$

Now $$\tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{6.334 \times 10^{-6}}{1k\Omega}$$

1K is chosen value for R_1

$$C_1 = 6.33nF$$

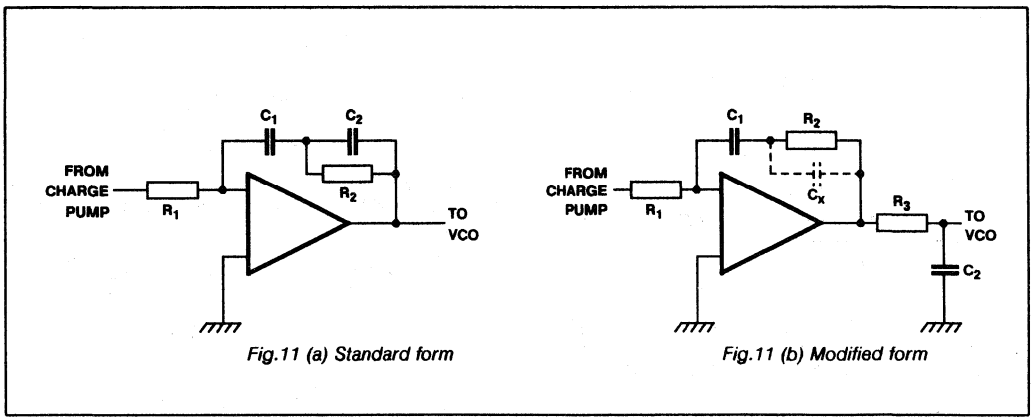


Fig.11 (a) Standard form

Fig.11 (b) Modified form

Fig.11 Third order loop filter

$$\tau_2 = C_1 R_2 \therefore \frac{4.50\times10^{-4}}{6.33\times10^{-9}} = R_2$$

$$R_2 = 71000\ \Omega$$

Third Order Loop

The third order loop filter is normally shown as in Fig.11a. Fig.11b shows the circuit redrawn to use an RC time constant after the amplifier, allowing any feedthrough capacitance on the VCO line to be included in the loop calculations. Where the modified form in Fig.11b is used it is advantageous to connect a small capacitor Cx of typically 100pF (shown dotted), across the amplifier to reduce sidebands caused by the amplifier being forced into non-linear operation by the phase comparator pulses.

Three equations are required to determine the time constants, τ_1, τ_2 and τ_3 where :

for Fig.11a:
$$\tau_1 = C_1 R_1$$
$$\tau_2 = R_2 (C_1 + C_2)$$
$$\tau_3 = C_2 R_2$$

and for Fig.11b:
$$\tau_1 = C_1 R_1$$
$$\tau_2 = C_1 R_2$$
$$\tau_3 = C_2 R_3$$

The equations are:

$$\tau_1 = \frac{K_\theta K_0}{N\omega_n^2}\left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]^{\frac{1}{2}} \quad \ldots(3)$$

$$\tau_2 = \frac{1}{\omega_n^2 \tau_3} \quad \ldots(4)$$

$$\tau_3 = \frac{-\tan\phi_0 + \frac{1}{\cos\phi_0}}{\omega_n} \quad \ldots(5)$$

Where:

K_θ is the phase detector gain factor in V/Radian
K_0 is the VCO gain factor in radians second/Volt
N is the total division ratio from VCO to reference frequency
ω_n is the natural loop bandwidth
ϕ_0 is the Phase margin normaly set to 45°

As in the second order filter example a value for R1 can be assumed and an equivalent gain K_θ in V/radian calculated from:

$$\frac{\text{phase comparator current setting } \mu\text{A/radian}}{2\pi} \times 1\text{k}$$

Where 1kΩ is the assumed value for R_1

These values can now be substituted in equation (3) to obtain a value for C_1 and equations (4) and (5) used to determine values for C_2 and R_2.

EXAMPLE

Calculate values for a loop with the following parameters.

Frequency to be synthesised:	800MHz
Reference frequency	100kHz
Division ratio	$\frac{800\text{MHz}}{100\text{kHz}} = 8000$
ω_n natural loop frequency	500Hz
K_0 VCO gain factor	2π x 10MHz/Volt
ϕ_0 phase margin	45°
Phase comparator current	50μA

assuming R_1 is 1kΩ, then the equivalent phase comparator gain K_θ in V/radian is:

$$\frac{50\mu A}{2\pi} \times 1000 = 0.00796 \text{ V/Radian}$$

From equation (3):

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{500\text{Hz} \times 2\pi} = \frac{0.4142}{3141.6}$$

$$\tau_3 = 1.318 \times 10^{-4}$$

From equation (4):

$$\tau_2 = \frac{1}{(500 \times 2 \times \pi)^2 \times 1.318 \times 10^{-4}}$$

$$\tau_2 = 7.687 \times 10^{-4}$$

Using these values in equation (3):

$$\tau_1 = \frac{7.96 \times 10^{-3} \times 2 \times \pi \times 10\text{MHz/V}}{8000 \times (2\pi \times 500)^2} \left[A\right]^{\frac{1}{2}}$$

Where A is:

$$\frac{1+\omega_n^2 \tau_2^2}{1+\omega_n^2 \tau_3^2} = \frac{1+(2\pi \times 500)^2 \times (7.687 \times 10^{-4})^2}{1+(2\pi \times 500)^2 \times (1.318 \times 10^{-4})^2}$$

$$\tau_1 = \frac{500141.6}{7.896 \times 10^{10}} \left[\frac{6.832}{1.1714}\right]^{\frac{1}{2}}$$

$$\tau_1 = 6.334 \times 10^{-6} \times 2.415$$

$$\tau_1 = 1.53 \times 10^{-5}$$

now $\tau_1 = C_1 R_1$

$$\therefore C_1 = \frac{1.53 \times 10^{-5}}{1\text{k}\Omega} \quad (R_1 \text{ is chosen as } 1\text{k}\Omega)$$

$$C_1 = 0.0153\mu\text{F}$$

for Fig.11a: $\tau_2 = R_2 (C_1 + C_2)$

for Fig.11b: $\tau_3 = C_2 R_2$

substituting for C_2

$$\tau_2 = R_2 \left[C_1 + \frac{\tau_3}{R_2}\right] \quad \therefore \tau_2 = R_2 C_1 + \tau_3$$

$$\therefore R_2 = \frac{\tau_2 - \tau_3}{C_1} = \frac{7.687 \times 10^{-4} - 1.318 \times 10^{-4}}{0.0153 \times 10^{-6}}$$

$$R_2 = 41627\Omega$$

$$\tau_3 = C_2 R_2 \quad \therefore C_2 = \frac{\tau_3}{R_2} = \frac{1.318 \times 10^{-4}}{41627}$$

$$C_2 = 3.17\text{nF}$$

for Fig.11b: $\tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{1.53 \times 10^{-5}}{1\text{k}}$

$$C_1 = 0.0153\mu\text{F}$$

$$\tau_2 = C_1 R_2 \quad \therefore R_2 = \frac{7.687 \times 10^{-4}}{1.53 \times 10^{-8}}$$

$$R_2 = 50.242\text{k}\Omega$$

$$\tau_3 = C_2 R_3$$

Since both values are independent of the other components, either C2 or R3 can be chosen and the other calculated.

assume $R_3 = 1\text{k}\Omega \quad \therefore C_2 = \frac{1.318 \times 10^{-4}}{1000}$

$$C_2 = 1.318 \times 10\text{-}7$$

$$C_2 = 0.1318\mu\text{F}$$

NJ88C40

SINGLE CHIP SYNTHESISER

The NJ88C40 contains all the logic needed for a VHF PLL synthesiser and is fabricated on the Plessey high performance small geometry CMOS. The circuit contains a reference oscillator and divider, a two modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic.

FEATURES

- Low Power CMOS - 7mA Max.
- Easy To Use
- 200 MHz Frequency Range
- Single Chip Synthesiser to VHF
- Lock Detect Output

APPLICATIONS

- Mobile Radios
- Hand Held Portable Radios
- Sonarbuoys

ABSOLUTE MAXIMUM RATINGS

V_{DD}	--0.3V to +6V
Voltage on any pin	-0.3V to V_{DD} +0.3V
Operating temperature	-40°C to +85°C
Storage temperature	-55°C to +125°C

ORDERING INFORMATION

NJ88C40 MA DG
NJ88C40 MA MP

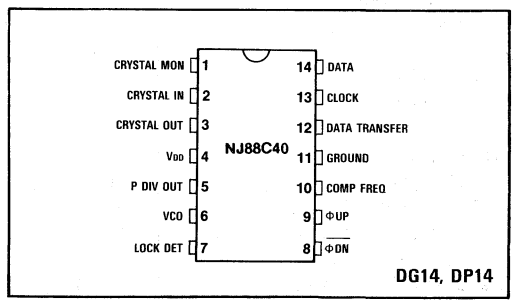


Fig.1 Pin connections (top view)

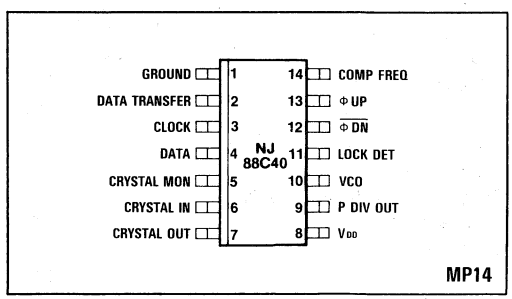


Fig.2 Pin connections (top view)

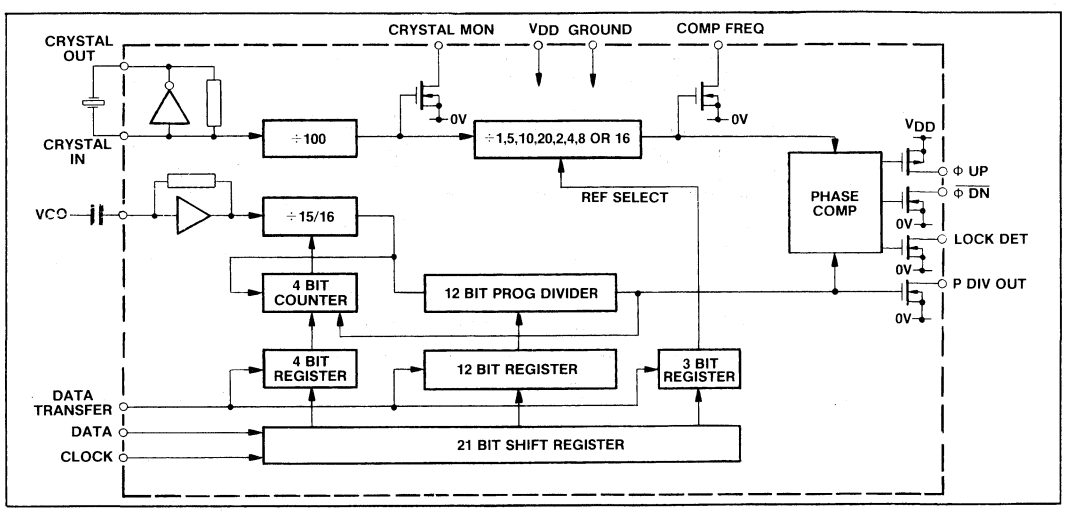
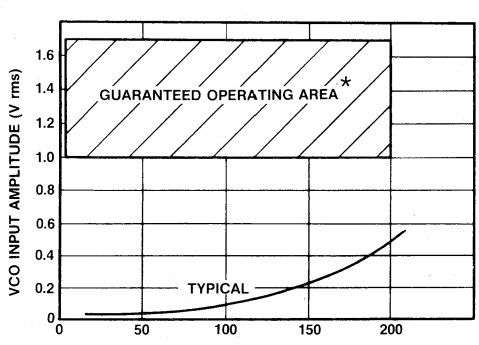


Fig.3 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 5V ± 0.5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply						
Supply current	8		4	7	mA	1V rms VCO input at 200MHz and f_{XTAL} = 10MHz
Crystal oscillator						
Frequency	6,7		10	15	MHz	Parallel resonant, fundamental crystal
External input level	6	1			V rms	AC coupled
High level	6	V_{DD}-1			V	DC coupled
Low level	6			1	V	DC coupled
VCO input						
VCO input sensitivity	10	1			V rms	At 200MHz, see Fig.4
Slew rate VCO input	10	4			V/μs	
VCO input impedance	10		5pF/10kΩ			
VCO input frequency	10	200			MHz	
DATA, DATA TRANSFER, CLOCK inputs						
High level	2,3,4	V_{DD}-1			V	
Low level	2,3,4			1	V	
Rise, fall time	2,3			200	ns	
Data set up time	3,4	200			ns	See Fig.5
Clock frequency	3			2	MHz	
Transfer pulse width	2	500			ns	
Crystal monitor output						
Current sink	5	0.8			mA	V_{OUT} = 0.5V
Comp freq, LOCK DET, P DIV						
Current sink	9,11,14	1.6			mA	V_{OUT} = 0.5V
Φ UP/Φ DN						
Current sink	12	0.8			mA	V_{OUT} = 0.5V
Current source	13	0.8			mA	V_{OUT} = V_{DD} - 0.5V



* Tested as specified in Table of Electrical Characteristics

Fig.4 Input sensitivity

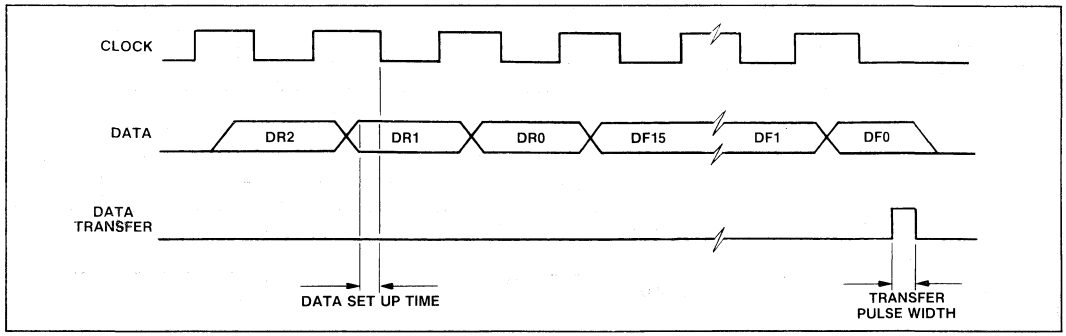


Fig.5 Input data timing diagram

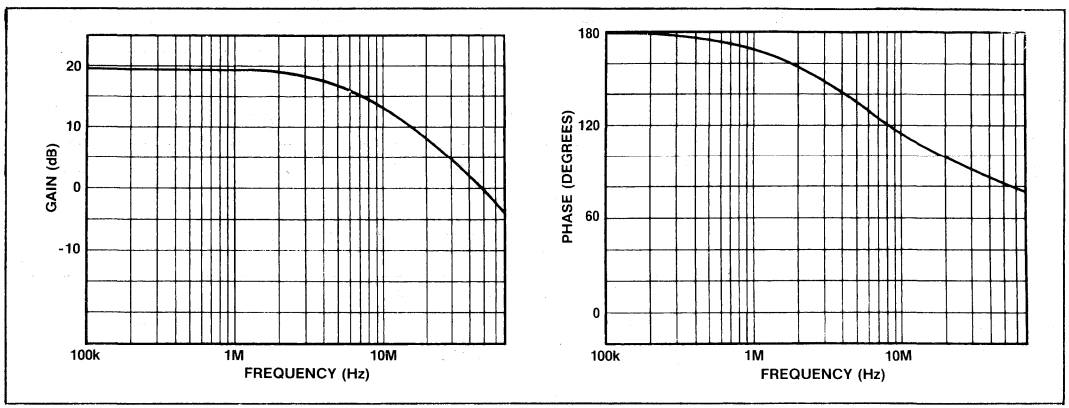


Fig.6 Gain phase characteristics of reference oscillator inverter

CIRCUIT DESCRIPTION

Crystal Oscillator and Reference Divider

The reference oscillator consists of a Pierce type oscillator intended for use with parallel resonant fundamental crystals. Typical gain and phase characteristics for the oscillator inverter are shown in Fig.6. An external reference oscillator may be used by either capacitively coupling a 1V rms sinewave into the CRYSTAL IN pin or if CMOS logic levels are available by connecting directly to CRYSTAL IN pin.

The reference oscillator drives a divider to produce a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies if a 10MHz crystal is used are shown in Fig.7.

DR2	DR1	DR0	Division Ratio	Comparison Frequency for 10MHz Ref. Osc.
0	0	0	1600	6.25kHz
0	0	1	800	12.5kHz
0	1	0	400	25kHz
0	1	1	200	50kHz
1	0	0	2000	5kHz
1	0	1	1000	10kHz
1	1	0	500	20kHz
1	1	1	100	100kHz

Fig.7 Reference divider division ratios

To assist in trimming the crystal, an open drain output at one hundredth of the reference oscillator frequency is provided on CRYSTAL MONITOR pin 1.

Programmable Divider

The programmable divider consits of a ÷15/16 two modulus prescaler with a 4-bit control register followed by a 12-bit programmable divider. A 1V rms sinewave should be capacitively coupled from the VCO to the divider input VCO pin.

The overall division ratio is selected by a single 16-bit word (DF 15 to 0) loaded through the serial data bus. A lower limit of 240 ensures correct prescaler operation; the upper limit is 65535. The VCO frequency in a locked system will be this division ratio multiplied by the comparison frequency.

Phase Comparator

The phase comparator consists of a digital type phase comparator with open drain Φ UP and $\overline{\Phi \text{ DN}}$ outputs and an open drain lock detect output. Open drain outputs from the reference divider and programmable divider are provided for monitoring purposes or for use with an external phase comparator. Waveforms for all these outputs are shown in Fig.8. The duty cycle of Φ UP and $\overline{\Phi \text{ DN}}$ versus phase difference are shown in Fig.9. The phase comparator is linear over a $\pm 2\pi$ range and if the phase gains or slips by more than 2π the phase comparator outputs repeat with a 2π period.

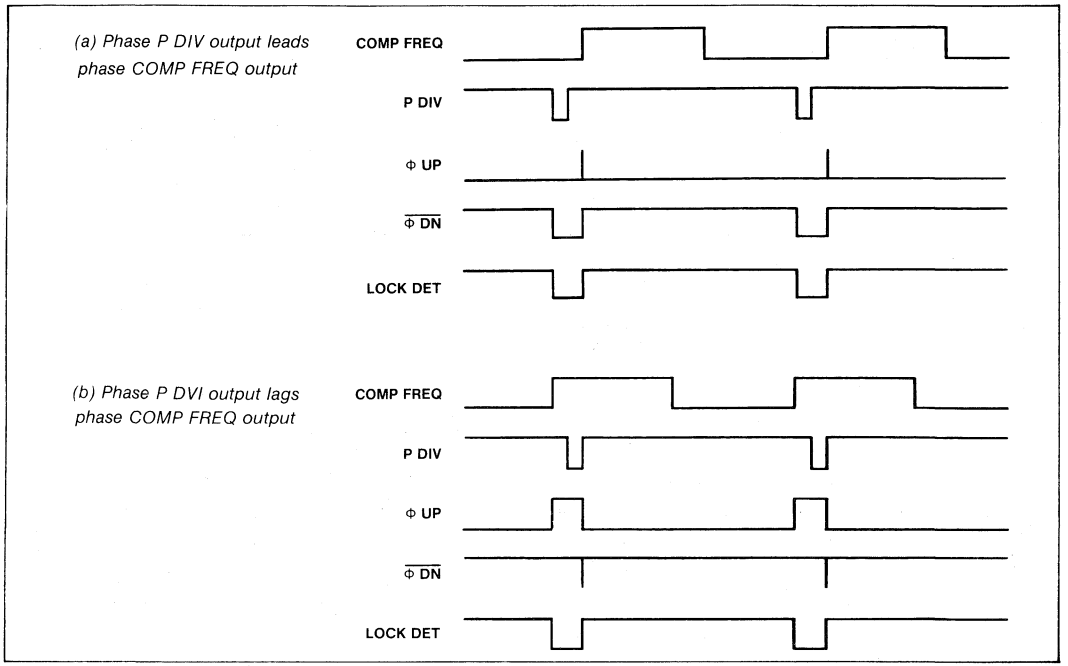


Fig.8 Phase comparator waveforms

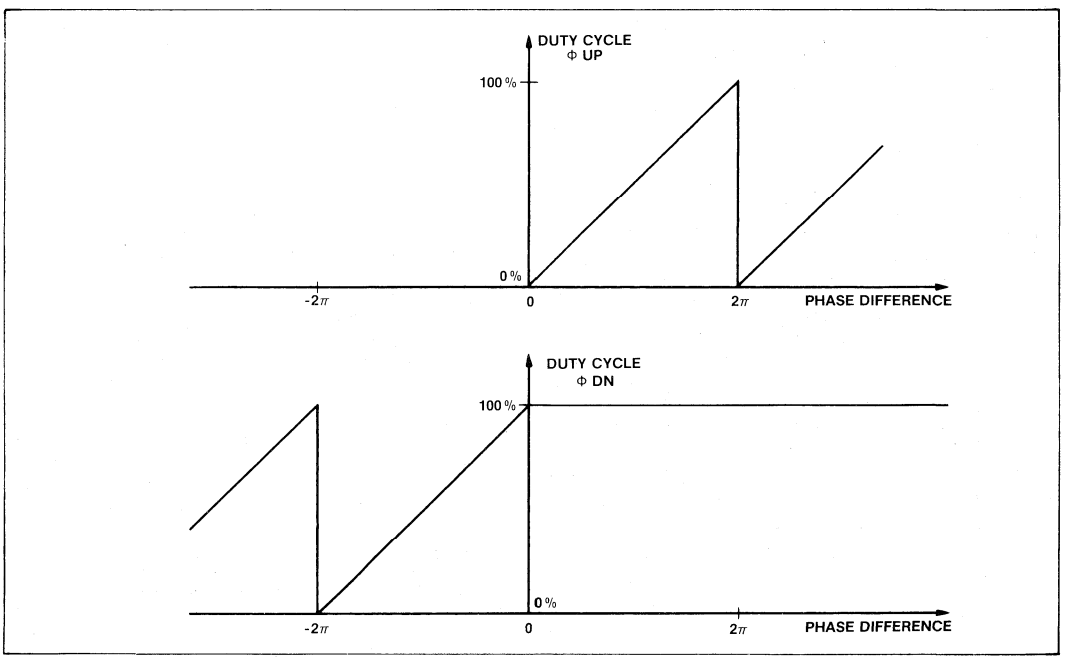


Fig.9 Phase comparator output characteristics

Once the phase difference exceeds 2π the comparator will gain or slip one cycle and then try to lock to the new zero phase difference. Note very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output.

Data Input and Control Register

To control the synthesiser a simple three line serial input is used with Data, Clock and Data Transfer signals. The data consists of 19 bits, the first three DR2, DR1, DR0 control the reference divider, the next sixteen, DF15 to DF0, control the prescaler and programmable divider. Until the synthesiser receives the Data Transfer pulse it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data.

APPLICATIONS

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig.10. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig.10 is required. Pulses from the phase comparator are filtered by R_1, R_2 and C_1. Their values can be determined, given a required natural loop bandwidth ω_n and damping factor δ, by the following equations:

$$R_1C_1 = \frac{K}{\omega_n^2}, \quad R_2C_1 = \frac{2\delta}{\omega_n} \quad \text{and} \quad K = \frac{GK_0V_{CC}}{2\pi N}$$

where

ω - natural loop bandwidth (rad/s)
δ - damping factor
K_0 - VCO gain factor (rad/Vs)
V_{CC} - charge pump supply voltage (V)
N - division ratio = f_{OUT}/f_{COMP}
G - gain of amplifier

The values in Fig. 10 were calculated for:

ω_n = 3000 rad/s
δ = 0.707
K_0 = 18 Mrad/Vs
V_{CC} = 5V
f_{OUT} = 100MHz
f_{COMP} = 50kHz
G = 2

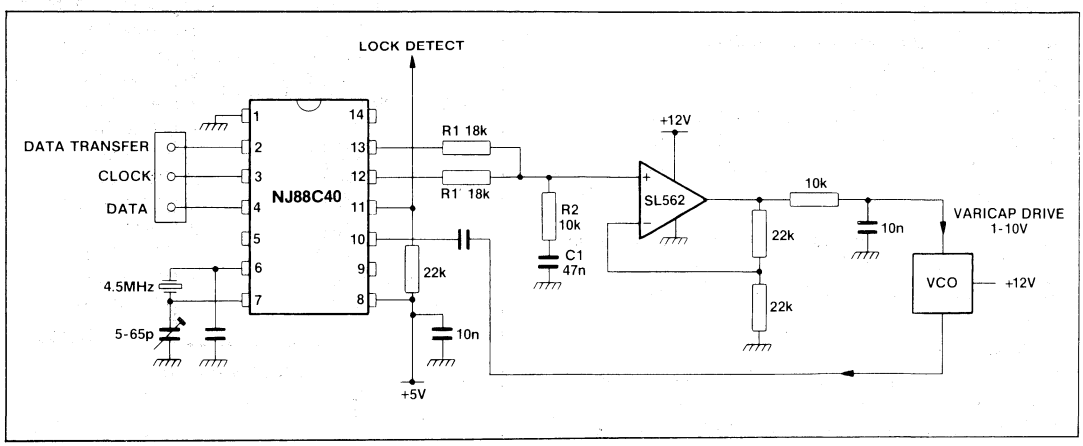


Fig.10 Typical application

Example of Programming

For a channel spacing (comparison frequency) of 5kHz when using a crystal oscillator of 10MHz the reference divider ratio will need to be 2000 (see Fig.7). This is programmed as binary 100 in the most significant three of the 19 bits (MSB programmed first).

To obtain the maximum VCO frequency of 200MHz the programmable divider ratio would be:

$$\frac{200 \times 10^6}{5 \times 10^3} = 40 \times 10^3 \text{ which is 9C40 Hex.}$$

The complete program word would then be:

	DR			DF														
Bit No.	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0
Hex	4			9				C				4				0			

Using the same crystal and 5kHz channel spacing the minimum VCO frequency programmable would be 1.2MHz with the division ratio of 240 (F0 Hex). The program word would then be:

	DR			DF														
Bit No.	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Hex	4			0				0				F				0			

SP2001

100MHz DIRECT DIGITAL FREQUENCY SYNTHESISER

(Supersedes January 1991 Edition)

The SP2001 Direct Frequency Synthesiser (DFS) is an ECL100K compatible 'numerically controlled oscillator' i.e. it directly generates the DAC code required for an output sinewave at any frequency up to 100MHz. The SP2001 has a 16 bit input bus giving a step size and minimum output frequency of 4kHz with a 262.144MHz clock

A full block diagram is shown in Fig 2.

FEATURES

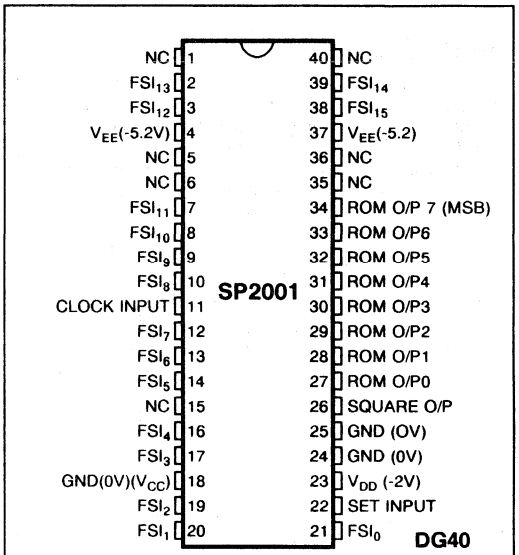
- Maximum clock frequency >300MHz
- 16-Bit Frequency resolution
- 8-Bit Parallel Cosine Output
- ECL 100K Compatible Inputs and Outputs
- Maximum Output Frequency > 100MHz
- Useable with 5, 10, 15 or 25kHz Channel Spacing
- Useable with 3.125, 6.25, 12.5 or 25kHz Channel Spacing
- Asynchronous Data Load for Fast (17ns) Hop Time
- Low Power: 1.85W
- Very Low Close to Carrier Noise.-135dBc/Hz Typ

APPLICATIONS

- LocalOscillator/Transmitter Synthesis in VHF Low Band (30-100MHz)
- LO Synthesis in Frequency Agile Radio/Radar
- Wide Single-Range Sinewave Generator
- ECM/ECCM -e.g. Follower Jammers or Fast Hoppers

ORDERING INFORMATION

SP2001 B DG
SP2001 A DG
SP2001 AA DG
SP2001 B HG
SP2001 A HG
SP2001 AA HG



PIN CONNECTIONS FOR HG PACKAGE

1	NC	16	NC	31	SQUARE O/P
2	FSI_{13}	17	NC	32	ROM O/P0
3	FSI_{12}	18	NC	33	ROM O/P1
4	V_{EE}(-5.2V)	19	FSI_4	34	ROM O/P2
5	NC	20	FSI_3	35	ROM O/P3
6	NC	21	GND(0V)(V_{CC})	36	ROM O/P4
7	NC	22	FSI_2	37	ROM O/P5
8	FSI_{11}	23	FSI_1	38	ROM O/P6
9	FSI_{10}	24	FSI_0	39	ROM O/P7
10	FSI_9	25	SET INPUT	40	NC
11	FSI_8	25	V_{DD}(-2V)	41	NC
12	CLOCK	27	GND(0V)	42	V_{EE}(-5.2V)
13	FSI_7	28	GND(0V)	43	FSI_{15}
14	FSI_6	29	NC	44	FSI_{14}
15	FSI_5	30	NC		

Fig.1 Pin connections - top view

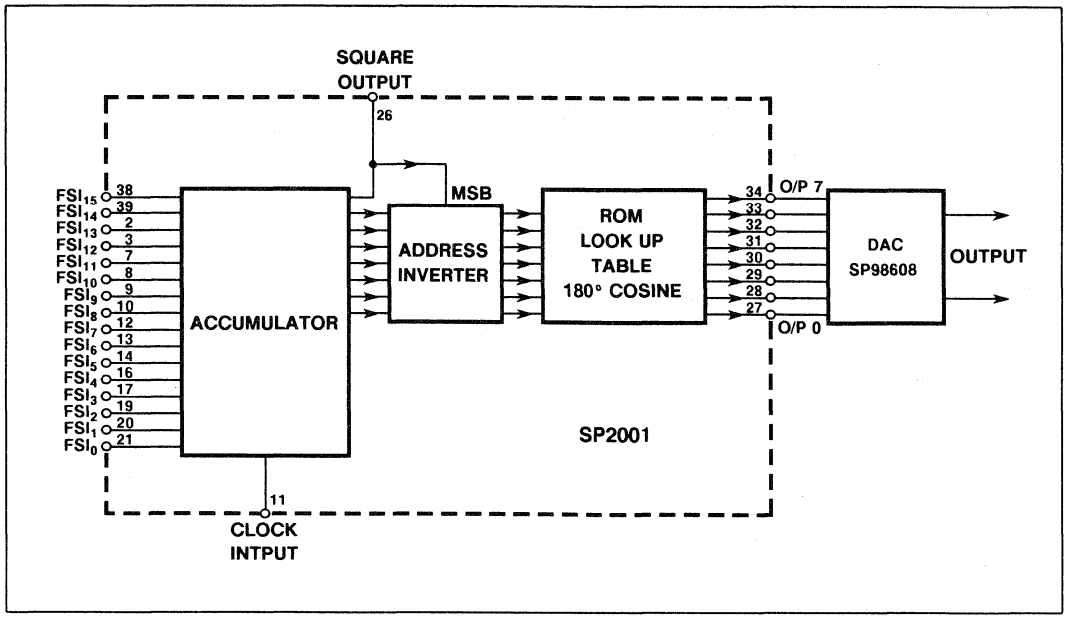


Fig.2 SP2001 Direct Frequency Synthesiser block diagram

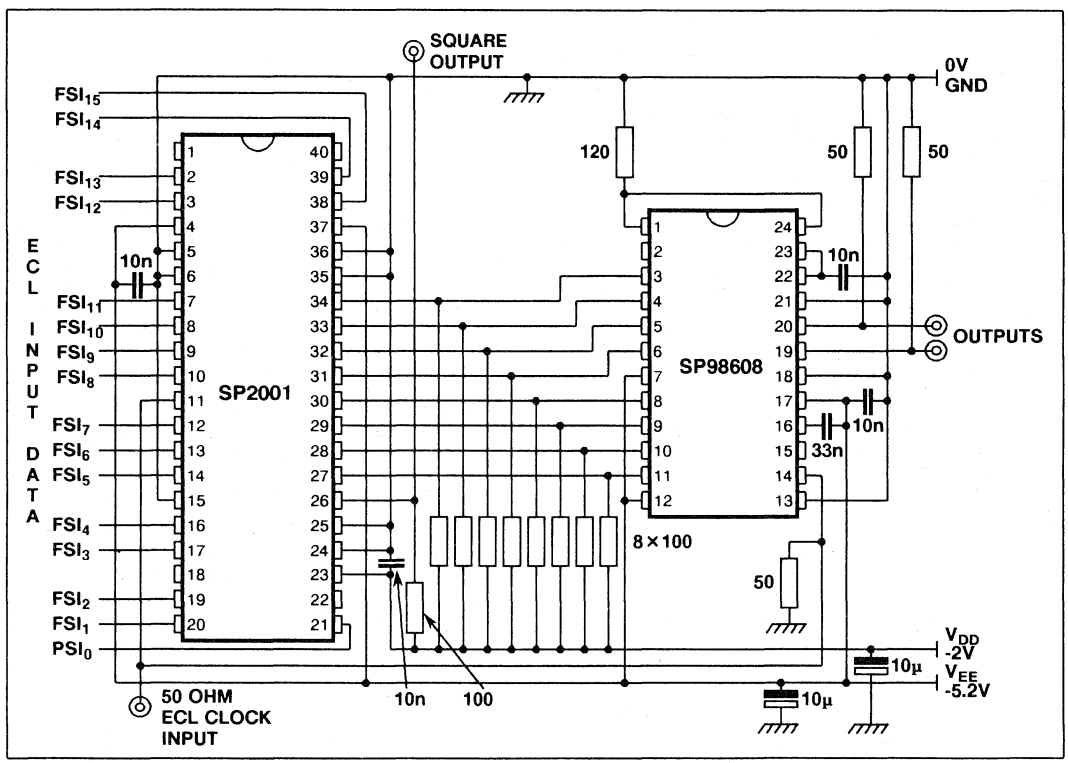


Fig.3 SP2001 Typical application circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
V_{EE} = -5.2V ± 0.25V, V_{DD} = -2V ± 0.1V, V_{CC} = GND
A Grade T_{amb} = -55°C to +125°C (see note), B Grade T_{amb} = -40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current I_{EE}	4,37	220	290	370	mA	All inputs at -1.8V
Supply current I_{DD}	23	40	60	84	mA	Does not include ECL output current
Input HIGH voltage	FSI_{0-15},Clk	-1125		-880	mV	
Input LOW voltage	FSI_{0-15},Clk	-1810		-1520	mV	
Output HIGH voltage	26-34	-1125		-880	mV	Loaded with100Ω to -2V
Output LOW voltage	26-34	-1810		-1520	mV	Loaded with100Ω to -2V

Note: The SP2001 must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at Tamb > 85°Cfor DG package and >70°C for HG package. θ_{JA} DG = 36°C/W. θ_{JA} HG = 50°C/W

ABSOLUTE MAXIMUM RATINGS

Storage temperature	-65°C to 150°C
Max. junction temperature	+125°C
Max voltage between V_{EE} and V_{CC}	-7.0V to + 0.5V
Input voltage (DC)	V_{EE} to (V_{CC} + 0.5)V
Output current at V_O = V_{OH}	20mA

CIRCUIT DESCRIPTION

The SP2001 is a digital frequency synthesiser with an output frequency up to 100MHz. The channel spacing and minimum output frequency depend on the clock frequency, but with the clock set to 262.144 MHz the minimum output frequency and step size are 4kHz. The circuit needs no reactive components except power supply decoupling capacitors and is under full digital control at all times. Frequency accuracy is set by an external oscillator and close to carrier phase noise on the synthesiser output is dominated by the clock performance.

The fully digital system does not contain control loops so 'hop time' between discrete output frequencies is limited in principle only by the digital to analog converter settling time of about 5ns. In practice, to simplify the logic, a further delay of four clock periods has been added: the resultant delay of 20ns worst case is about five orders of magnitude faster than loop synthesisers. The block diagram (Fig. 2) shows the full DFS, including the recommended GPS SP98608 Digital to Analog Converter.

The function of the blocks can be seen from Fig.2. To avoid the need for a full 360 degrees in the ROM, the MSB output of the accumulator is used as a sign inverter, which with the LSBs, forms a digitised triangular number sequence. The MSB of the accumulator provides a square wave output via an ECL buffer which may be used as a variable clock in digital systems. The 1K ROM organised as 128x8 bits contains the data for 180 degrees stored in a cosine sequence which is read twice for each cycle of output data giving 256 words of data in total.

The data passes through retiming latches at each stage including the output in order to provide accurate data at the high clock rate; pipelined delays are unimportant in a non-looped system.

Finally the DAC reconstructs the output waveform, which consists of discrete points on the output sinusoid. Interpolation could be carried out by low pass filtering but in practice no filters are used except the inherent low pass action of the DAC.

Performance of the system is limited by the maximum update rate of the DAC used. The recommended SP98608 will typically update to ±½LSB at over 500MHz. When the clock is running at 327.68MHz, the DAC achieves 5-6 bits accuracy but is otherwise unimpaired in operation. Spur levels are frequency specific and are therefore difficult to measure and specify; also they are dependent on the performance of the output D-A converter. When using the GPS SP98608 450MHz DAC, the spur level remains close to the theoretical limit of -48dBc for an 8 bit system, for all output frequencies up to about 1/8 of the clock. At higher output frequencies around 1/4 of the clock, a spur with a frequency given by f_{CLOCK} -3 X f_{OUT} becomes significant when the clock frequency is greater than 100MHz. This spur has a level of approximately -47dBc at f_{CLOCK} = 100MHz degrading to -36dBc at f_{CLOCK} = 300MHz. When the input code is a whole binary number such as 0001 0000 0000 0000 the output will be free of spurs. Close to carrier noise is very good and is dominated by the clock source; measurements indicate a noise floor of better than -135 dBc/Hz at ±25kHz.

The set input (pin 22) provides a 'start from zero' as a test facility. It sets all the accumulator latches to zero so that the output of the ROM is all ones state.

The frequency equation is:

$$f_{OUT} = \frac{f_{CLOCK}}{2^{16}} \times Input\ Data$$

e.g. For 5kHz increments, f_{CLOCK} = 327.68MHz
For 3.125kHz increments, f_{CLOCK} = 204.8MHz

APPLICATIONS

A typical application circuit diagram is shown in figure 3, using the SP2001 in conjunction with a GPS SP98608 DAC. The eight ECL data outputs from the SP2001 are connected directly to the DAC inputs with 100Ω pull down resistors. The pull down resistors are essential as there are no internal loads for the ECL output transistors.

A square wave output is available from pin 26 which uses an identical output stage to those feeding the DAC. The load resistance can be reduced to 50Ω to allow feeding a terminated 50Ω line. In applications where the square wave output is not required, it may be left open circuit to reduce power consumption. When only the square wave output is required, the DAC drive outputs may be left open circuit.

In the application Fig. 3, the DAC is used in latched mode with the clock input feeding both the SP2001 and the DAC. The DAC may also be used in transparent mode by connecting pin 15 to ground and removing the clock, but performance will be slightly degraded when compared to the latched case.

The clock required in the Fig. 3 application is an ECL square wave. When a high frequency clock is required, a true ECL signal may be difficult to obtain and the arrangement shown in Fig. 4 will be more suitable. In this case, the the clock inputs to the SP2001 and DAC are biased to the centre of the ECL logic swing range (approximately -1.4V) using 68Ω and 180Ω resistors which also provide a 50Ω match to the clock input cable. A sine wave clock signal is AC coupled to the biased clock inputs by C1. The optimum clock input level is +4dBm which equals the nominal 1V p-p standard ECL logic swing.

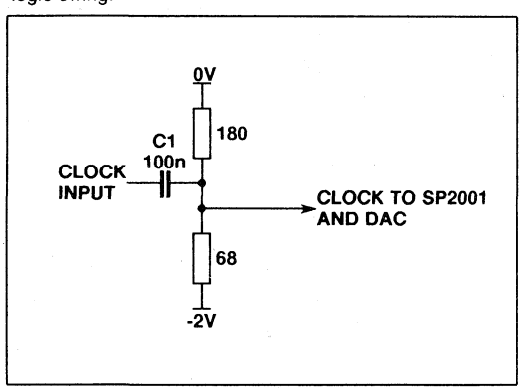


Fig. 4. Connection of high frequency sine wave clock

The Frequency Set data inputs to the SP2001 are ECL compatible with a nominal threshold voltage of about -1.4V and ECL data may be connected directly. Connection to CMOS input data is also straight forward provided the CMOS logic or microprocessor providing the data is operating from the -5.2V supply used by the SP2001. The arrangement is shown in figure 5.

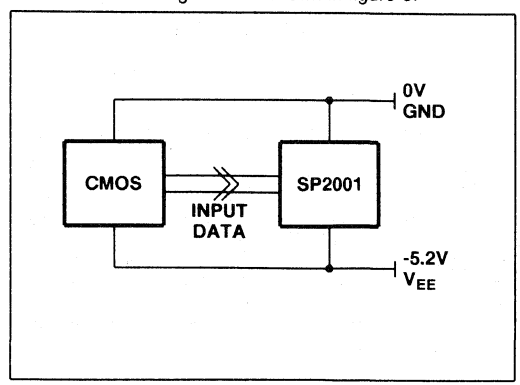


Fig. 5. Interface to CMOS logic

TTL drive logic may also be used in the same way as CMOS provided resistor pull ups are connected to the positive supply are used to ensure a logic high level close to the positive supply.

In order to obtain optimum performance, care should be taken with the layout of printed circuit boards. An earth plane as continuous as possible and common to both the SP2001 and the DAC should be used for the V_{CC} supply. The -5.2V V_{EE} and -2v V_{DD} supplies to both the SP2001 and the DAC should be decoupled close to the device pins preferably using surface mount 10nF capacitors. The eight ECL connections between the SP2001 and the DAC should be of equal length to ensure the input data is presented without time skew.

SP2002

350/400MHz DIRECT FREQUENCY SYNTHESISER

(Supersedes January 1991 Edition)

The SP2002 is a Direct Frequency Synthesiser (DFS) with square and selectable sine or triangular output waveforms available from on-chip 8-bit D-A converters.

The maximum programmable output frequency and resolution is dependent on the clock frequency. With a clock frequency of 1.074GHz the output frequency can be programmed in 0.5Hz steps from 0.5Hz to 268MHz by means of an externally applied binary word. Inputs are ECL 100k compatible.

The SP2002 is the first in a new range of DFS products.

FEATURES

- 400MHz Output Frequency
- In-Phase (I) and Quadrature (Q) Outputs
- 0.5Hz Resolution with 1074MHz Clock
- Sine, Square or Triangle Output

APPLICATIONS

- LO Synthesis in Frequency Agile Radio/Radar
- ECM/ECCM
- Deceptive Countermeasures
- Multi-Function Radio
- Instrumentation

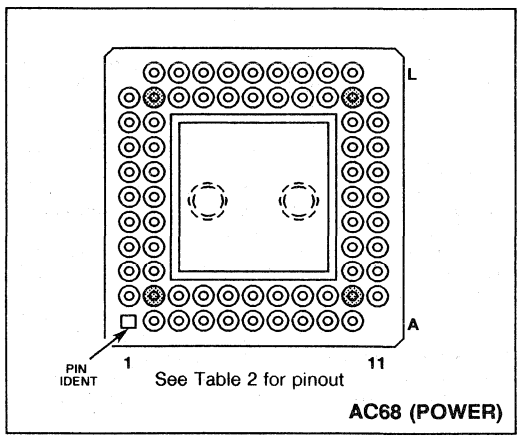


Fig.1 Pin connections - bottom view

ORDERING INFORMATION

SP2002 A AC
SP2002 B AC

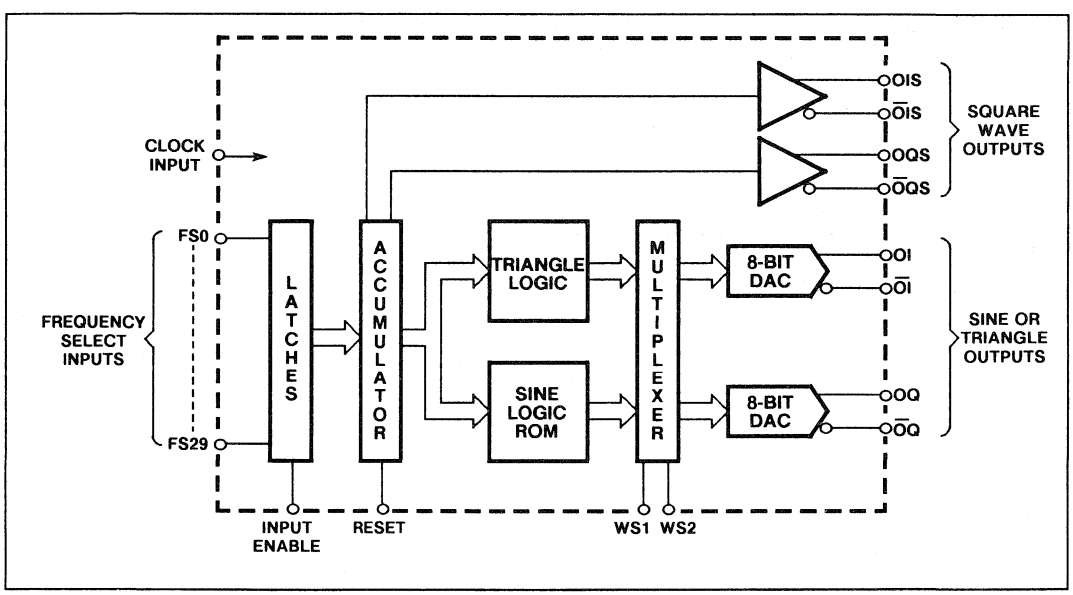


Fig. 2 SP2002 direct frequency synthesiser block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 25°C, V_{EE} = -4.5V, ±0.25V, V_{IH} = -1V, V_{IL} = -1.67V, A grade T_{case} = -55°C to +125°C, f_C = 1.4GHz.
B grade T_{case} = -40°C to +85°C, f_C = 1.6GHz

Characteristic	Signal Name	Value			Units	Conditions
		Min	Typ	Max		
Supply current	I_{EE}	0.95	1.15	1.35	A	Note 1
Sine/Triangle Output Current	$\overline{OQ}$, OQ $\overline{OI}$, OI	20	26	30	mA p-p	See Operating Notes, f_{OUT} = 3.125MHz
Square Wave Output Current	$\overline{OQS}$, OQS $\overline{OIS}$, OIS	8	14	20	mA p-p	See Operating Notes f_{OUT} = 3.125MHz
ECL Input Bias Current, all I/Ps except Clock	FS0-FS29 I/P EN, RESET		150		µA	
Waveform Select Input Current	WS1, WS2		1		mA	V_{IH} = 0V
Waveform Select Input High Voltage	WS1, WS2	-0.5V		0V	V	
Waveform Select Input Low Voltage	WS1, WS2	$-V_{EE}$		$-V_{EE}$ +0.5	V	
Clock Input Current	CLOCK		40		µA	
Output Frequency Range	All Outputs	1		400M	Hz	f_c = 1.6GHz, Note 2
Channel Spacing	All Outputs	0.5			Hz	f_c = 1.074GHz, Note 2
Close to Carrier Noise			-135		dBc/Hz	10kHz offset, Note 6
Spurious Output levels	Sine Output					In 10kHz Bandwidth
f_{out} ~6MHz				-46	dBc	Note 3, f_C = 1600MHz Decimal I/P code = 8389631
f_{out} ~125MHz				-42	dBc	Note 3, f_C = 1600MHz Decimal I/P code = 167773183
f_{out} ~200MHz				-21	dBc	Note 3, f_C = 1600MHz Decimal I/P code = 268436479
Frequency Change Range Time		8		40	Clock Cycle	Note 4
Package Thermal Resistance Chip to Case			2		°C/W	Note 5

NOTES

(1) The power taken by the synthesiser depends upon the 'Waveform Select' inputs (see Fig. 2). The I_{EE} current quoted is for the square wave plus sine wave 'I' and 'Q' outputs where all the SP2002 circuitry is powered up. The output waveform options and associated I_{EE} currents are shown in Table 1. (2) The SP2002 will operate at any clock frequency below 1.6 GHz e.g. at f_c = 214MHz, output frequency range = 0.1Hz to 50MHz in steps of 0.1Hz. (3) Levels refer to the highest rather than total spurious power. A sine wave output and clock frequency of 1.6 GHz is assumed. These figures will degrade by 10 to 20dB for triangle and 20 to 30dB for square wave output. (4) Minimum figure assumes only MSB Frequency Set Input is changed. Maximum figure assumes LSB Frequency Set Input is changed. (5) A suitable heatsink should be attached to the studs on the top of the package. (6) Assuming no spurious output at the offset frequency.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	-65°C to +150°C
Supply voltage (V_{EE})	-6V
Input voltages	V_{EE} to +0.5V
Junction temperature	+150°C

CIRCUIT DESCRIPTION

The sine, triangle or square wave output frequency is determined by a parallel 30 bit Frequency Set binary input word. With a clock input rate of 1.074GHz, the output frequency can be incremented in 0.5Hz steps from 0.5Hz to 268MHz. In phase ('I') and Quadrature ('Q') outputs are provided for all three waveform options, as are true and complementary phase outputs. Due to the internal organisation of the chip the maximum output frequency is limited to a quarter of the clock frequency.

Referring to the block diagram of Fig. 2, Waveform Select (WS) pins are provided to enable programming of different output waveform combinations by hard-wiring to the supplies as shown (see Table 1). Depending on the output option chosen, unused circuitry on-chip is automatically turned off to conserve power.

A Reset input is provided to initialise the internal circuits and allow the output waveforms to start from a known state as shown in Fig. 4. Input Frequency Set data can be latched if required, by holding the Input Enable pin high.

Referring to Fig. 2, the basic operation is as follows. Frequency Set data is entered via the data latches to an accumulator which is incremented by the clock input.

The accumulator MSB output provides the square wave. The 8 MSB outputs are used to generate the sine and triangle functions. The output of the accumulator is effectively a sawtooth which is converted to a triangle by the triangle logic. The sinewave is generated by circuitry including a ROM containing a quadrant of sinewave data which, with the associated logic, produces a complete sinewave in digital form. A multiplexer selects triangle or sine output under the control of the Waveform Select pins. The analog triangle or sine outputs are generated via 8-bit DACs.

OPERATING NOTES

The SP2002 is a very high speed ECL circuit with a maximum clock frequency in excess of 1.6GHz and output frequency capability above 400MHz. In order to achieve correct operation at these frequencies and to ensure output waveform integrity, attention must be paid to the layout of the application board. The use of a ground plane and good RF techniques is recommended. Power supply pins should be well decoupled using high frequency capacitors. All power supply and ground pins must be connected.

The clock input is ECL100K compatible and if a relatively low frequency clock is required the input may be driven directly from a ECL100K gate with a 50 Ohm termination resistor to -2V mounted close to the clock pin. At frequencies greater than a few hundred MHz, clock drive from ECL is not practicable and a sinewave drive ac-coupled to the clock input may be used. The application diagram in figure 4 shows a typical arrangement where the 68 Ohm and 160 Ohm resistors set a suitable bias voltage for the clock input and also provide a 50 Ohm termination for the connecting cable or stripline. A suitable drive level is +4dBm or 1V p-p, but at very high clock frequencies this may need to be increased by a few dB to make up for losses.

The frequency set, input enable and reset inputs are ECL100K compatible, and when very fast frequency hopping is required, for instance when generating chirp waveforms the input data will necessarily come from an ECL source. Many other applications may require much slower data which may be generated from a CMOS source. CMOS data cannot be connected directly to the SP2002 inputs since the high logic is equal to the positive supply which would saturate the input transistors and cause the circuit to malfunction.

A possible interface to CMOS logic is shown in Fig. 3 where the CMOS positive power rail is dropped approximately 0.7V below that feeding the SP2002 by including a diode in series with the CMOS supply.

The low logic level for the SP2002 may be equal to the V_{EE} supply but should not be taken more negative.

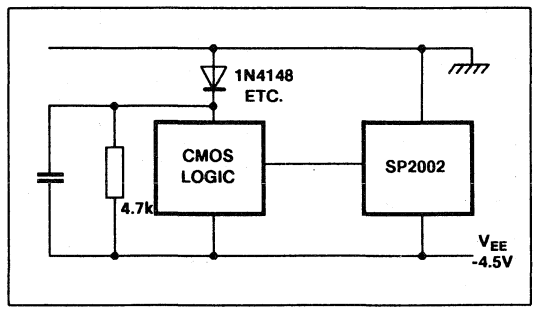


Fig. 3 Interface to CMOS Logic

The output frequency and step size is a function of the clock rate and the frequency select data. The output frequency can be calculated from the formula

$$fout = \frac{Kfc}{2^N} \text{ where } N = 31, \text{ the number}$$

of bits in the accumulator, fc is the clock frequency and K the number on the frequency select inputs.

The minimum output frequency and step size are given by

$$fmin = \frac{fc}{2^N}$$

The reset pin sets the 31 bit accumulator to zero regardless of the state of any other inputs.

The input is active high and when reset, the sine triangle and square wave outputs remain at the level obtained when the accumulator reaches zero in dynamic operation. The effect of the Input enable and Reset inputs is shown diagramatically in Fig. 4.

All the outputs are current sources, the sine and triangle outputs being obtained from the DAC outputs whilst the square wave outputs are fed from a separate buffer circuit driven direct from the accumulator MSB. Normally the output signal is obtained by loading the output with a 50 Ohm resistor to ground, but in practice the resistor can be any value from zero to 50 Ohms allowing control of the output voltage. If necessary the output load resistor can be returned to an output voltage up to 1V more positive than ground. This feature may be used to produce output signals symmetrical about ground, in the case of the sine triangle outputs, 50 Ohm resistors connected to +0.5V will produce ≃ 1V peak to peak output centred about ground.

A heatsink is required to maintain the chip operating temperature at a safe value. The heatsink should be attached to the studs on the top of the package using M3 nuts. A thermal resistance of 10°C/W is suitable for operation at 25°C.

The frequency select input is positive logic, ie the minimum output frequency is obtained when the LSB is high and all other inputs low.

All frequency select inputs have a nominal 30K input pull down resistor to V_{EE} and will therefore be pulled low if left open circuit.

The waveform select pins WS1 and WS2 are intended to be hard wired to V_{EE} or ground depending on the output waveform requirements. When necessary, the inputs could be switched using external transistors provided the minimum level requirements specified in the table of characteristics are met. The waveform select inputs should not be left open circuit.

The input Enable pin controls entry of input data to the input latches. When the input is low the input latches are transparent and any data change results in a change to the output frequency. When the input is taken high the data present on the frequency select inputs before the low to high transition is retained on the input latches and sets the output frequency.

The frequency select input can be changed without changing the output frequency until the frequency select input is again taken low, and the new data enters the latches. The Input Enable pin has an internal nominally 30K pull down resistor to V_{EE} and will therefore go low if left open circuit.

Waveform Select input		Output waveform selected	I_{EE} (A) TYP	Power (W)
WS1	WS2			
V_{EE}	V_{EE}	Square wave 'I' and 'Q' Triangle 'I' and 'Q'	1.0	4.5
GND	V_{EE}	Square wave 'I' and 'Q' Sine wave 'I'	1.0	4.5
V_{EE}	GND	Square wave 'I and Q'	0.8	3.6
GND	GND	Square wave 'I' and 'Q' Sine wave 'I' and 'Q'	1.1	5.0

Table 1 Output waveform options

Pin No.	Pin name	Pin No.	Pin name
B1	WS2	K11	FS23
B2	WS1	K10	FS24
C1	TDI	J11	FS25
C2	TRC	J10	FS26
D1	RESET	H11	FS27
D2	GND	H10	FS28
E1	GND	G11	FS29
E2	V_{EE}	G10	I PEN
F1	GND	F11	CLOCK
F2	FS0	F10	V_{EE}
G1	FS1	E11	GND
G2	FS2	E10	GND
H1	FS3	D11	GND
H2	FS4	D10	TOQ
J1	FS5	C11	TOI
J2	FS6	C10	$\overline{O}$QS
K1	FS7	B11	OQS
L2	FS8	A10	$\overline{O}$IS
K2	FS9	B10	OIS
L3	FS10	A9	IC
K3	FS11	B9	NC
L4	FS12	A8	$\overline{O}$Q
K4	FS13	B8	OQ
L5	FS14	A7	NC
K5	GND	B7	V_{EE}
L6	V_{EE}	A6	GND
K6	FS15	B6	IC
L7	FS16	A5	NC
K7	FS17	B5	$\overline{O}$I
L8	FS18	A4	OI
K8	FS19	B4	NC
L9	FS20	A3	V_{EE}
K9	FS21	B3	GND
L10	FS22	A2	NC

Table 2 SP2002 pin assignment. 'IC' (internal connection) pins are not required for normal use but should be left open.

Pin name	Function
WS1, WS2	Waveform select, see Table 1.
TDI, TRC, TOQ,TOI	Test pins only. Not required for normal operation. Leave open circuit.
RESET	A logic '1' on this pin resets the accumulator
FS0-FS29	Frequency Select inputs. FS0 is the LSB.
I PEN	Frequency Select Input Enable. A logic '1' on this pin latches data into the accumulator.
CLOCK	Clock input.
OQS, OIS	Square wave outputs.
OQ, OI	Sine or triangle outputs.
GND	0V
V_{EE}	Negative power supply (-4.5V).
NC	Not connected.
NC*	These pins are not required for normal use but should be left open.

Table 3 SP2002 pin descriptions

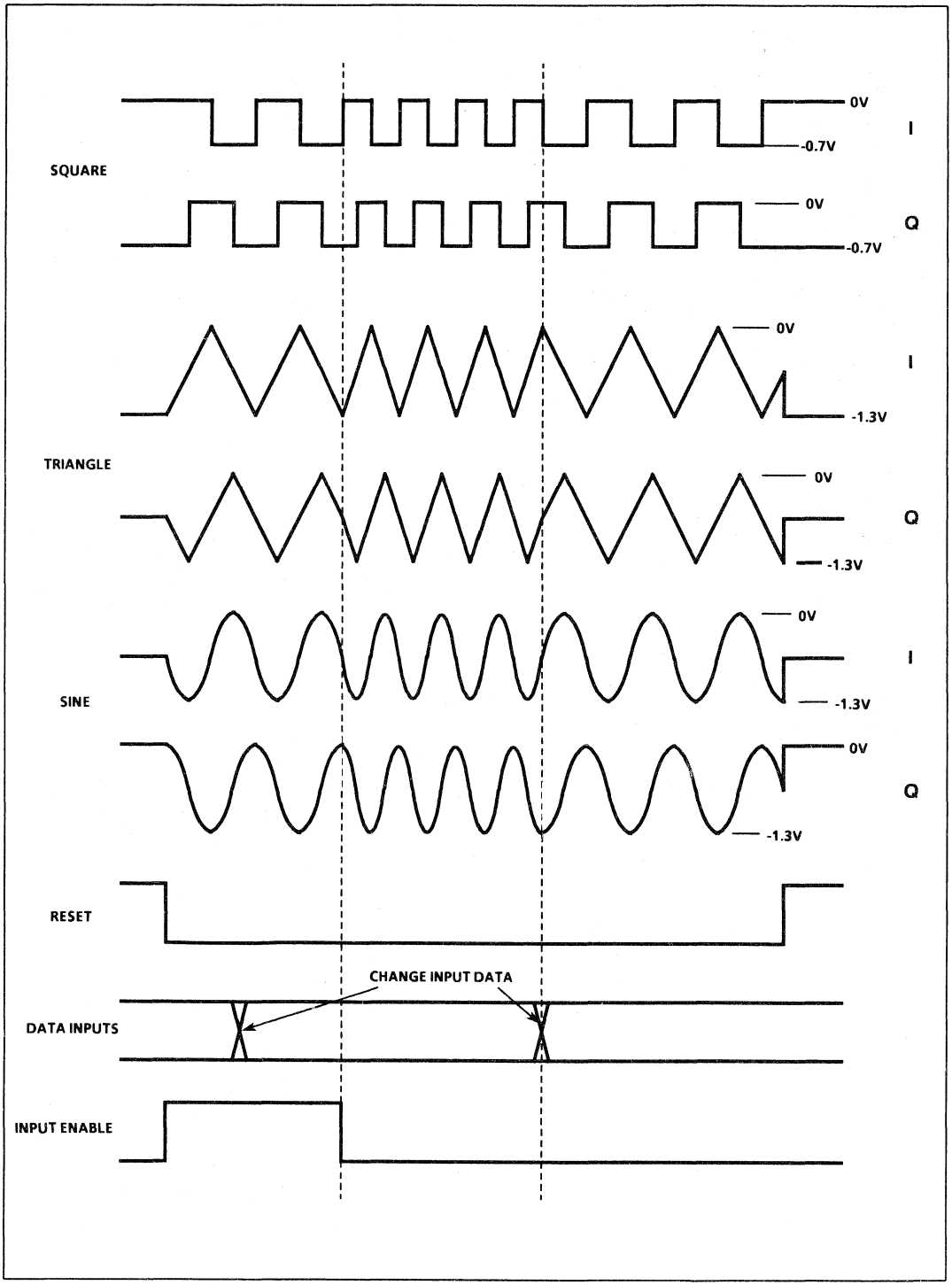
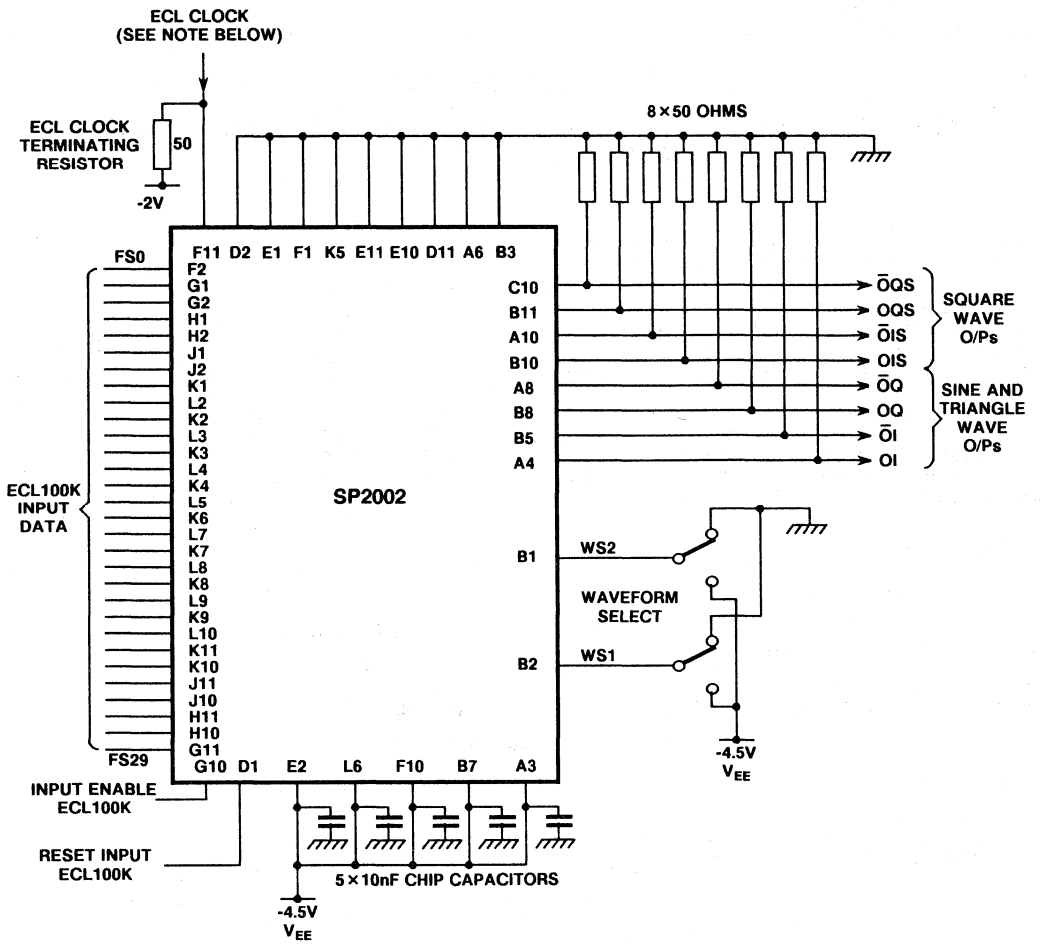


Fig. 4 SP2002 timing and waveform diagram.



NOTE

The clock input may be ECL level DC-coupled as shown above or a sinewave input of 1V peak-to-peak amplitude AC-coupled. When sinewave drive is used the input should be biased to -1.3V and the input cable terminated close to the IC with 50 ohms.

Minimum operating frequency with sinewave drive is 50MHz.

Use chip components mounted as close as possible to the IC pins.

Typical sinewave clock bias and termination circuit

Fig. 5 SP2002 typical application circuit

NJ8821

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH RESETTABLE COUNTERS

The NJ8821A is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

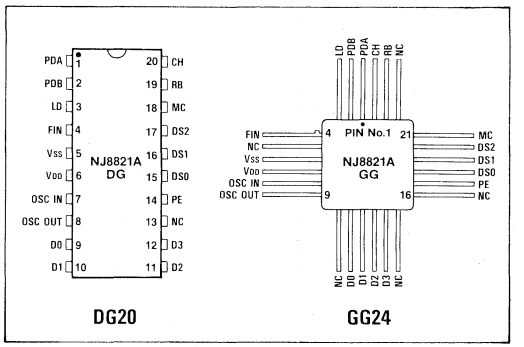


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- >10MHz Input Frequency
- Military Temperature Range (-55°C to +125°C)

ORDERING INFORMATION

NJ8821 A DG
NJ8821 A GG
NJ8821 AB DG

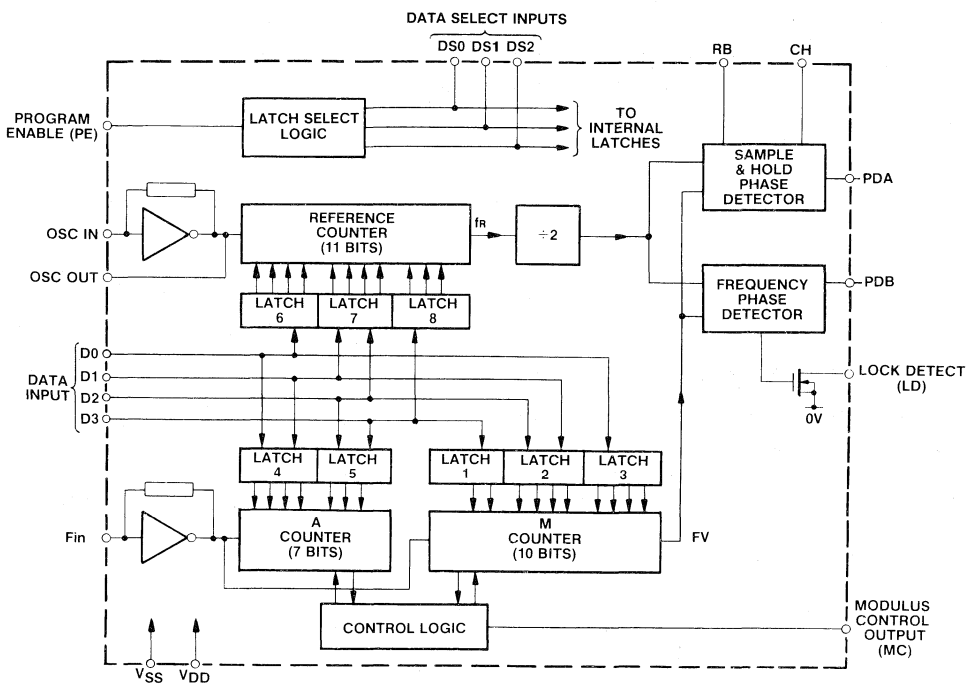


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} - V_{SS} 5V ± 0.5V
Temperature range -55°C to +125°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	7.0	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	2.0	mA	FOSC, FIN = 1.0MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 4mA
Low level			0.4	V	I_{sink} 4mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}.Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No. GG	Pin No. DG	Name	Description
1	1	PDA	Analogue output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
6	5	V_{SS}	Negative supply (normally ground)
7	6	V_{DD}	Positive supply
8,9	7,8	OSC.IN OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The programme range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
11,12,13,14	9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
17	14	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines
18,19,20	15,16,17	DS0-DS2	Data-select inputs to control the addressing of data latches.
21	18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The programme range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ⩾A. Where every possible channel is required, the minimum division ratio should be N^2-N.
23	19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
24	20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C

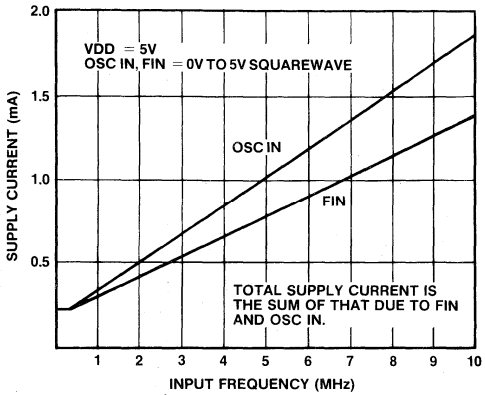


Fig.3 Typical supply current versus input frequency

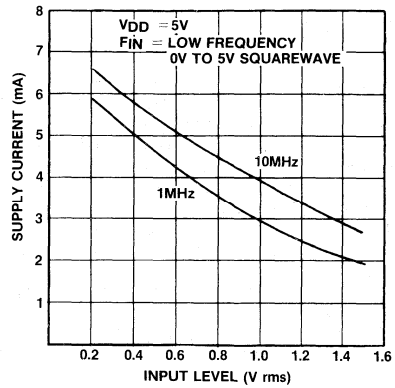


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information is given in Fig.6.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec. If shorter lock up times are required, when making only small changes in frequency, the non-resettable version NJ8823 should be considered.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

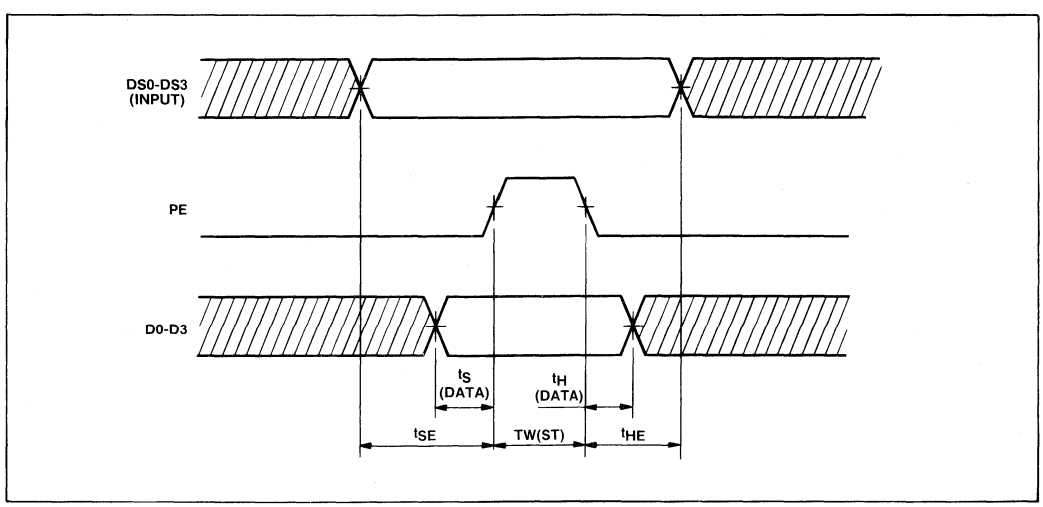


Fig.6 Timing diagram

PHASE COMPARATORS

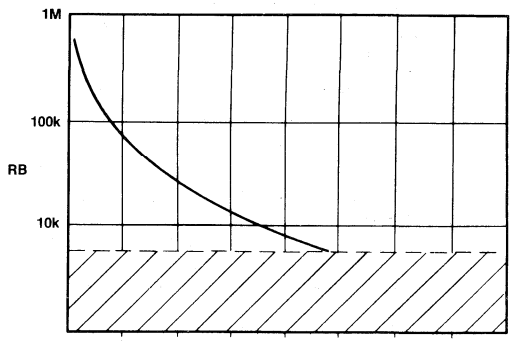
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-½})]}{2 \times \pi\ 50\times10^{-12} \times RB\times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

NJ88C22

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH RESETTABLE COUNTERS

The NJ88C22 is a synthesiser circuit fabricated on the Plessey small geometry CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable refrence divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters subsequent updating can be abbreviated to 17 bits when only the 'A' and 'M' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8705 series to produce a universal binary coded synthesiser for up to 1100MHz operation.

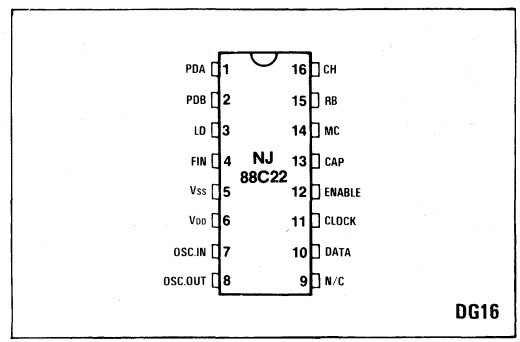


Fig.1 Pin connections - top view, not to scale

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- > 10MHz Input Frequency
- Military Temperature Range (-55°C to +125°C)

ORDERING INFORMATION

NJ88C22 AA DG

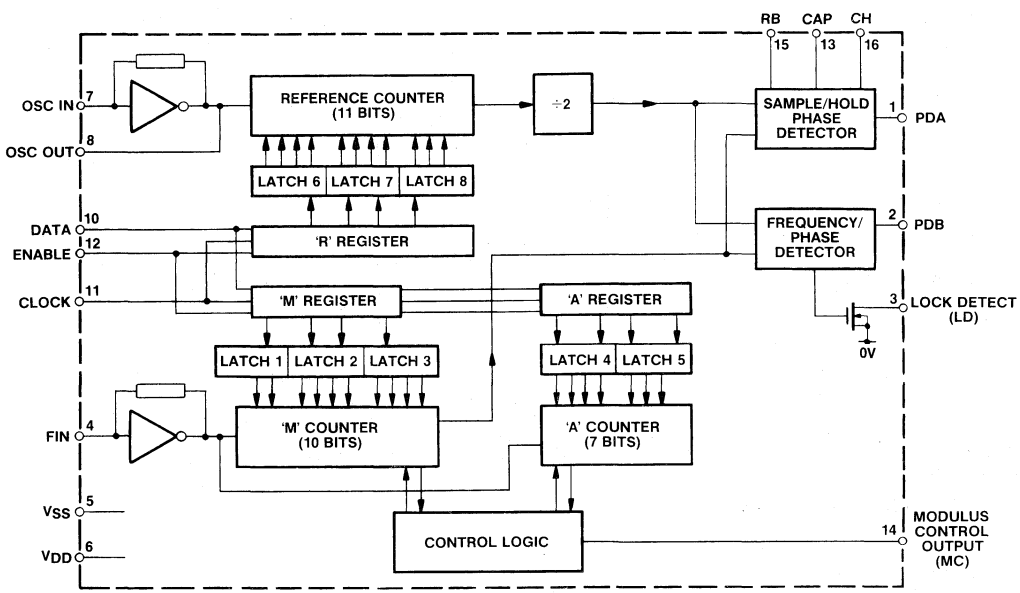


Fig.2 Block diagram.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range -55°C to +125°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		6.3	7.0	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	2.0	mA	FOSC, FIN = 1MHz }
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB OUTPUT					
High level	4.6			V	I_{source} 4mA
Low level			0.4	V	I_{sink} 4mA
3-state leakage			±250	nA	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}, 25°C
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{CH}	0.5			µs	
Clock low time, t_{CL}	0.5			µs	All timing periods are referenced to the negative transition of the clock waveform
Enable set-up time, t_{ES}	0.2		t_{CH}	µs	
Enable hold time, t_{EH}	0.2			µs	
Data set-up time, t_{DS}	0.2			µs	
Data hold time, t_{DH}	0.2			µs	
Clock rise and fall times	0.2			µs	
Positive going threshold, V_{T+}			V_{DD}-0.8	V	Note 1
Negative going threshold, V_{T-}	0.8			V	
Hysteresis	1.0			V	
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull up resistors. They are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). **In a type 2 loop, this pin is at (V_{DD} - V_{SS})/2 when the system is in lock.**
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
5	V_{SS}	Negative supply (ground).
6	V_{DD}	Positive supply (normally 5V).
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 ohm resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
9	N/C	Not connected.
10	DATA	Information on this pin is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are three data words which control the NJ88C22 : 'A' (7 bits), 'M' (10 bits) and 'R' (11 bits); MSB is first in the order.
11	CLK	Data is clocked in on the negative transition of the clock waveform. If less than 28 negative clock transitions have been received when the enable line goes low (i.e. only 'M' and 'A' will have been clocked in) then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted then the 'R' counter will be loaded with the new data.
12	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock input are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions only allowed when CLK is high.
13	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷ 128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M ⩾ A. Where every possible channel is required, the minimum division ratio should be $N^2 - N$.
15	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	CH	An external hold capacitor should be connected between this pin and V_{SS}.

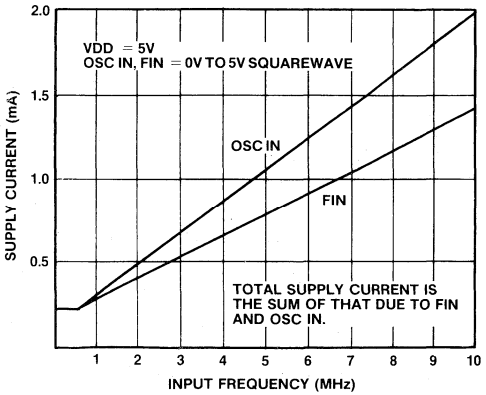


Fig.3 Typical supply current v. input frequency

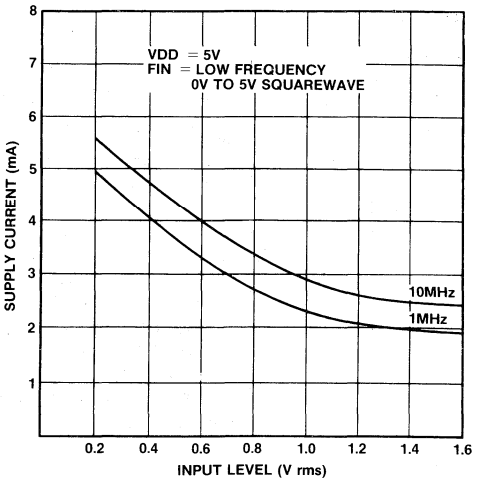


Fig.4 Typical supply current v. input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N+1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127.
Note $M \geqslant A$

$$\text{Also } P = \frac{f_{VCO}}{f_{comp}}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \quad \text{therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required divide ratio.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec.

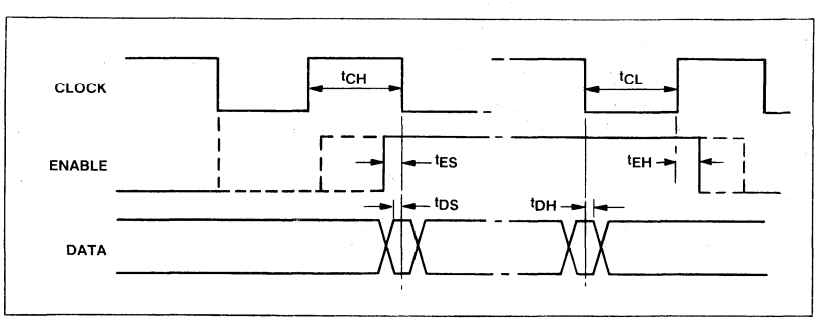


Fig.5 Timing diagram showing timing periods required for correct operation

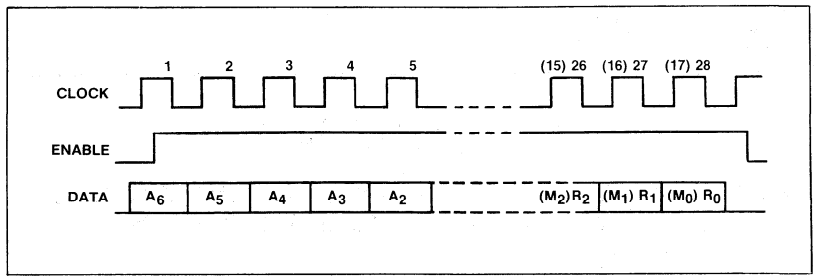


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K\Phi K_V/P$, where $K\Phi$ is phase detector constant (volts/rad), K_V is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ88C22 has both a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-1/2})]}{2\pi\,[CAP + 50\times10^{-12}] \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used. Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

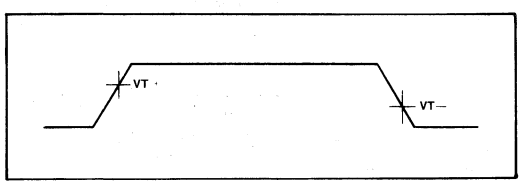


Fig.7 Timing diagram showing voltage thresholds

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

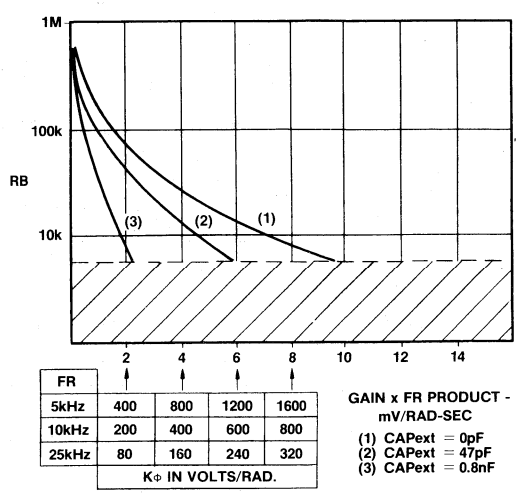


Fig.8 RB v. gain and reference frequency

NJ88C24

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE) WITH NON-RESETTABLE COUNTERS

The NJ88C24 is a synthesiser circuit fabricated on the Plessey small geometry CMOS process and is capable of achieving high sideband attenuation and low noise performance. It contains a reference oscillator, 11-bit programmable refrence divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters subsequent updating can be abbreviated to 17 bits when only the 'A' and 'M' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8705 series to produce a universal binary coded synthesiser for up to 1100MHz operation.

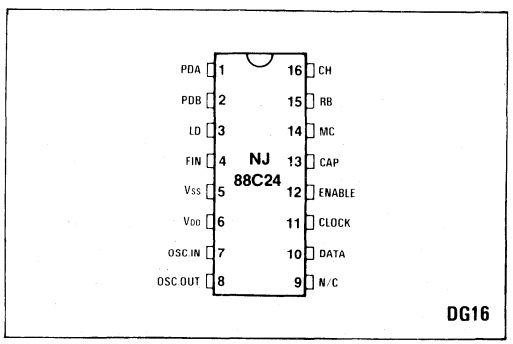


Fig.1 Pin connections - top view, not to scale

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- > 10MHz Input Frequency
- Military Temperature Range (-55°C to +125°C)

ORDERING INFORMATION

NJ88C24 AA DG

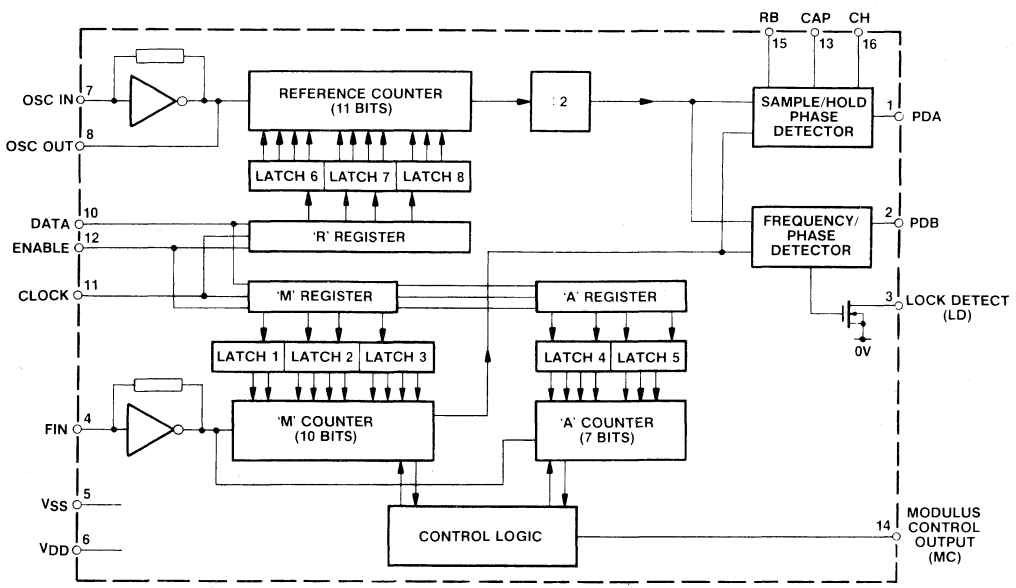


Fig.2 Block diagram.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range -55°C to +125°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		6.3	7.0	mA	FOSC, FIN = 10MHz } 0 to 5V square wave
		0.7	2.0	mA	FOSC, FIN = 1MHz } 0 to 5V square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB OUTPUT					
High level	4.6			V	I_{source} 4mA
Low level			0.4	V	I_{sink} 4mA
3-state leakage			±250	nA	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}, 25°C
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming inputs					
Clock high time, t_{CH}	0.5			µs	
Clock low time, t_{CL}	0.5			µs	All timing periods are referenced to the negative transition of the clock waveform
Enable set-up time, t_{ES}	0.2		t_{CH}	µs	
Enable hold time, t_{EH}	0.2			µs	
Data set-up time, t_{DS}	0.2			µs	
Data hold time, t_{DH}	0.2			µs	
Clock rise and fall times	0.2			µs	
Positive going threshold, V_{T+}			V_{DD}-0.8	V	Note 1
Negative going threshold, V_{T-}	0.8			V	
Hysteresis	1.0			V	
Phase Detector					
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	≈nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data, Clock and Enable inputs are high impedance Schmitt buffers without pull up resistors. They are therefore not TTL compatible.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). **In a type 2 loop, this pin is at (V_{DD} - V_{SS})/2 when the system is in lock.**
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
5	V_{SS}	Negative supply (ground).
6	V_{DD}	Positive supply (normally 5V).
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 ohm resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 3 to 2047 in steps of 1, with the division ratio being twice that programmed.
9	N/C	Not connected.
10	DATA	Information on this pin is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are three data words which control the NJ88C24 : 'A' (7 bits), 'M' (10 bits) and 'R' (11 bits); MSB is first in the order.
11	CLK	Data is clocked in on the negative transition of the clock waveform. If less than 28 negative clock transitions have been received when the enable line goes low (i.e. only 'M' and 'A' will have been clocked in) then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted then the 'R' counter will be loaded with the new data.
12	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock input are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions only allowed when CLK is high.
13	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷ 128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M ≥ A. Where every possible channel is required, the minimum division ratio should be $N^2 - N$.
15	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	CH	An external hold capacitor should be connected between this pin and V_{SS}.

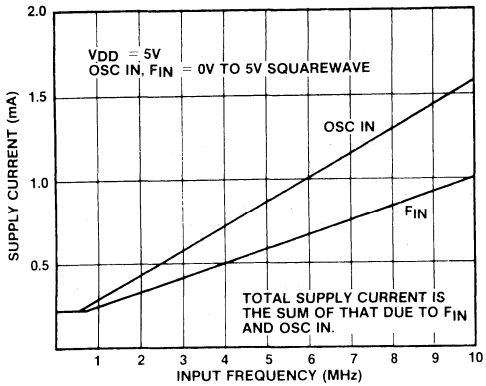


Fig.3 Typical supply current v. input frequency

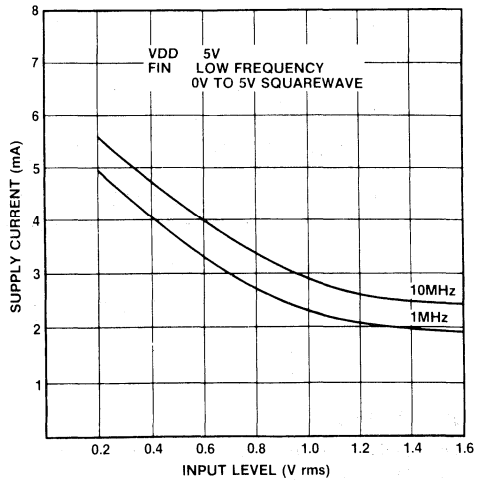


Fig.4 Typical supply current v. input level, Osc In

PROGRAMMING

Reference Divider Chain

The comparison frequency depends upon the crystal oscillator frequency and the division ratio of the R counter, which can be programmed in the range 3 to 2047.

$$R = \frac{fosc}{2 \times fcomp}$$

ie where *fcomp* = comparison frequency
fosc = oscillator frequency
R = R counter ratio

For example where crystal frequency = 10MHz and a channel spacing comparison frequency of 12.5kHz is required,

$$R = \frac{10^7}{2 \times 12.5 \times 10^3} = 400$$

Thus the R register would be programmed to 400 expressed in binary.
NB The total divider range is from 6 to 4094 in steps of 2.

VCO Divider Chain

The synthesised frequency of the voltage control oscillator (VCO) will depend on the division ratio of the M and A counters, the value of the external two modulus prescaler ($N/N + 1$) and the value of the comparison frequency *fcomp*.

The division ratio $P = NM + A$
where *M* is the ratio of the M counter in the range 3 to 1023 and *A* is the ratio of the A counter in the range 1 to 127.
Note $M \geqslant A$

$$\text{Also } P = \frac{f_{VCO}}{f_{comp}}$$

For example if the desired VCO frequency = 275MHz, the comparison frequency is 12.5kHz and a two modulus prescaler of ÷64/65 is being used, then:

$$P = \frac{275 \times 10^6}{12.5 \times 10^3} = 22 \times 10^3$$

Now $P = NM + A$
which can be rearranged to be $P/N = M + A/N$
In our example we have

$$\frac{22 \times 10^3}{64} = M + \frac{A}{6} \quad \text{therefore } 343.75 = M + \frac{A}{64}$$

M is programmed to the integer part = 343 and *A* is programmed to the fractional part times 64
ie $A = 0.75 \times 64 = 48$
NB The minimum ratio that can be used is $N^2 - N$
To check $P = 343 \times 64 + 48 = 22000$ which is the required divide ratio.

When re-programming, the counters are changed only when they reach a zero state. There is no reset to zero state. This means the synthesiser loop lock up time will be variable. For the case when only small changes in frequency are required, the non-resettable synthesiser should achieve the shortest loop lock up times.

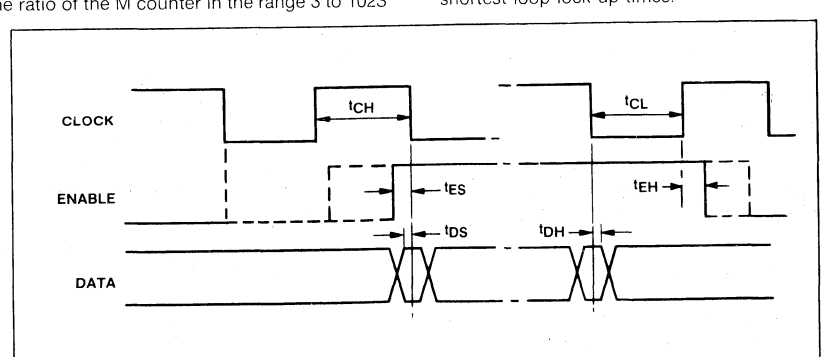


Fig.5 Timing diagram showing timing periods required for correct operation

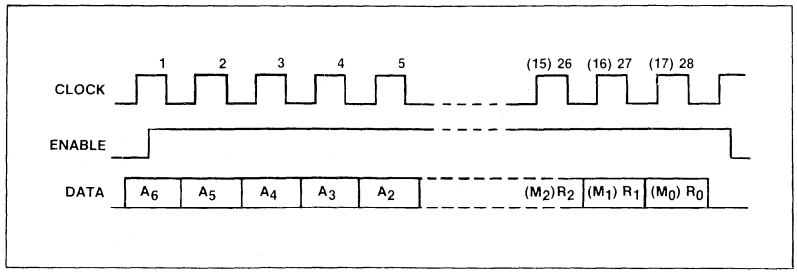


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K_\Phi K_V/P$, where K_Φ is phase detector constant (volts/rad), K_V is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ88C24 has both a high gain and uses a double sampling technique to reduce spurious outputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-1/2})]}{2\pi\,[CAP + 50\times10^{-12}] \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used. Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

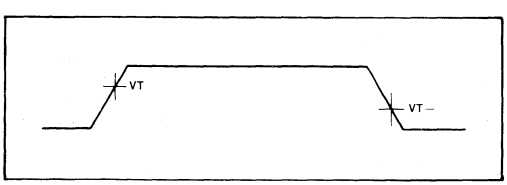


Fig.7 Timing diagram showing voltage thresholds

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

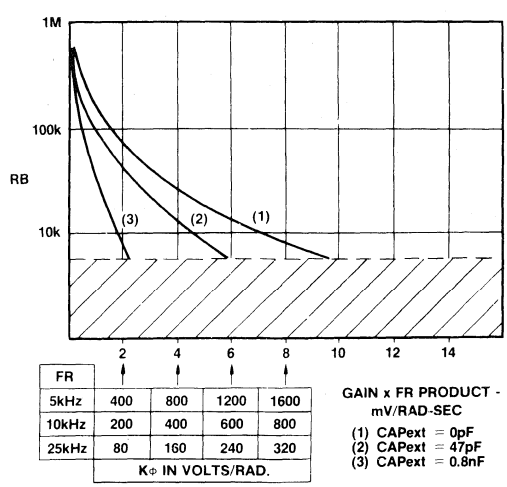


Fig.8 RB v. gain and reference frequency

Section 3

Technical Data: Frequency dividers

MIL-STD-883C Class B

Many of the integrated circuits detailed in this section are available screened in conformance with MIL-STD-883C Class B and are identified in their ordering codes by the letters **AC** immediately following the device type number. Separate data sheets for these circuits are available from your local GEC Plessey Semiconductors Sales Office.

SP8643

350MHz ÷ 10/11

The SP8643 is an ECL variable modulus divider, with ECL 10K compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC coupled, with externally-applied bias.

FEATURES

- ECL Compatible Inputs/Outputs
- AC Coupled Input (External Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 260mW
- Temperature Range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

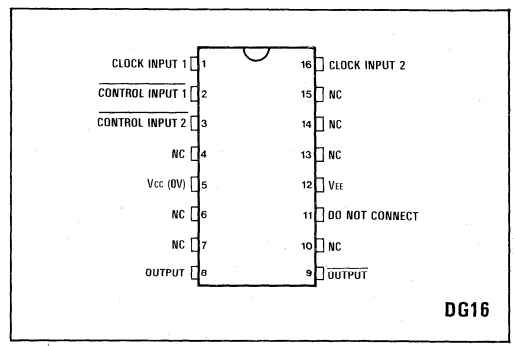


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP8643 A DG
SP8643 AB DG
SP8643 AC DG

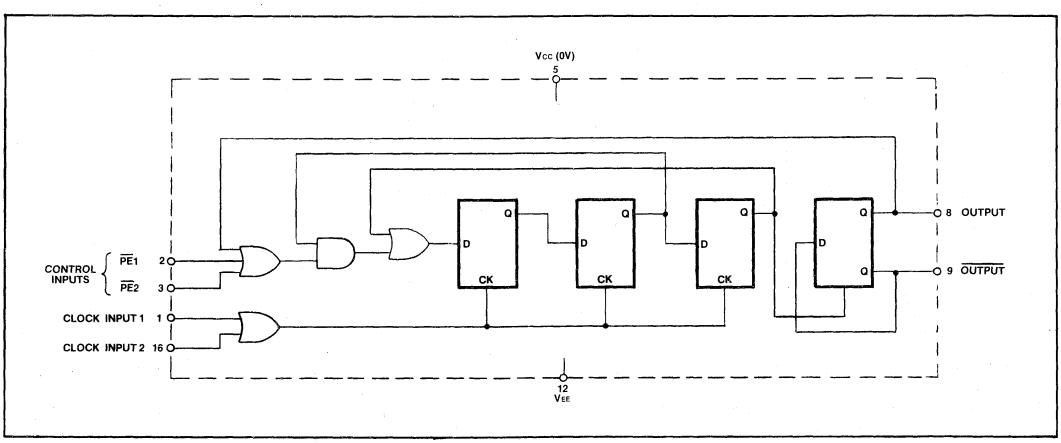


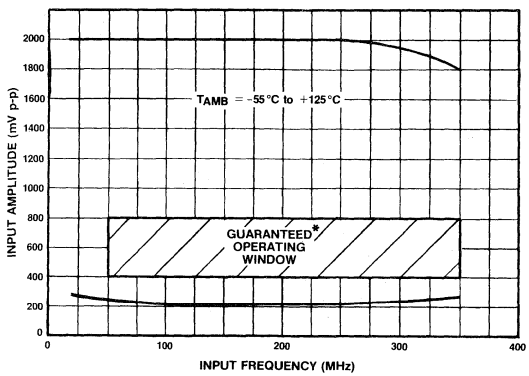
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	350		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25° C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25° C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25° C)	
Clock to ECL output delay	t_p		6	ns		Note 6
Set-up time	t_s	2.5		ns		Note 6
Release time	t_r	3		ns		Note 6

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L ⟶ H transition of control input and the next L ⟶ H clock pulse transition to ensure that ÷10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H ⟶ L transition of the control input and the next L ⟶ H clock pulse transition to ensure that the ÷11 mode is obtained.
6. Guaranteed but not tested.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8643A

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

OPERATING NOTES

1. The clock and control inputs are ECL III compatible. There is an internal pulldown resistor to V_{EE} of 4.3k on each input and therefore any unused input can be left open circuit when not in use but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity. If it is desirable to capacitively couple the signal source to the clock input then an external bias is required as shown in Fig. 6. The external bias voltage should be -1.3V at 25°C.
2. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. Input impedance is a function of frequency. See Fig. 5.
5. All components should be suitable for the frequency in use.

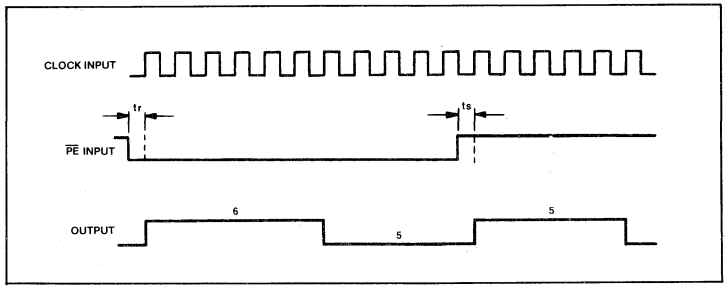


Fig.4 Timing diagram

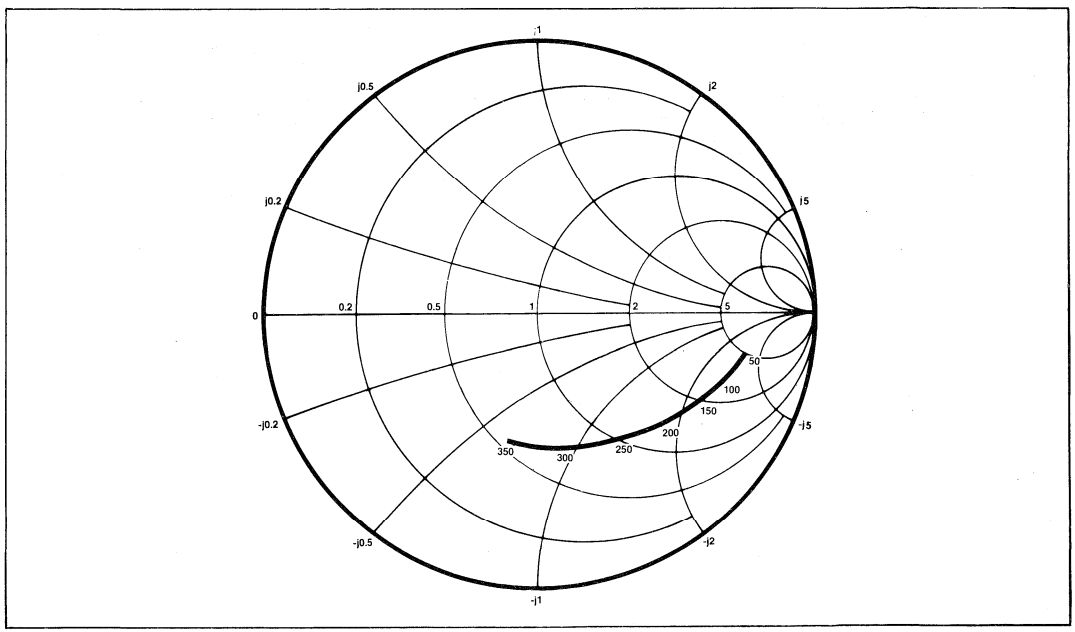


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

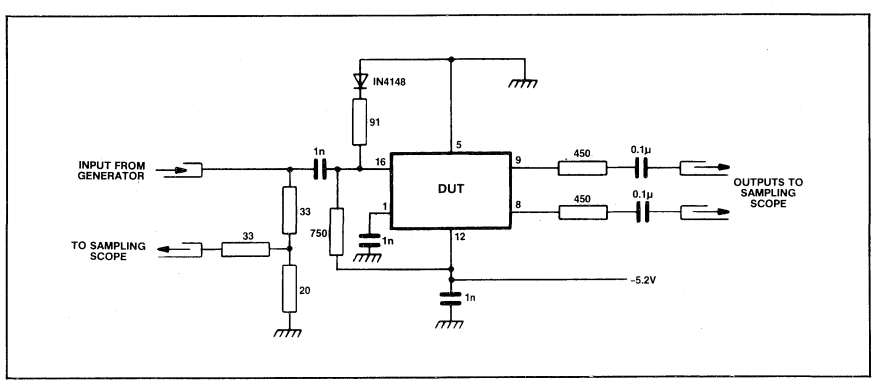


Fig.6 Test circuit

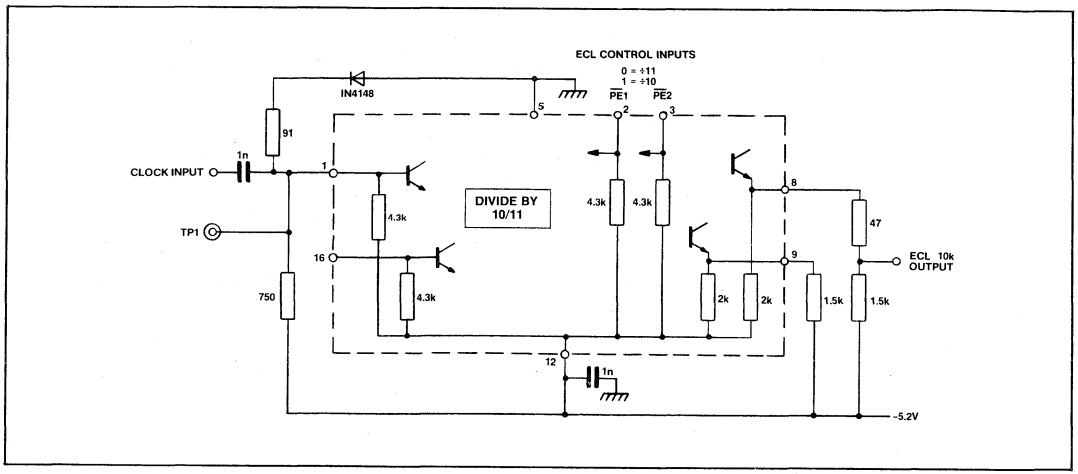


Fig.7 Typical application using ECL outputs. NB Voltage at TP1 should be -1.3V at 25°C

SP8647

250MHz ÷ 10/11

The SP8647 is an ECL variable modulus divider, with ECL 10K and TTL/CMOS compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC coupled, with externally-applied bias.

FEATURES

- ECL Compatible Inputs/Outputs
- Open Collector TTL/CMOS Output
- AC Coupled Input (External Bias)

QUICK REFERENCE DATA

- Supply Voltage V_{CC}-V_{EE} : 5.2V ± 0.25V
- Power Consumption: 260mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} - V_{EE}	8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Open collector voltage (Pin 11)	+12V
Max. clock I/P voltage	2.5V p-p
Max. open collector current	15mA

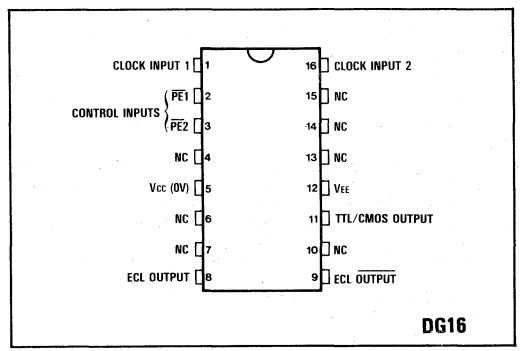


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP8647 A DG
SP8647 B DG
SP8647 AB DG
SP8647 AC DG
SP8647 ABSS2 DG

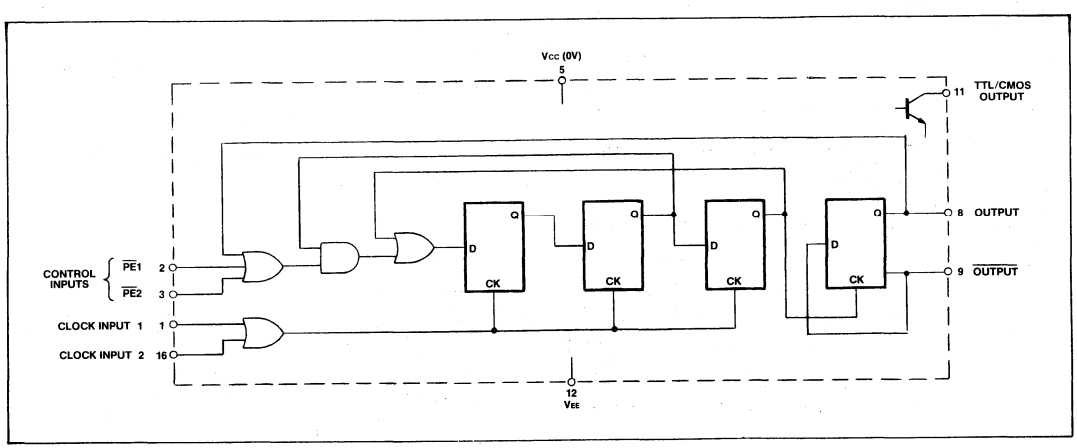


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS (ECL OPERATION)

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV p-p	Note 6
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 6
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	Note 6
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Clock and $\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
Clock and $\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		6	ns		Note 7
Set-up time	t_s	2.5		ns		Note 7
Release time	t_r	3		ns		Note 7

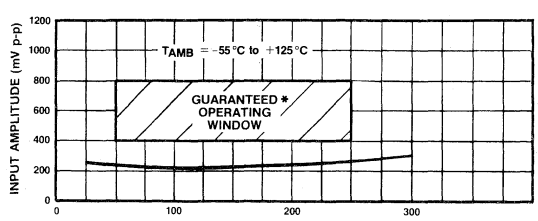
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L → H transition of control input and the next L → H clock pulse transition to ensure that ÷10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H → L transition of the control input and the next L → H clock pulse transition to ensure that the ÷11 mode is obtained.
6. SP8647B tested at 25°C only.
7. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS (TTL OPERATION)

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		65	mA		Note 3
TTL output low voltage	V_{OL}		0.5	V	V_{CC} = +5.25V Sink current = 8mA	Note 3, 5
TTL output high voltage	V_{OH}	3.5		V	V_{CC} = +5.0V	Note 3, 5
Clock to TTL output high delay (positive going)	t_{PLH}		15	ns		Note 4
Clock to TTL output low delay (negative going)	t_{PHL}		15	ns		Note 4
Set-up time	t_s	2.5		ns		Note 4
Release time	t_r	3		ns		Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. SP8647B tested at 25°C only.
4. Guaranteed but not tested.
5. TTL output for use up to 15MHz output frequency. $C_{load} \leq 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8647A

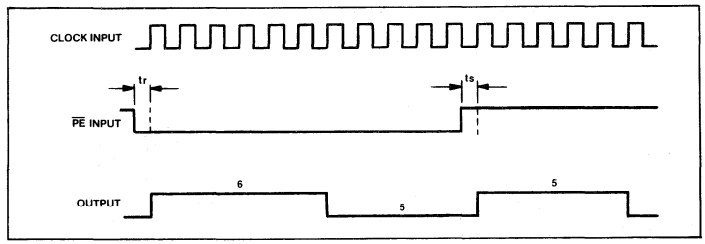


Fig.4 Timing diagram

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

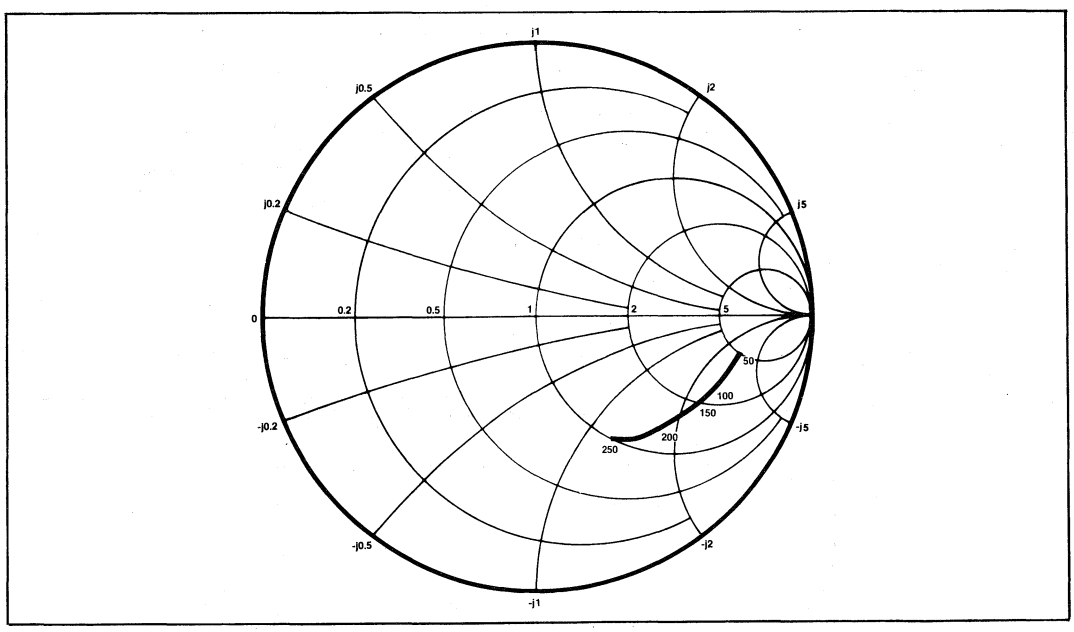


Fig.5 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock and control inputs are ECL III compatible. There is an internal pulldown resistor to V_{EE} of 4.3k on each input and therefore any unused input can be left open circuit. If it is desirable to capacitively couple the signal source to the clock then an external bias is required as shown in Fig. 6. The external bias voltage should be -1.3V at 25°C.
2. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 8.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. Input impedance is a function of frequency. See Fig. 5.
5. The TTL/CMOS O/P is a free collector, with an output rise/fall time which is a function of load resistance and load capacitance. The load capacitance should therefore be kept to a minimum and the load resistance should not be too small otherwise V_{OL} will be too great. eg TTL output current = 8mA V_{OL} = 0.5V. For CMOS outputs, the value of load resistor should be the maximum consistent with satisfactory rise times.
6. All components should be suitable for the frequency in use.

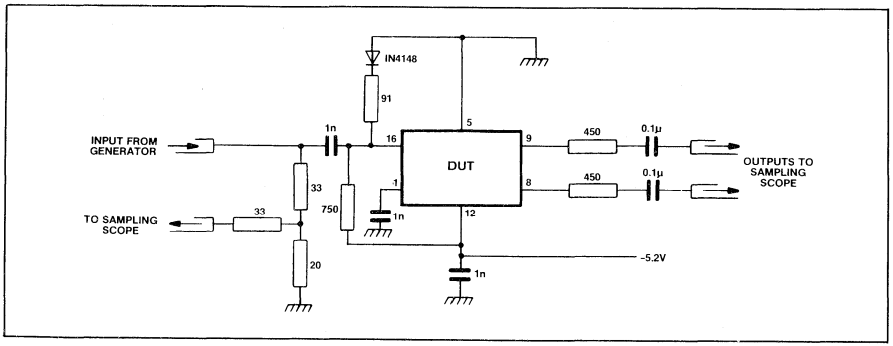


Fig.6 Test circuit

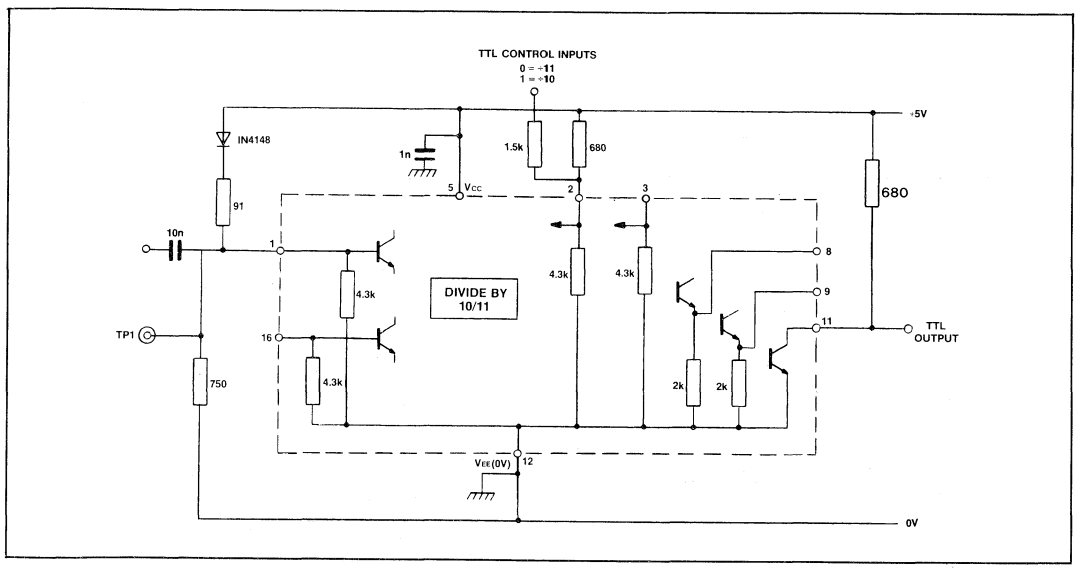


Fig.7 Typical application showing interfacing. NB Voltage at TP1 should be 3.7V at 25°

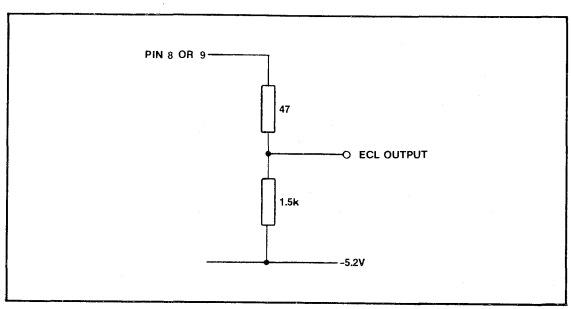


Fig.8 Interfacing to ECL 10K

SP8680A

550MHz ÷ 10/11

The SP8680 is an ECL counter with both ECL 10K and TTL compatible outputs. The circuit can operate from either ECL or TTL supplies. The division ratio is controlled by two control inputs (PE1 and PE2) which are ECL compatible. The counter will divide by 10 when either control input is in the high state and by 11 when both inputs are low. The counter can also be set to the eleventh state by applying a high level to the master set input.

FEATURES

- Very High Speed - 650MHz Typ.
- ECL and TTL Compatible Outputs
- DC or AC Clocking
- Clock Enable
- Divide By 10 or 11
- Asynchronous master set
- Equivalent to Fairchild 11C90

QUICK REFERENCE DATA

- Supply Voltage: 5V +0.5V -0.25V
  or -5V -0.5V +0.25V
- Power Consumption: 420mW
- Temperature: -55°C to +125°C

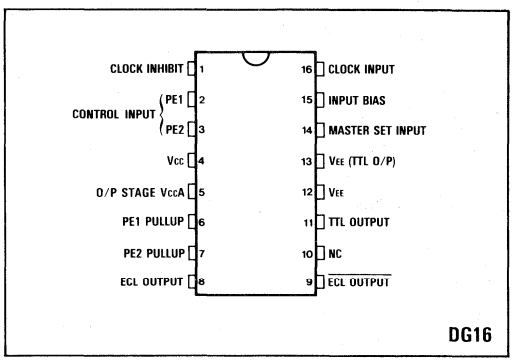


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP8680 A DG
SP8680 AB DG
SP8680 AC DG

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
ECL output source current	50mA
Storage temperature range	-55° C to +150° C
Max. junction temperature	+175° C
TTL output sink current	30mA
Max. clock I/P voltage	2.5V p-p

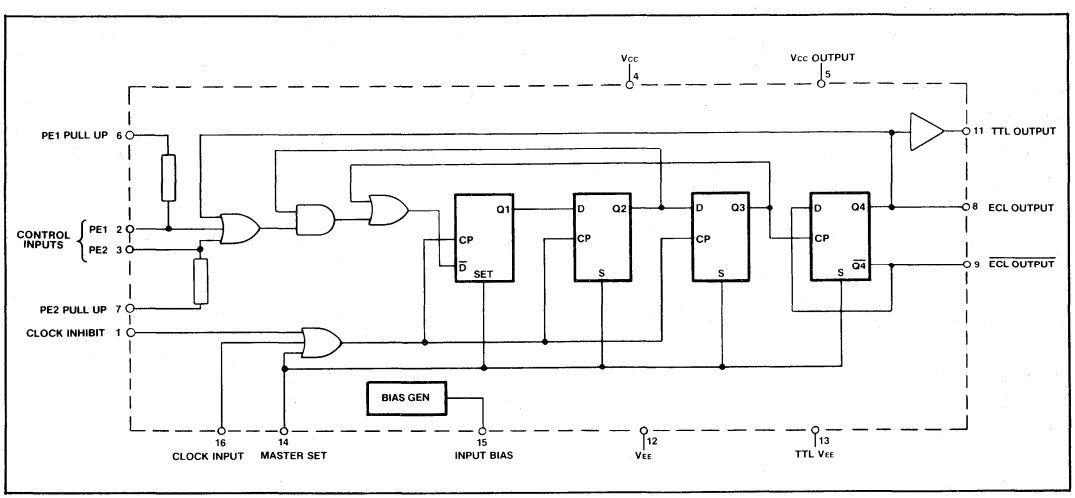


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS
TTL OPERATION

Supply voltage: V_{CC} = $V_{CC}A$ = 4.75 to 5.5V V_{EE} = 0V
Temperature: T_{amb} = -55°C to +125°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}		550	MHz	Clock input AC coupled = 350mV p-p	Note 4
Minimum frequency sinewave input	f_{min}	10		MHz	Clock input AC coupled = 600mV p-p	Note 5
Power supply current	I_{EE}		105	mA	V_{CC} = V_{CC} max. Pins 6,7,13 open circuit	Note 4
Power supply current including TTL stage	I_{EE}		111	mA	V_{CC} = V_{CC} max. Pins 6,7 open circuit	Note 4
TTL output high voltage	V_{OH}	2.3		V	V_{CC} = V_{CC} min. I_{OH} = -640μA	Note 4
TTL output low voltage	V_{OL}		0.5	V	V_{CC} = V_{CC} max. I_{OL} = -20mA	Note 4
Input high voltage PE1 and PE2 inputs	V_{INH}	3.9		V	V_{CC} = 5.0V (25°C)	
Input low voltage PE1 and PE2 inputs	V_{INL}		3.5	V	V_{CC} = 5.0V (25°C)	
Input low current PE1 and PE2 inputs	I_{IL}	-4		mA	V_{CC} = V_{CC} max. (25°C) Pins 6,7 = V_{CC} V_{IN} = 0.4V	
Propagation delay CP to Q TTL	t_{pHL} t_{pLH}	6	14	ns	V_{CC} = 5.0V (25°C)	Note 5
Propagation delay MS to Q TTL	t_p		17	ns	V_{CC} = 5.0V (25°C)	Note 5
Mode control set-up time	t_s	4		ns	V_{CC} = 5.0V (25°C)	Note 5
Mode control release time	t_r	4		ns	V_{CC} = 5.0V (25°C)	Note 5
TTL output rise time (20 % - 80 %)	t_{TLH}		5	ns	V_{CC} = 5.0V (25°C)	Note 5
TTL output fall time (80 % - 20 %)	t_{THL}		5	ns	V_{CC} = 5.0V (25°C)	Note 5

ELECTRICAL CHARACTERISTICS
ECL OPERATION

Supply Voltage: V_{EE} = -4.75V to -5.5V V_{CC} = 0V
Temperature: T_{amb} = -55°C to +125°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}		550	MHz	Clock input AC coupled = 350mV p-p	Note 4
Minimum frequency sinewave input	f_{min}	10		MHz	Clock input AC coupled = 600mV p-p	Note 5
Power supply current	I_{EE}		105	mA	V_{CC} = V_{CC} max. Pins 6,7,13 open circuit	Note 4
ECL output high voltage	V_{OH}	-0.93	-0.78	V	V_{EE} = -5.2V (25°C) Load = 100Ω to -2V	
ECL output low voltage	V_{OL}	-1.85	-1.62	V	V_{EE} = -5.2V (25°C) Load = 100Ω to -2V	
Input high voltage	V_{INH}	-1.095	-0.81	V	V_{EE} = -5.2V (25°C)	
Input low voltage	V_{INL}	-1.85	-1.475	V	V_{EE} = -5.2V (25°C)	
Input low currents	I_{IL}	0.5		μA	25°C	
Input high current						
Clock and MS	I_H		400	μA	V_{IN} = -1.85V (25°C)	
PE1 and PE2	I_H		250	μA	V_{IN} = -0.8V (25°C)	

ELECTRICAL CHARACTERISTICS - ECL OPERATION (CONT.)

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Propagation delay CP to Q4	t_{pHL}		4	ns	Load = 100Ω to -2V (25°C)	Note 5
	t_{pLH}		3	ns		
Propagation delay MS to Q4	t_{pLH}		6	ns	25°C	Note 5
Mode control set-up time	t_s	4		ns	25°C	Note 5
Mode control release time	t_r	4		ns	25°C	Note 5
ECL output rise time (20 % - 80 %)	t_{TLH}		2	ns	25°C	Note 5
ECL output fall time (80 % - 20 %)	t_{THL}		2	ns	25°C	Note 5

NOTES
1. Unless otherwise stated, the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.2mV/°C, V_{OL} = +0.24mV/°C and of V_{IN} = +0.8mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. Tested at 25°C and +125°C only.
5. Guaranteed but not tested.

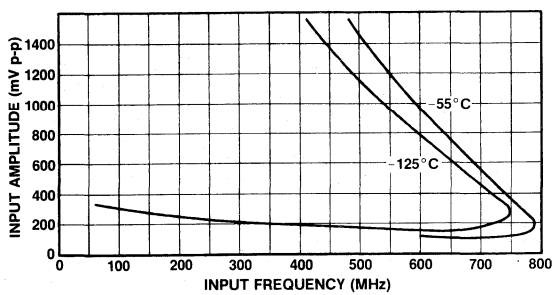
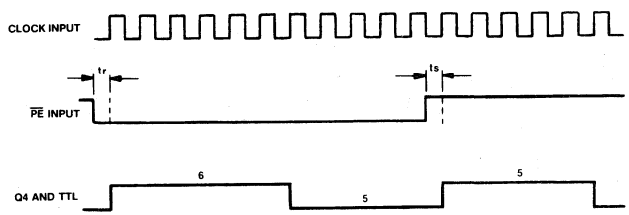


Fig.3 Typical input sensitivity SP8680



MS	CLOCK INH.	PE1	PE2	OUTPUT RESPONSE
H	X	X	X	ALL OUTPUTS SET HIGH
L	H	X	X	HOLD
L	L	L	L	÷11
L	L	H	L	÷10
L	L	L	H	÷10
L	L	H	H	÷10

X = DON'T CARE

Fig.4 Truth table and timing diagram SP8680

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

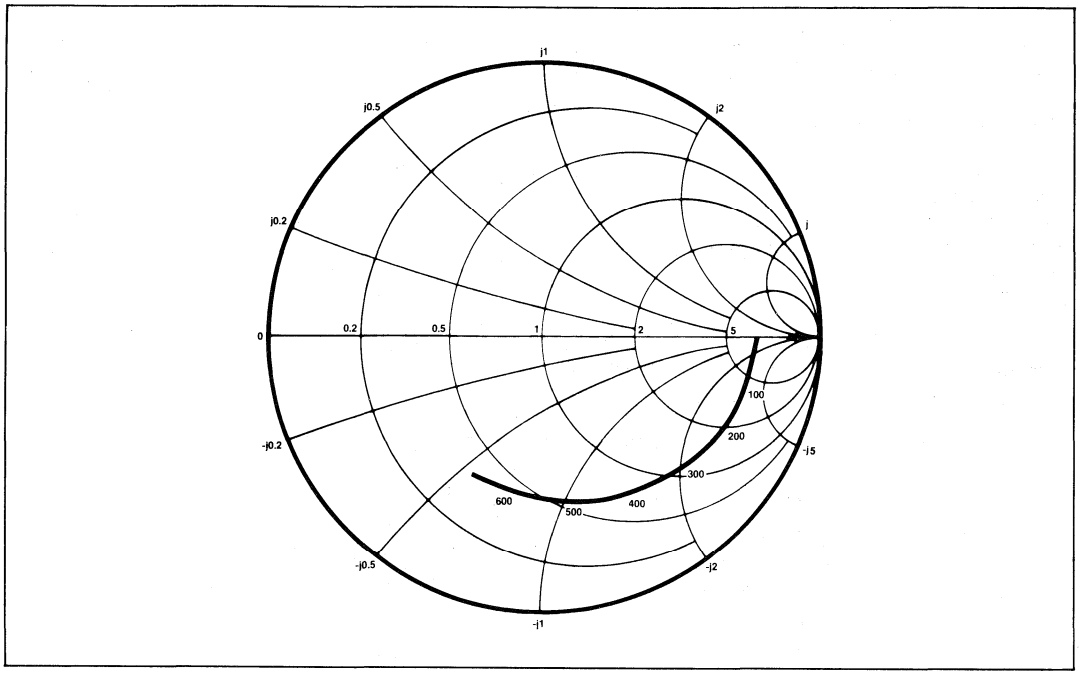


Fig.5 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

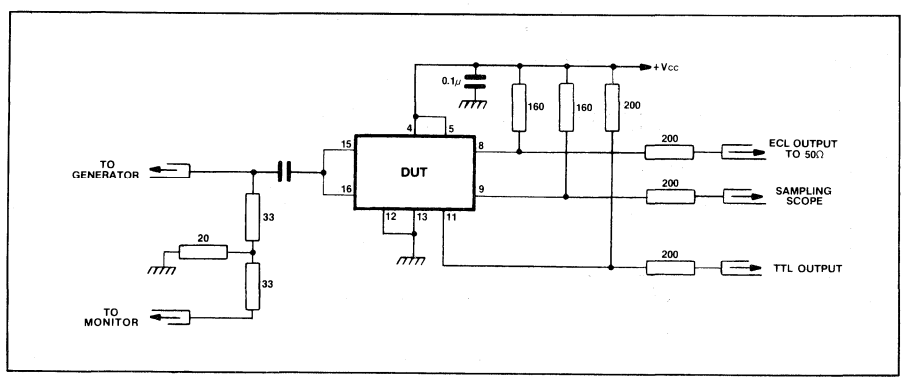


Fig.6 Test circuit

OPERATING NOTES

1. The clock input, which is ECL 10K compatible throughout the temperature range, can also be directly coupled to TTL as shown in Fig.9. The clock can also be capacitively coupled to the signal source (see Fig.7). Connecting the internally-generated bias voltage to the clock input, i.e. pin 15 to pin 16 centres the clock input about the switching threshold (see Fig.8).
2. The two complementary outputs are ECL 10K compatible but internal pulldown resistors are not included, and thus an external resistor to V_{EE} is required.
3. The TTL totem pole output operates with the same supply and is powered up by connecting V_{EE} (pin 12) to TTL V_{EE} (pin 13). If the TTL output is not required then the TTL V_{EE} (pin 13) should be left open-circuit reducing the power consumption by 20mW.
4. Both control inputs (PE1 and PE2) are ECL 10K compatible throughout the temperature range. Each control input is provided with a pull up resistor, the remote ends of which are connected to pins 6 and 7. This allows the pull up resistors to be unused if so desired, or to be used to interface from TTL (see Fig.9). If interfacing to ECL is required then pins 6 and 7 should be left open circuit: alternatively they can be connected to V_{EE} to act as pull-down resistors. When high, the master set input sets the counter to the eleventh state, is asynchronous, and overrides the clock input.
5. All the inputs have an internal pull-down resistor of 50k.
6. The device will operate down to DC but input slew rate must be better than 20V/μs.
7. Input impedance is a function of frequency. See Fig.5.

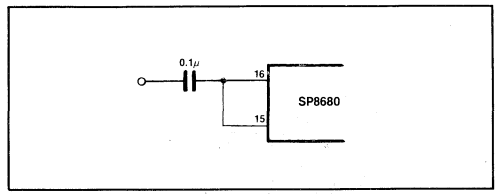


Fig.7 AC coupled input

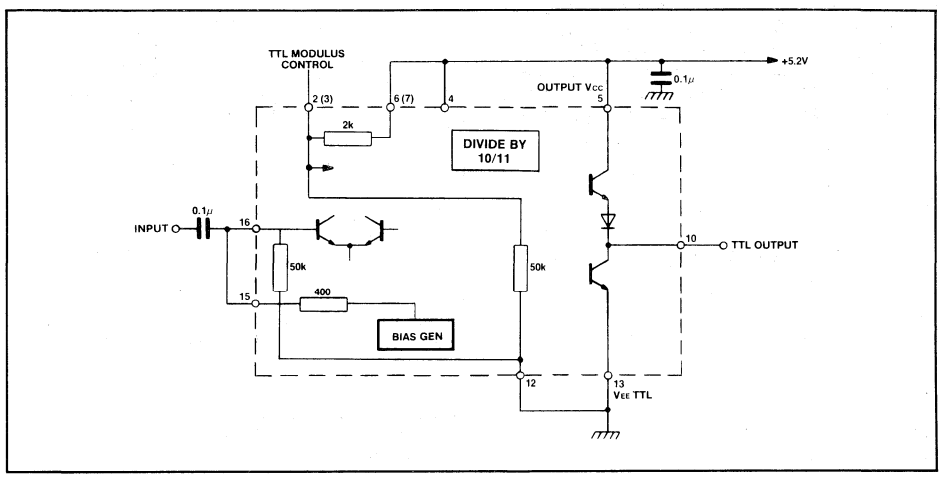


Fig.8 Typical application showing interfacing

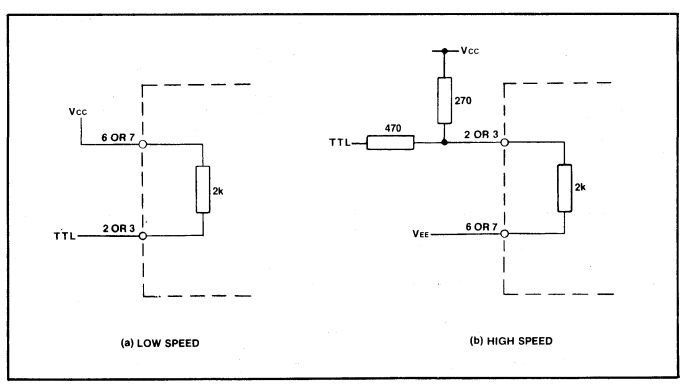


Fig.9 TTL interface to PE1 and PE2

SP8680B

575MHz ÷ 10/11

The SP8680 is an ECL counter with both ECL 10K and TTL compatible outputs. The circuit can operate from either ECL or TTL supplies. The division ratio is controlled by two control inputs (PE1 and PE2) which are ECL compatible. The counter will divide by 10 when either control input is in the high state and by 11 when both inputs are low. The counter can also be set to the eleventh state by applying a high level to the master set input.

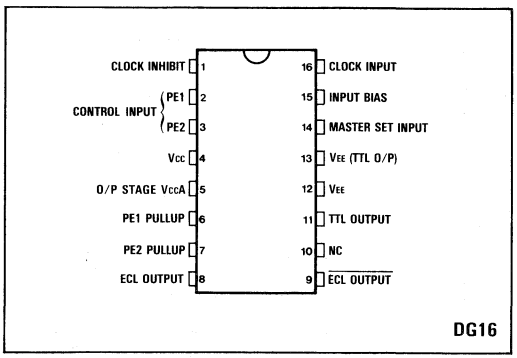


Fig.1 Pin connections - top view

FEATURES

- Very High Speed - 650MHz Typ.
- ECL and TTL Compatible Outputs
- DC or AC Clocking
- Clock Enable
- Divide By 10 or 11
- Asynchronous master set
- Equivalent to Fairchild 11C90

ORDERING INFORMATION

SP8680 B DG

QUICK REFERENCE DATA

- Supply Voltage: 5V +0.5V -0.25V
  or -5V -0.5V +0.25V
- Power Consumption: 420mW
- Temperature: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
ECL output source current	50mA
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
TTL output sink current	30mA
Max. clock I/P voltage	2.5V p-p

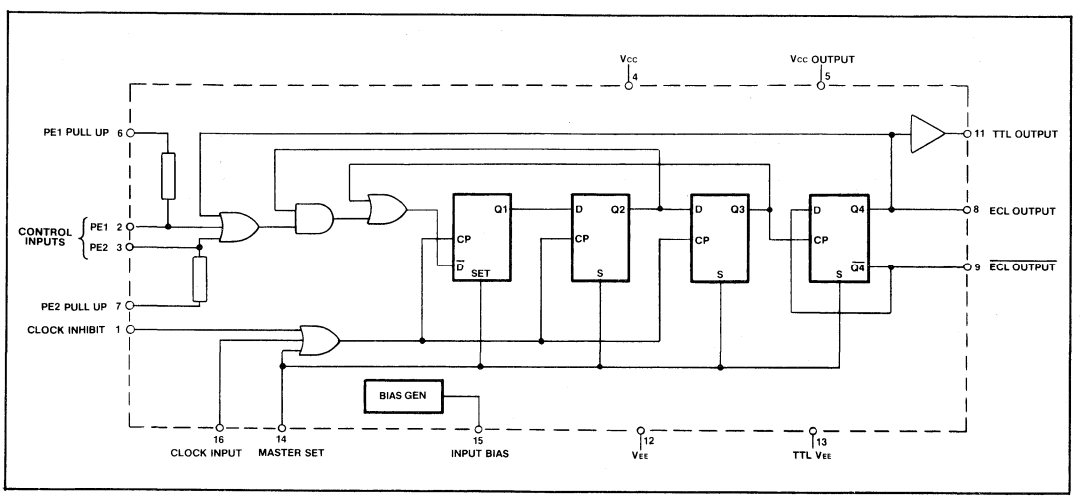


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS
TTL OPERATION

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C Supply voltage: V_{CC} = V_{CCA} = 4.75 to 5.5V V_{EE} = 0V

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}		575	MHz	Clock input AC coupled = 350mV p-p	
Minimum frequency sinewave input	f_{min}	10		MHz	Clock input AC coupled = 600mV p-p	Note 4
Power supply current	I_{EE}		105	mA	V_{CC} = V_{CC} max. Pins 6,7,13 open circuit	
Power supply current including TTL stage	I_{EE}		111	mA	V_{CC} = V_{CC} max. Pins 6,7 open circuit	
TTL output high voltage	V_{OH}	2.3		V	V_{CC} = V_{CC} min. I_{OH} = -640μA	
TTL output low voltage	V_{OL}		0.5	V	V_{CC} = V_{CC} max. I_{OL} = -20mA	
Input high voltage PE1 and PE2 inputs	V_{INH}	3.9		V	V_{CC} = 5.0V (25°C)	
Input low voltage PE1 and PE2 inputs	V_{INL}		3.5	V	V_{CC} = 5.0V (25°C)	
Input low current PE1 and PE2 inputs	I_{IL}	-4		mA	V_{CC} = V_{CC} max. (25°C) Pins 6,7 = V_{CC} V_{IN} = 0.4V	
Propagation delay CP to Q TTL	t_{pHL} t_{pLH}	6	14	ns	V_{CC} = 5.0V (25°C)	Note 4
Propagation delay MS to Q TTL	t_p		17	ns	V_{CC} = 5.0V (25°C)	Note 4
Mode control set-up time	t_s	4		ns	V_{CC} = 5.0V (25°C)	Note 4
Mode control release time	t_r	4		ns	V_{CC} = 5.0V (25°C)	Note 4
TTL output rise time (20 % - 80 %)	t_{TLH}		5	ns	V_{CC} = 5.0V (25°C)	Note 4
TTL output fall time (80 % - 20 %)	t_{THL}		5	ns	V_{CC} = 5.0V (25°C)	Note 4

ELECTRICAL CHARACTERISTICS
ECL OPERATION

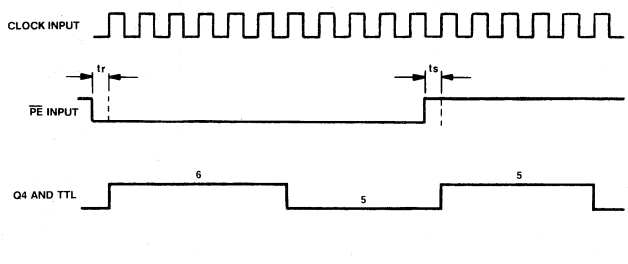
Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C Supply Voltage: V_{EE} = -4.75V to -5.5V V_{CC} = 0V

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}		575	MHz	Clock input AC coupled = 350mV p-p	
Minimum frequency sinewave input	f_{min}	10		MHz	Clock input AC coupled = 600mV p-p	Note 4
Power supply current	I_{EE}		105	mA	V_{CC} = V_{CC} max. Pins 6,7,13 open circuit	
ECL output high voltage	V_{OH}	-0.93	-0.78	V	V_{EE} = -5.2V (25°C) Load = 100Ω to -2V	
ECL output low voltage	V_{OL}	-1.85	-1.62	V	V_{EE} = -5.2V (25°C) Load = 100Ω to -2V	
Input high voltage	V_{INH}	-1.095	-0.81	V	V_{EE} = -5.2V (25°C)	
Input low voltage	V_{INL}	-1.85	-1.475	V	V_{EE} = -5.2V (25°C)	

ELECTRICAL CHARACTERISTICS - ECL OPERATION (CONT.)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Input low currents	I_{IL}	0.5		μA	25° C	
Input high current						
Clock and MS	I_H		400	μA	V_{IN} = -1.85V(25° C)	
PE1 and PE2	I_H		250	μA	V_{IN} = -0.8V(25° C)	
Propagation delay CP to Q4	t_{pLH}		3	ns	Load = 100Ω to -2V(25° C)	Note 4
Propagation delay MS to Q4	t_{pLH}		6	ns	25° C	Note 4
Mode control set-up time	t_s	4		ns	25° C	Note 4
Mode control release time	t_r	4		ns	25° C	Note 4
ECL output rise time (20 % - 80 %)	t_{TLH}		2	ns	25° C	Note 4
ECL output fall time (80 % - 20 %)	t_{THL}		2	ns	25° C	Note 4

NOTES
1. Unless otherwise stated, the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.2mV/°C, V_{OL} = +0.25mV/°C and of V_{IN} = +0.8mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5
4. Guaranteed but not tested.



MS	CLOCK INH.	PE1	PE2	OUTPUT RESPONSE
H	X	X	X	ALL OUTPUTS SET HIGH
L	H	X	X	HOLD
L	L	L	L	÷11
L	L	H	L	÷10
L	L	L	H	÷10
L	L	H	H	÷10

X = DON'T CARE

Fig.3 Truth table and timing diagram SP8680

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

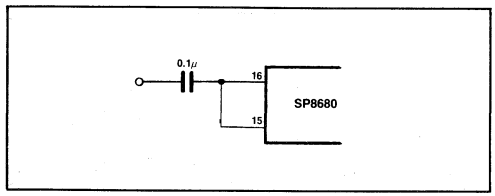


Fig.6 AC coupled input

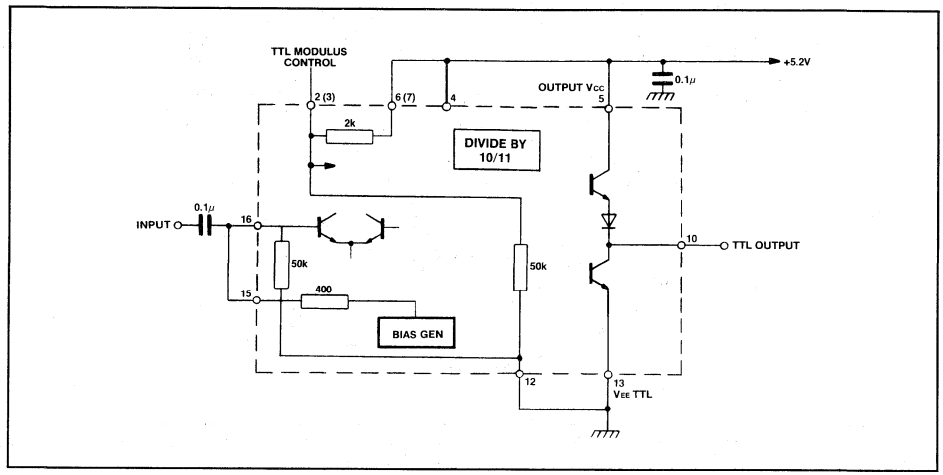


Fig.7 Typical application showing interfacing

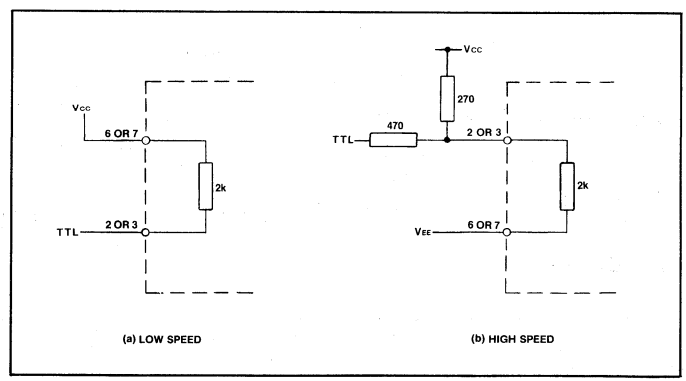


Fig.8 TTL interface to PE1 and PE2

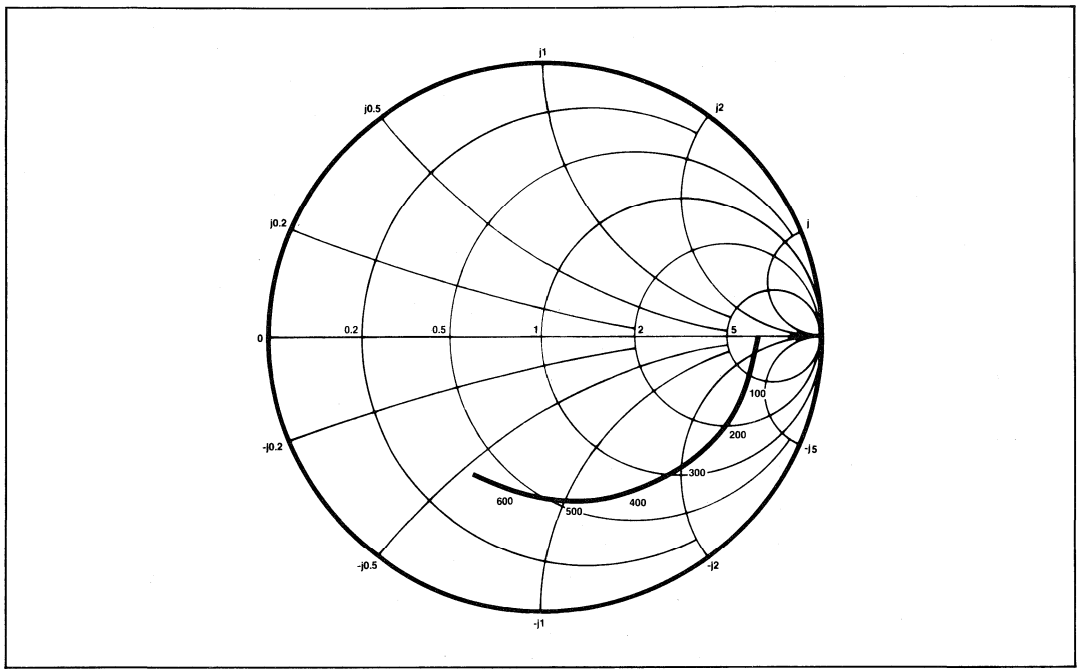


Fig.4 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

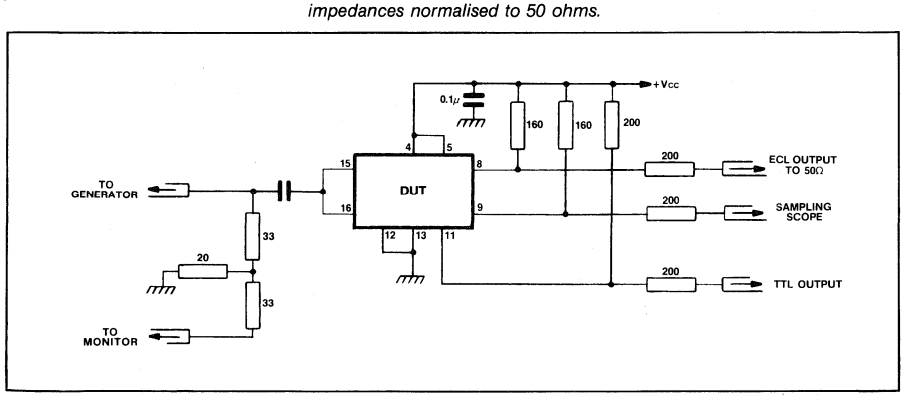


Fig.5 Test circuit

OPERATING NOTES

1. The clock input, which is ECL 10K compatible throughout the temperature range, can also be directly coupled to TTL as shown in Fig.8. The clock can also be capacitively coupled to the signal source (see Fig.6). Connecting the internally-generated bias voltage to the clock input, i.e. pin 15 to pin 16 centres the clock input about the switching threshold (see Fig.7).
2. The two complementary outputs are ECL 10K compatible but internal pulldown resistors are not included, and thus an external resistor to V_{EE} is required. The outputs are capable of driving a 50 ohm load to -2V over the temperature range -40°C to +85°C. The output high level will typically be reduced by 50mV.
3. The TTL totem pole output operates with the same supply and is powered up by connecting V_{EE} (pin 12) to TTL V_{EE} (pin 13). If the TTL output is not required then the TTL V_{EE} (pin 13) should be left open-circuit reducing the power consumption by 20mV.
4. Both control inputs (PE1 and PE2) are ECL 10K compatible throughout the temperature range. Each control input is provided with a pull up resistor, the remote ends of which are connected to pins 6 and 7. This allows the pull up resistors to be unused if so desired, or to be used to interface from TTL (see Fig.8). If interfacing to ECL is required then pins 6 and 7 should be left open circuit: alternatively they can be connected to V_{EE} to act as pull-down resistors. When high, the master set input sets the counter to the eleventh state, is asynchronous, and overrides the clock input.
5. All the inputs have an internal pull-down resistor of 50k.
6. The device will operate down to DC but input slew rate must be better than 20V/μs.
7. Input impedance is a function of frequency. See Fig.4.

SP8685

500MHz ÷ 10/11

The SP8685 is an ECL variable modulus divider, with ECL 10K compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

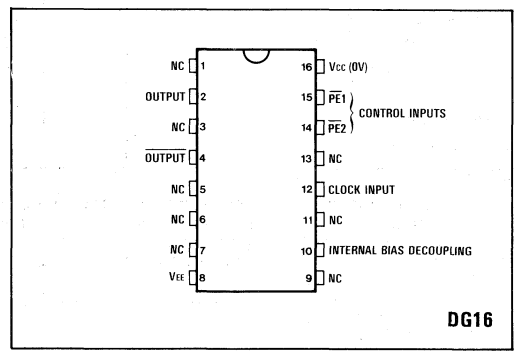


Fig.1 Pin connections - top view

FEATURES

- Divides by 10 and 11
- AC Coupled Input (Internal Bias)
- ECL Compatible Output

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 300mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8685 A DG
SP8685 B DG
SP8685 AB DG
SP8685 AC DG

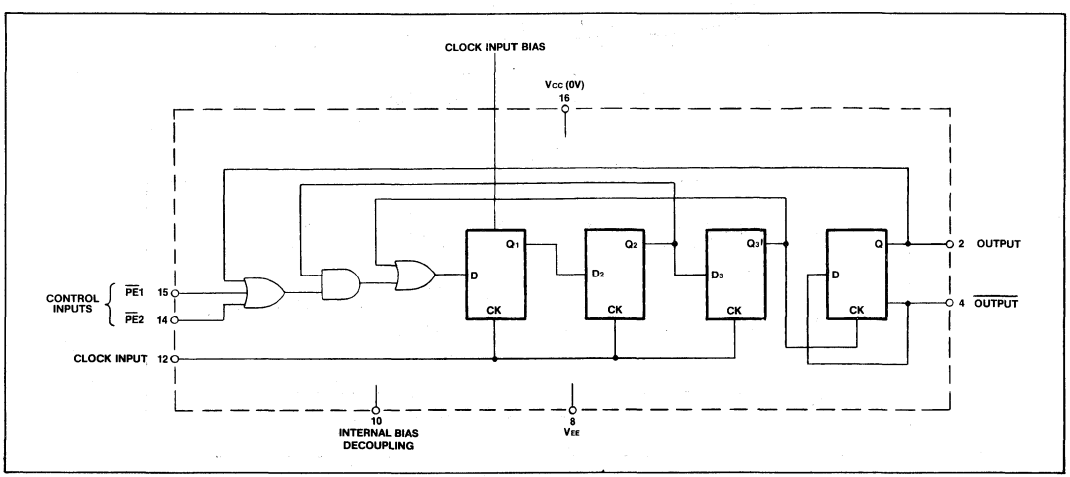


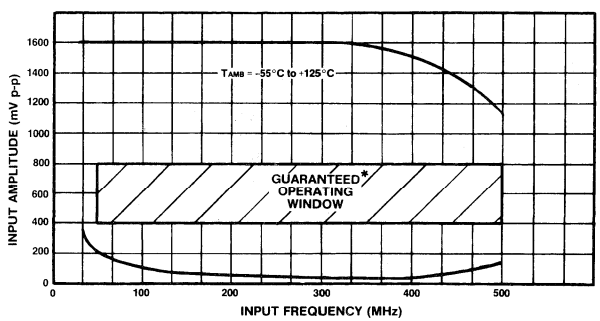
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	500		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 6
Power supply current	I_{EE}		70	mA	V_{EE} = -5.2V	Note 6
Output high voltage	V_{OH}	-0.87	-0.7	V	V_{EE} = -5.2V (25°C)	
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to output delay	t_p		6	ns		Note 7
Set-up time	t_s	2		ns		Note 7
Release time	t_r	2		ns		Note 7

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L ⟶ H transition of control input and the next L ⟶ H clock pulse transition to ensure that ÷10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H ⟶ L transition of the control input and the next L ⟶ H clock pulse transition to ensure that the ÷11 mode is obtained.
6. Tested at 25°C only.
7. Guaranteed but not tested.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic SP8685A

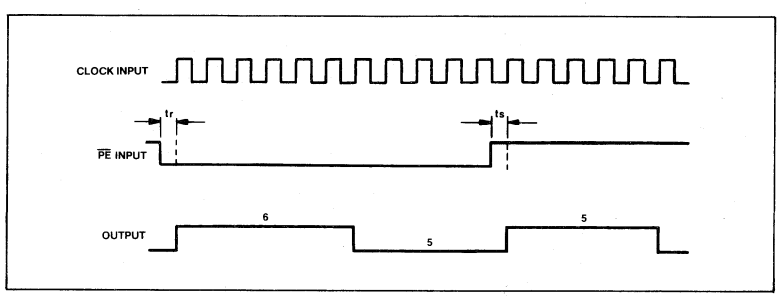


Fig.4 Timing diagram

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from clock input (Pin 12) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig.7.
5. The $\overline{PE}$ inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open.

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

6. Input impedance is a function of frequency. See Fig. 5.
7. All components should be suitable for the frequency in use.

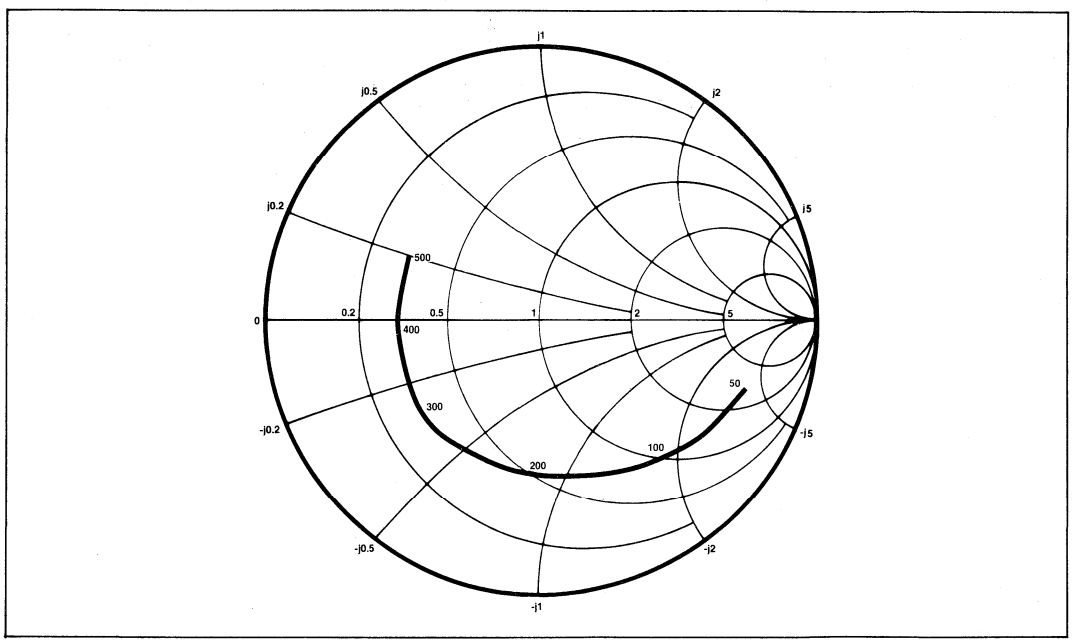


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

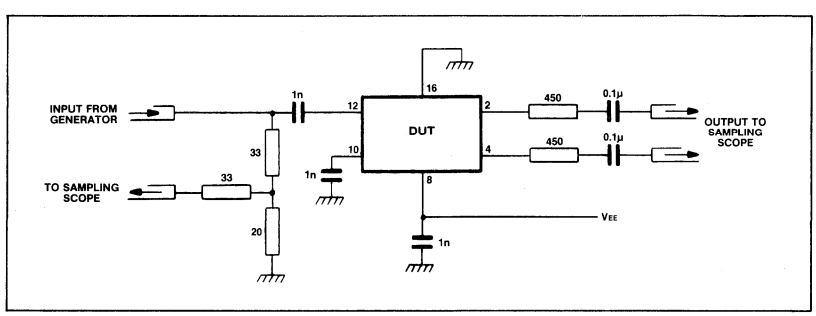


Fig.6 Test circuit

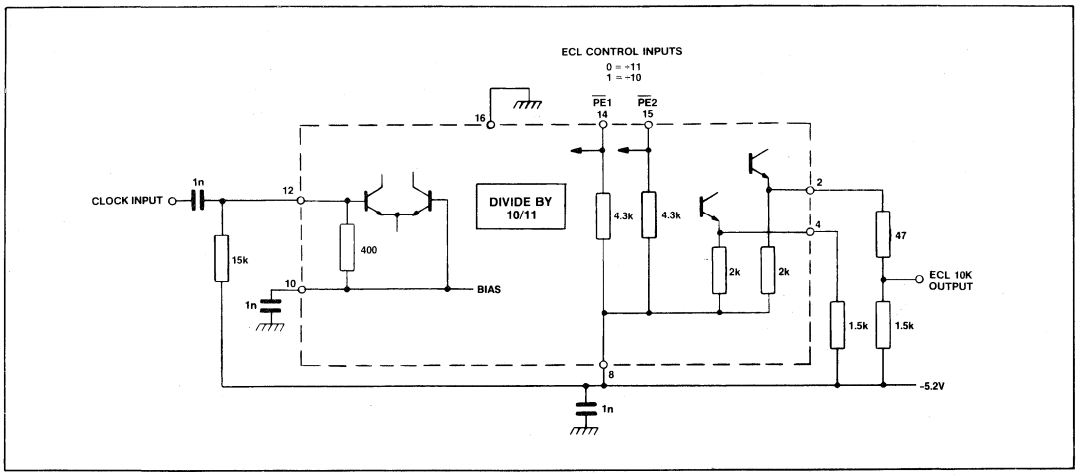


Fig.7 Typical application showing interfacing

SP8690 200MHz ÷ 10/11
SP8691 200MHz ÷ 8/9

The SP8690 and SP8691 are low power ECL counters with both ECL 10K and TTL compatible outputs. They divide by the lower division ratio when either control input is in the 'high' state and by the higher ratio when both are 'low' (or open circuit).

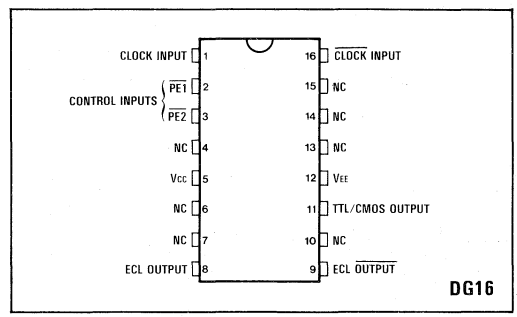


Fig.1 Pin connections - top view

FEATURES

- ECL and TTL/CMOS Output
- AC Coupled Input
- Control Inputs ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 70mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output ECL current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
TTL output	+12V
Input voltage	2.5V p-p
Max. open collector current	15mA

ORDERING INFORMATION

SP8690 A DG
SP8690 B DG
SP8690 AB DG
SP8690 AC DG
SP8691 A DG
SP8691 B DG
SP8691 AB DG
SP8691 AC DG

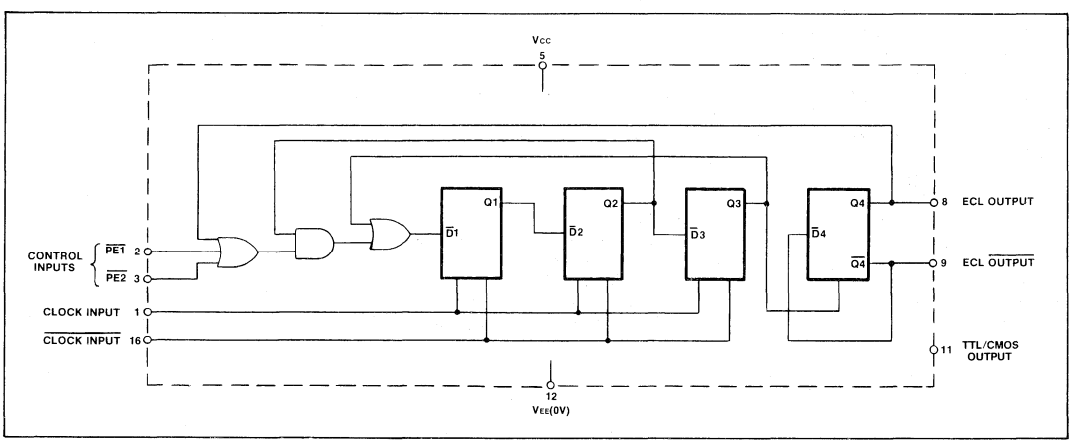


Fig.2 Functional diagram (SP8690)

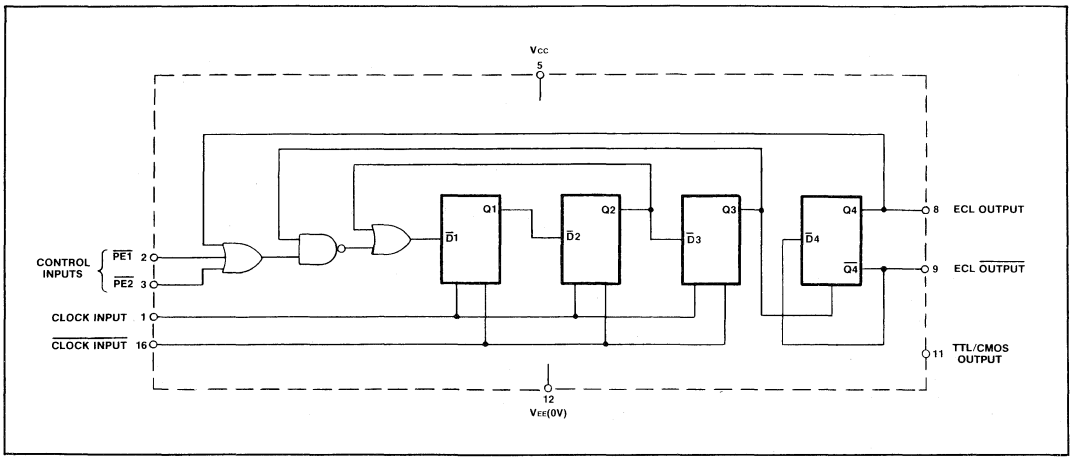


Fig.3 Functional diagram (SP8691)

ELECTRICAL CHARACTERISTICS

TTL OPERATION

Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input =400 - 800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input =400 - 800mV p-p	Note 3
Power supply current	I_{EE}		21	mA	V_{CC}= 5.0V	Note 3
TTL output high voltage	V_{OH}	3.75		V	V_{CC} = 5V RL = 560Ω	Note 3, 5
TTL output low voltage	V_{OL}		0.5	V	RL = 560Ω	Note 3, 5
Clock to TTL output delay (positive going)	t_{pLH}		32	ns	RL = 560Ω	Note 4
Clock to TTL output delay (negative going)	t_{pHL}		18	ns	RL = 560Ω	Note 4
Set-up time	t_s		3	ns		Note 4
Release time	t_r		8	ns		Note 4

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8690/1B tested at 25°C only.
4. Guaranteed but not tested.
5. Open collector output not recommended for use above 15MHz output frequency. $C_{load} \leqslant 5pF$.

ELECTRICAL CHARACTERISTICS

ECL OPERATION

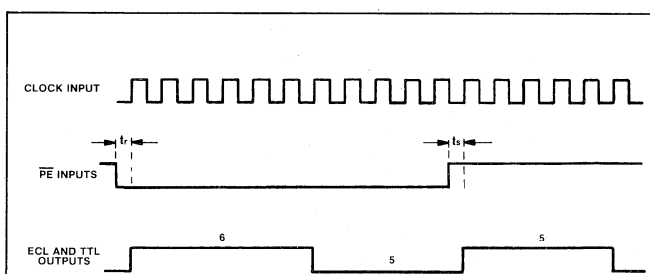
Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		21	mA	V_{EE} = -5.0V	Note 3

ELECTRICAL CHARACTERISTICS (CONTINUED)
ECL OPERATION

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V(25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V(25° C)	
PE input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V(25° C)	
PE input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V(25° C)	
Clock to ECL output delay	t_p		9	ns		Note 4
Set-up time	t_s	3		ns		Note 4
Release time	t_r	8		ns		Note 4

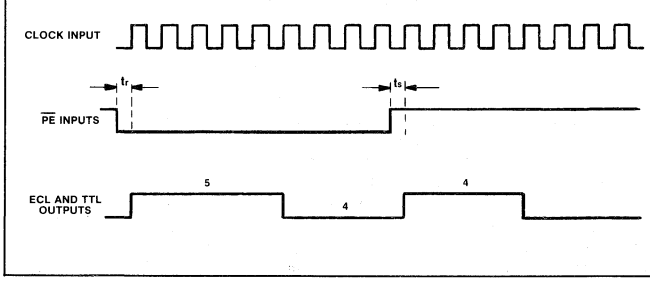
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8690/1B tested at 25°C only.
4. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig.4 Timing diagram SP8690

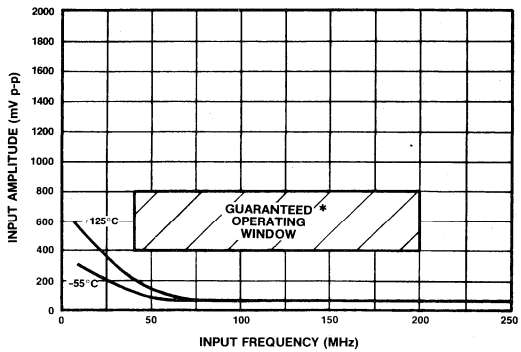


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	9
H	L	8
L	H	8
H	H	8

Fig.5 Timing diagram SP8691

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷10 or 8 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷11 or 9 mode is obtained.



*Tested as specified in table of Electrical Characteristics

Fig.6 Typical input characteristics SP86790/1

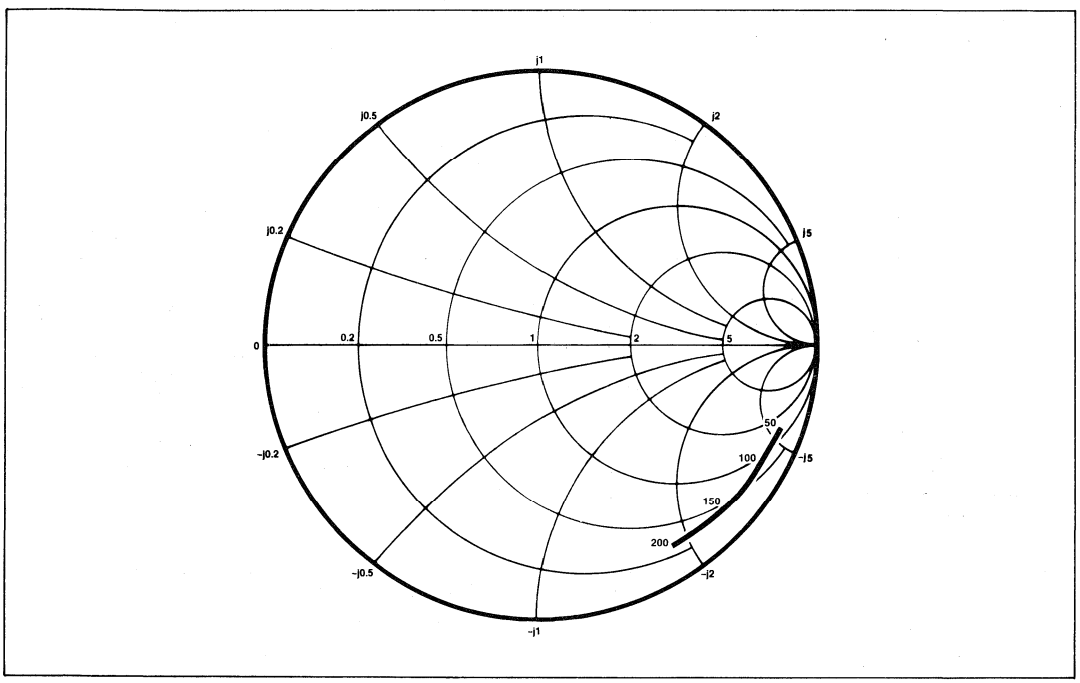


Fig.7 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs can be single or differentially driven. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 68k resistor from the input to V_{EE} (i.e. Pin 1 or 16 to Pin 12). This reduces input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The Q_4 and $\overline{Q_4}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig.9 .
5. The PE inputs are ECL III/10K compatible and include a 10k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8690/1 varies as a function of frequency. See Fig. 7.
7. The TTL/CMOS output has a free collector and the high state output voltage will depend on the supply that the collector load is taken too. This should not exceed 12V.
8. The rise/fall time of the open collector output waveform is directly proportional to load capacitance and load resistor value. Therefore load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 8| the output rise time is approximately 10ns and fall time is 7ns typically.

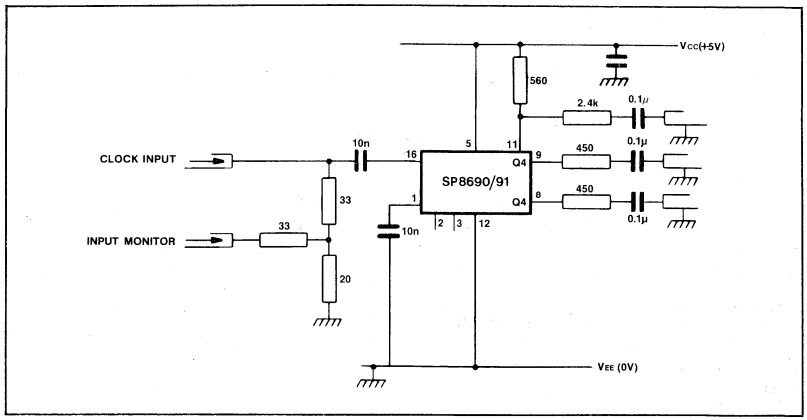


Fig.8 Test circuit for dynamic measurements

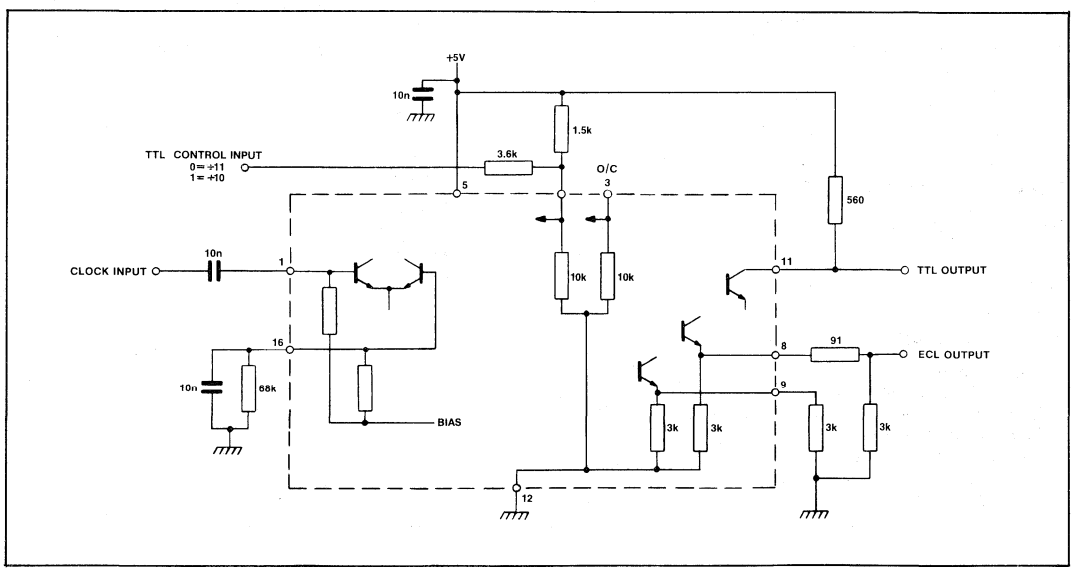


Fig.9 Typical applications circuit showing interfacing

SP8695

200MHz ÷ 10/11

The SP8695 is a low power ECL counter with both ECL 10K and TTL compatible outputs. They divide by 10 when either control input in the 'high' state and by 11 when both are 'low' (or open circuit). The inputs are ECL II compatible but can also be AC coupled. An open collector output is provided for interfacing to TTL or CMOS.

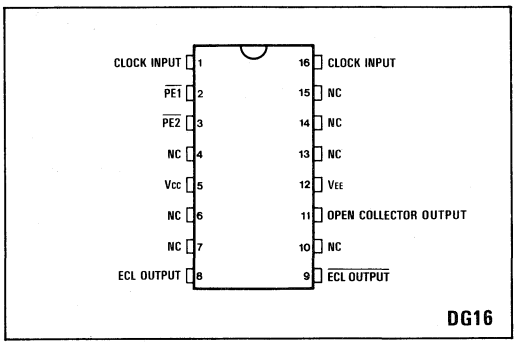


Fig.1 Pin connections - top view

FEATURES

- Low Frequency Operation
- ECL and TTL/CMOS Outputs
- DC or AC Coupled Input
- Temperature Ranges:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

QUICK REFERENCE DATA

- Supply Voltage: +5.0V
- Power Consumption: 80mW
- Maximum Input Frequency: 200MHz

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output ECL current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. input voltage	2.5V p-p
Max. open collector output voltage	+12V
Max. open collector current	15mA

ORDERING INFORMATION

SP8695 A DG
SP8695 B DG
SP8695 AB DG
SP8695 AC DG

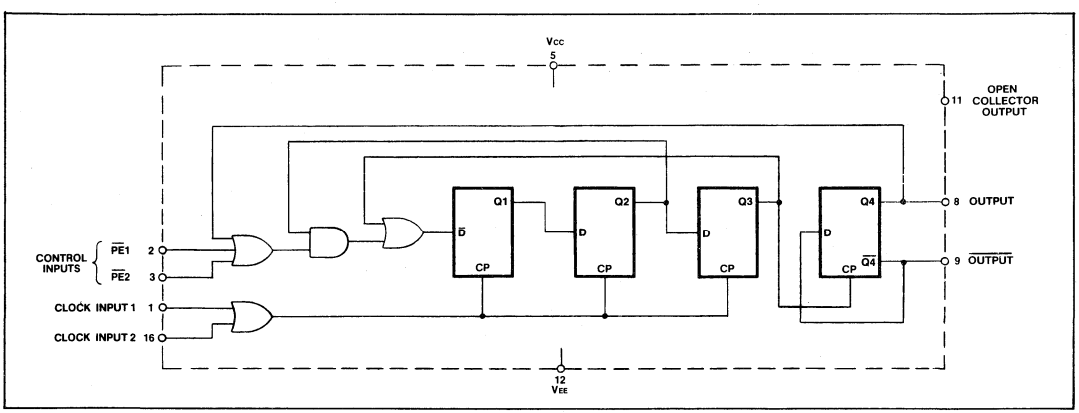


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

ECL OPERATION

Supply Voltage: V_{EE} = -5.2V ± 0.25V V_{CC} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade: T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Temperature
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		2	MHz	Input = 400-800mV	Note 4
Power supply current	I_{EE}		21	mA	V_{EE} = -5.0V	Note 3
ECL output low voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output high voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		9	ns		Note 4
Set-up time	t_s	3		ns		Note 4
Release time	t_r	8		ns		Note 4

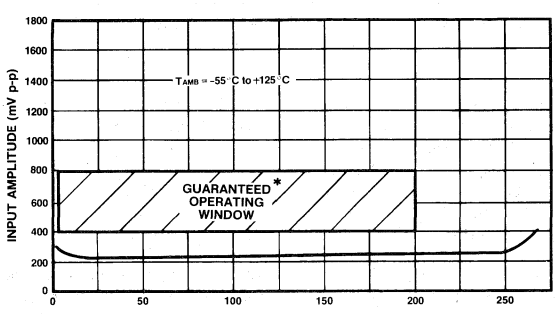
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8695B tested at 25°C only.
4. Guaranteed but not tested.
5. TTL output not recommended for use above 15MHz output frequency. $C_{load} \leq 5pF$.

ELECTRICAL CHARACTERISTICS

TTL OPERATION

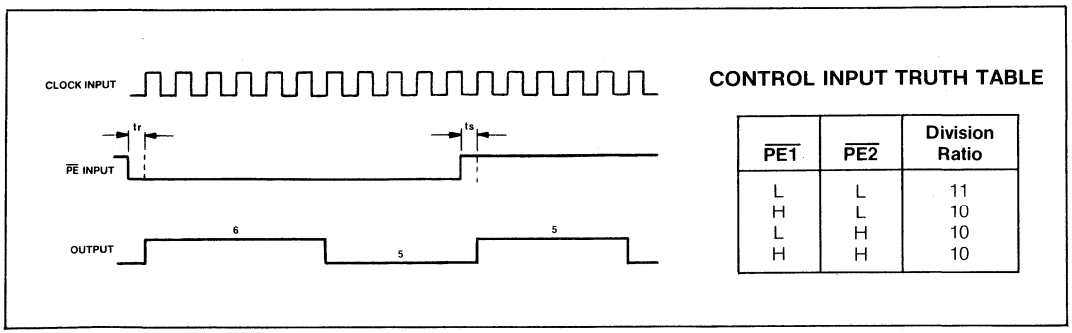
Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input =400 - 800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		2	MHz	Input =400 - 800mV p-p	Note 4
Power supply current	I_{EE}		21	mA	V_{CC}= 5.0V	Note 3
TTL output high voltage	V_{OH}	3.75		V	V_{CC}= 5V RL = 560Ω	Note 3, 5
TTL output low voltage	V_{OL}		0.5	V	RL = 560Ω	Note 3
Clock to TTL output delay (positive going)	t_{pLH}		32	ns	RL = 560Ω	Note 4
Clock to TTL output delay (negative going)	t_{pHL}		18	ns	RL = 560Ω	Note 4
Set-up time	t_s	3		ns		Note 4
Release time	t_r	8		ns		Note 4



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8695A



CONTROL INPUT TRUTH TABLE

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig.4 Timing diagram SP8695

NOTES

The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.

The release time t_r is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

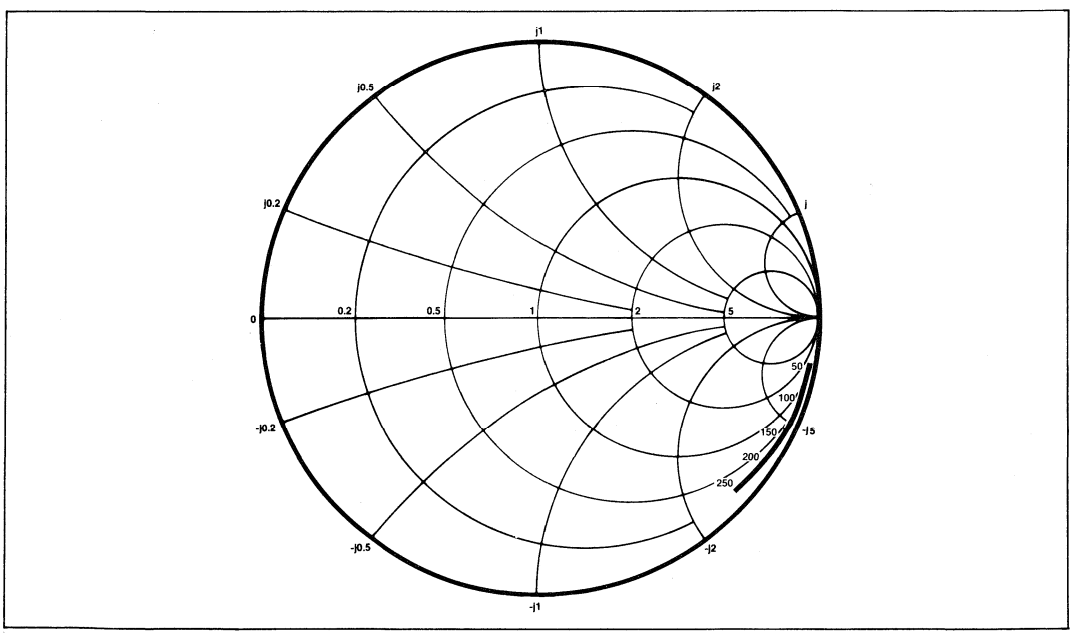


Fig.5 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 Ohms.

OPERATING NOTES

1. The clock inputs can be driven from ECL II, III and 10K. The input reference voltage (-3.8V at 25°C) is compatible with ECL II, III and 10K over the specified temperature range. The inputs can also be capacitively coupled by addition of external bias as shown in Fig. 6. Each input has an internal pull-down resistor of 10k, and unused inputs can therefore be left open circuit. They should by bypassed to RF where maximum noise immunity is required.
2. The PE control inputs are similarly ECL III/10K compatible and also have an internal 10k pull-down resistor, allowing unused inputs to be left open circuit if required.
3. The Q_4 and $\overline{Q}_4$ ECL outputs have internal circuitry equivalent to a 14k pull-down resistor on each output and are ECL II compatible: they can however be interfaced to ECL III/10K as shown in Fig. 8.
4. The circuit will operate down to DC but slew rate must be better than 5V/µs.
5. The input impedance of SP8695 varies as a function of frequency. See Fig. 5.
6. The TTL/CMOS output has a free collector and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed 12V. The rise and fall time of the open collector output waveform is directly proportional to load capacitance and load resistance value. Therefore load capacitance should be kept to a minimum and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 6 the output rise time is approximately 10ns and fall time is 7ns typically.

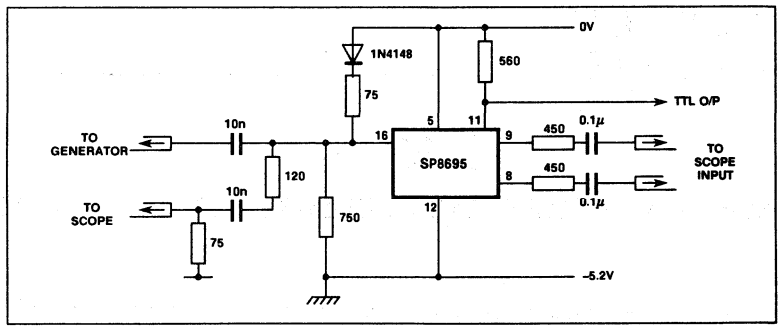


Fig. 6 Test circuit

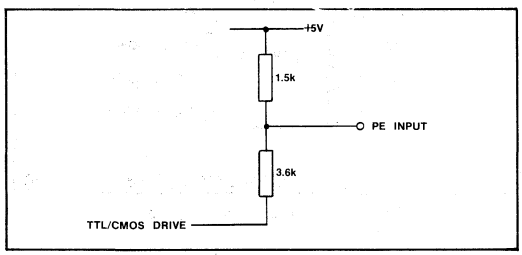


Fig.7 Interfacing TTL/CMOS to PE inputs

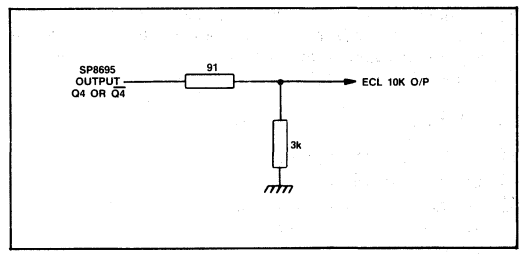


Fig.8 Interfacing to SP8695 output to ECL 10K

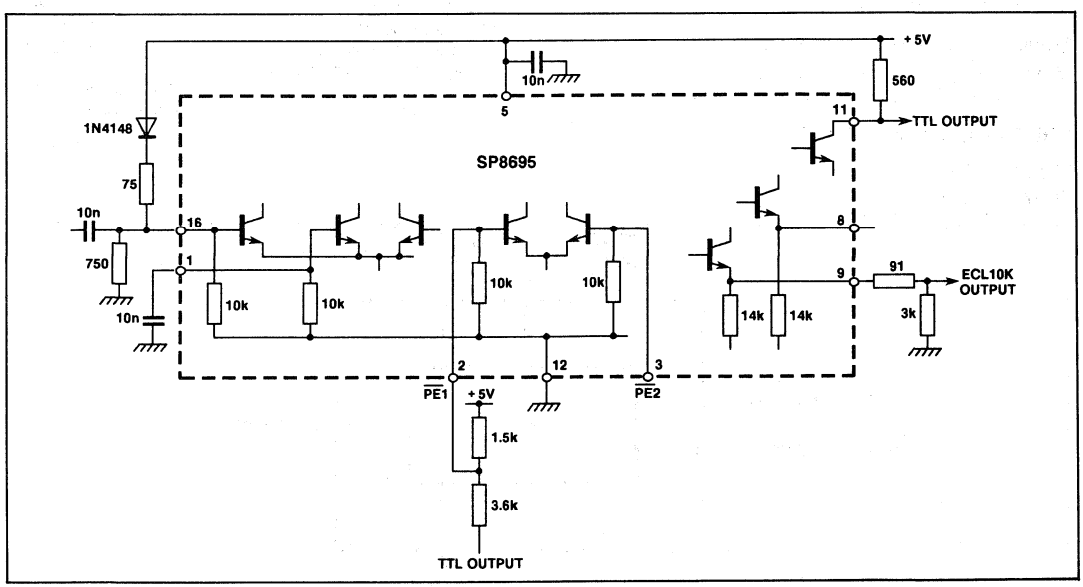


Fig.9 Typical application showing interfacing

SP8710

225MHz LOW POWER TWO MODULUS DIVIDER ÷ 100/101

The SP8710 is a Low Power Two Modulus Divider with a divide by 100 ratio when the modulus control input is high and 101 when the input is low. The device also features a power down mode and will operate with a 3V power supply.The 'A' Grade device is characterised over the full military temperature range of -55°C to +125°C, the 'B' Grade over the industrial range of -40°C to +85°C.

FEATURES

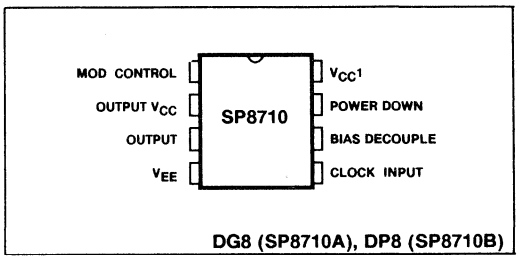
- Low Power High Speed
- Power Down Mode
- CMOS Compatible Output Capability
- Ideal for Decade Synthesisers
- 3V Supply Operation

QUICK REFERENCE DATA

- Supply Voltage Range 3V to 10V
- Full Military Temperature Range: -55°C to 125°C (SP8710A)

ORDERING INFORMATION

SP8710 A DG
SP8710 B DP



DG8 (SP8710A), DP8 (SP8710B)

Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	12V
Clock input level	2.5V p-p
Junction temperature	+175°C
Storage temperature range	
SP8710A	-55°C to +150°C
SP8710B	-55°C to +125°C

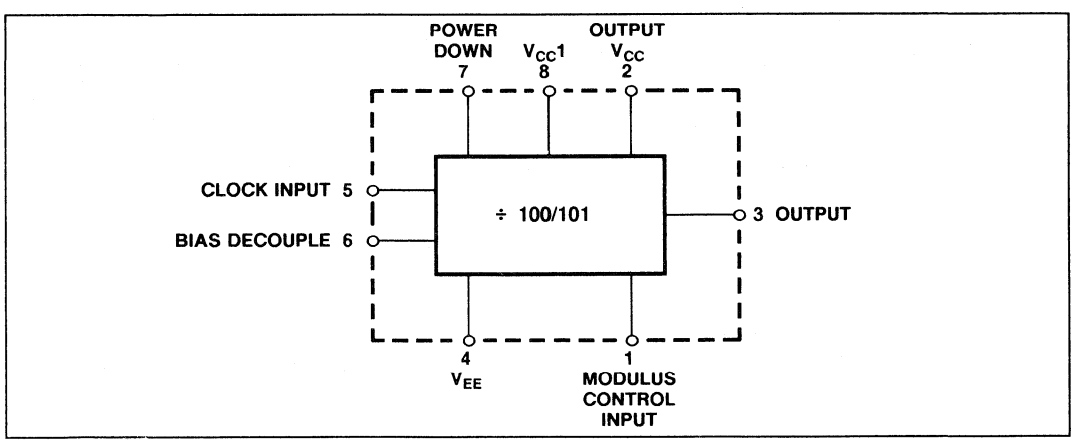


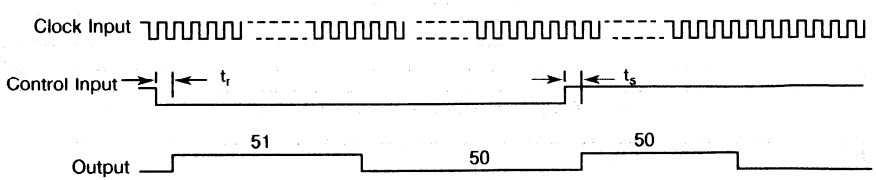
Fig.1 SP8710 functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = SP8710A -55°C to +125°C, SP8710B -40°C to +85°C, V_{CC} = +3V to +10V

Characteristic	Pin	Value		Units	Conditions
		Min.	Max.		
Max. sinewave input frequency	5	225		MHz	Input = 200mV - 1200mV p-p
Min. sinewave input frequency	5		20	MHz	Input = 400mV - 1200mV p-p
Min. slew rate for LF operation	5		100	V/µs	
Power supply current I_{EE}	8		8	mA	Power up V_{CC} = 5V
			8.5	mA	Power up V_{CC} = 10V
			1	mA	Power down
Output low voltage	3	0	0.5	V	Load = 10pF//100k
Output high voltage		V_{CC}-0.9	V_{CC}	V	Load = 10pF//100k, V_{CC} = 5V
		V_{CC}-0.95	V_{CC}	V	Load = 10pF//100k,V_{CC} = 10V
Modulus control input high voltage	1	0.6V_{CC}	V_{CC}	V	
Modulus control input low voltage	1	0	0.4V_{CC}	V	
Modulus control input high current	1		20	µA	Input = V_{CC}
Modulus control input low current	1		-10	µA	Input = 0V
Clock to output propagation delay	5,6,3		80	ns	
Set up time	1,3		10	ns	
Release time	1,3		10	ns	
Power down input high voltage	7	0.6V_{CC}	V_{CC}	V	
Power down input low voltage	7	0	0.4V_{CC}	V	
Power down input high current	7		1	µA	
Power down input low current	7		-1	µA	



TRUTH TABLE FOR CONTROL INPUTS

Control inputs	Division ratio
0	101
1	100

Fig 2 Timing diagram SP8710

NOTE

The set up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L → H clock pulse transition to ensure that the :100 mode is selected.

The release time t_r. is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the 101 mode is selected.

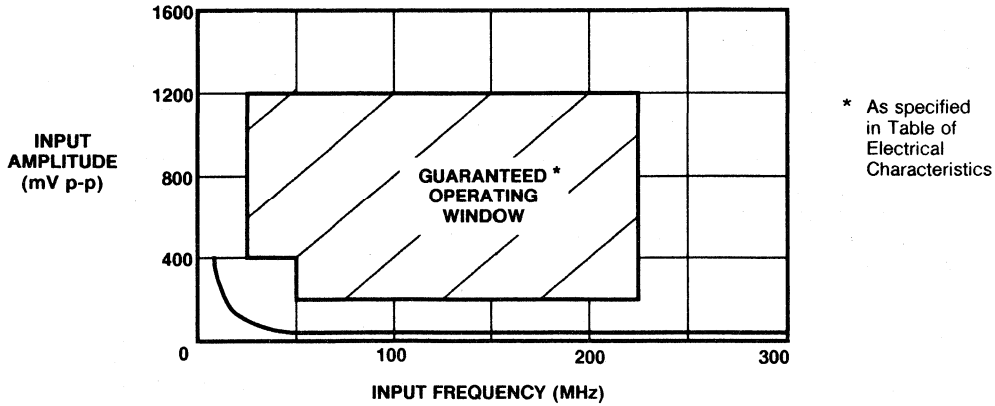


Fig.3 Typical input characteristics SP8710

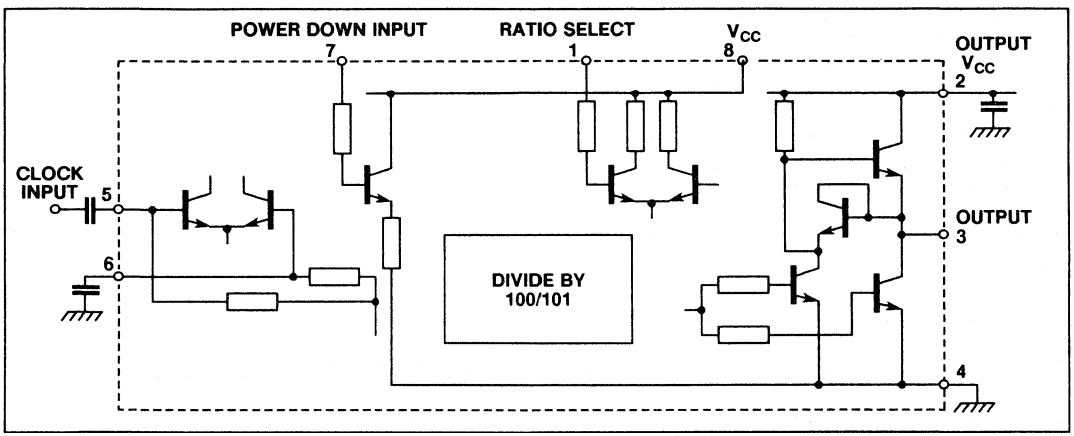


Fig.4 Typical application showing interfacing

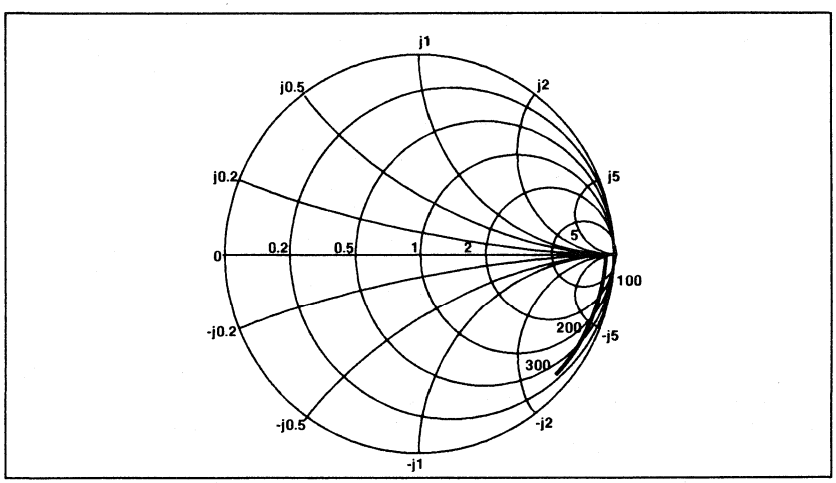


Fig.5 Typical Input Impedance. Test conditions:supply voltage 5V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 Ohms

SP8716/8/9

520MHz ULTRA LOW CURRENT TWO MODULUS DIVIDERS

The SP8716A ÷ 40/41, SP8718A ÷ 64/65 and SP8719A ÷80/81 are 50mW programmable dividers with a maximum specified operating frequency of 520MHz over the temperature range -55°C to +125°C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the maximum loop delay.

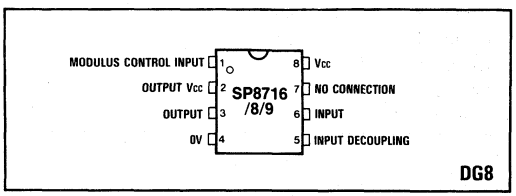


Fig.1 Pin connections - top view

FEATURES

- DC to 520MHz Operation
- -55°C to +125°C Temperature Range
- Control Inputs and Outputs are CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.2V ± 0.25V
- Supply Current 10.5mA typ.

ABSOLUTE MAXIMUM RATING

Supply voltage (pin 2 or 8):	8V
Storage temperature range:	-55°C to +150°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p

ORDERING INFORMATION

SP8716 A DG
SP8716 AB DG
SP8716 AC DG
SP8718 A DG
SP8718 AB DG
SP8718 AC DG
SP8719 A DG
SP8719 AB DG
SP8719 AC DG

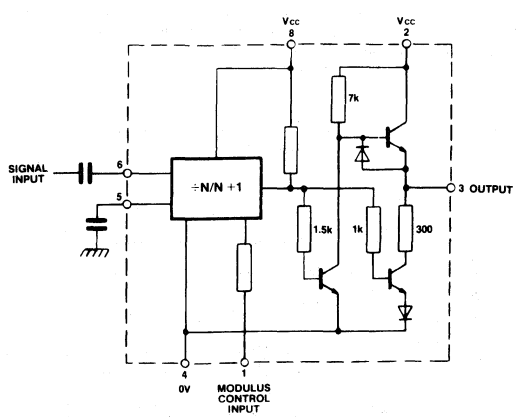


Fig.2 Functional diagram

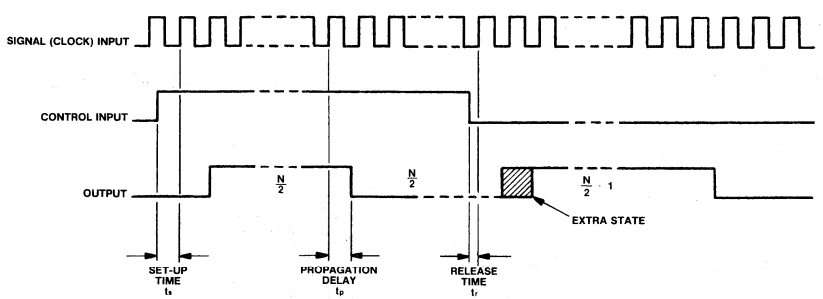
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage: V_{CC} = +4.95 to 5.45V, Temperature: T_{amb} = -55°C to +125°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Max. frequency	f_{max}	520		MHz	Input 125-350mV p-p	1
Min. frequency (sinewave input)	f_{min}		30	MHz	Input 400-800mV p-p	2
Power supply current	I_{CC}		11.9	mA	C_L = 3pF; pins 2, 8 linked	1
Output high voltage	V_{OH}	(V_{CC} -1.2)	1.2	V	I_L = -0.2mA	1
Output low voltage	V_{OL}		1	V	I_L = 0.2mA	1
Control input high voltage	V_{INH}	3.3	8	V	÷N	1
Control input low voltage	V_{INL}	0	1.7	V	÷N + 1	1
Control input high current	I_{INH}		0.41	mA	V_{INH} = 8V	1
Control input low current	I_{INL}	-0.20		mA	V_{INL} = 0V	1
Clock to output delay	t_p		28	ns	C_L = 10pF	2
Set-up time	t_s	10		ns	C_L = 10pF	2
Release time	t_r	10		ns	C_L = 10pF	2

NOTES
1. Tested at 25°C only.
2. Guaranteed but not tested.

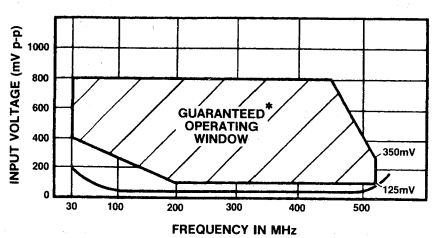


NOTE

The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷N mode is obtained.

The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷(N + 1) mode is obtained.

Fig.3 Timing diagram



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/µs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

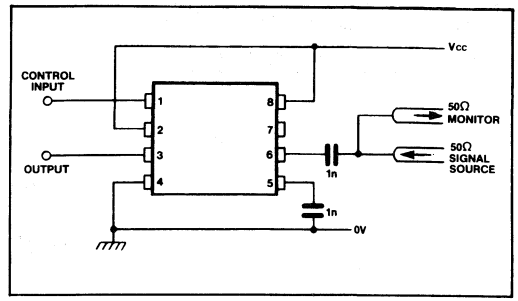


Fig.5 Toggle frequency test circuit

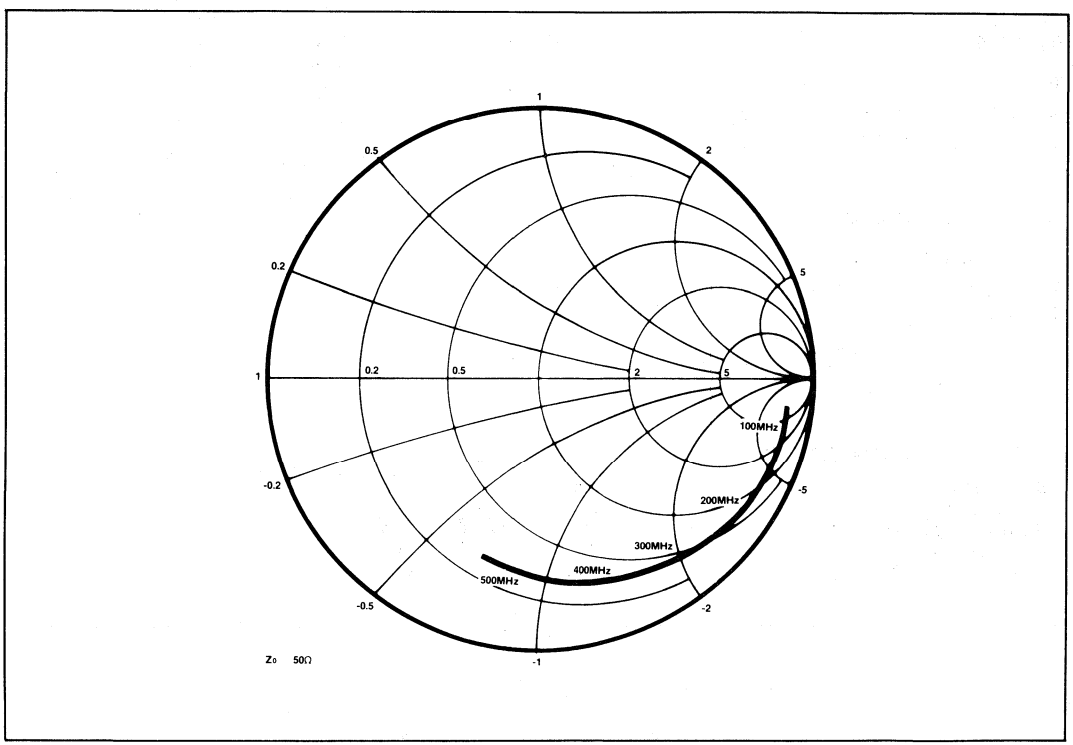


Fig.6 Typical input impedance

SP8720

300MHz ÷ 3/4

The SP8720 is an ECL counter with ECL 10K compatible outputs. It divides by 3 when either control input is in the high state and by 4 when both inputs are low (or open circuit). An AC coupled input of 600mV p-p is required.

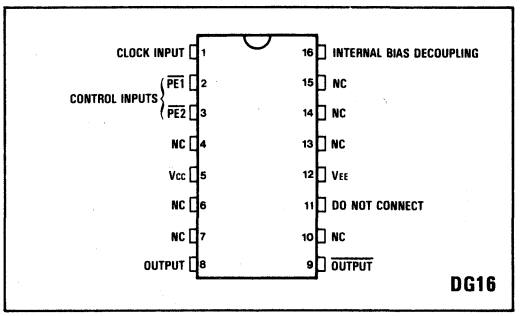


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Input (Internal Bias)
- Control Inputs ECL III/10K Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8720 A DG
SP8720 B DG
SP8720 AB DG
SP8720 AC DG

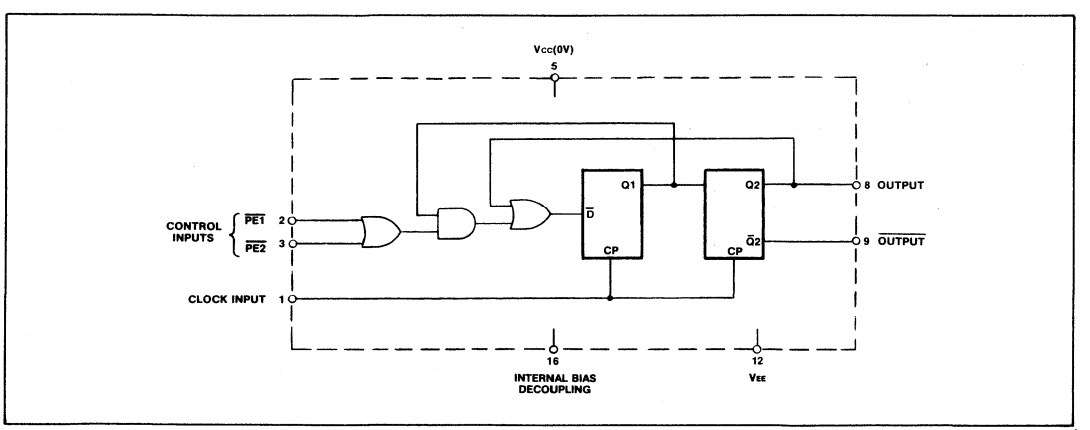


Fig.2 Functional diagram

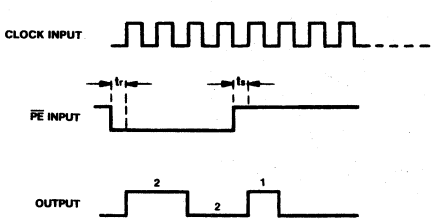
ELECTRICAL CHARACTERISTICS

ECL OPERATION

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	300		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	Note 3
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25° C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25° C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25° C)	
Clock to ECL output delay	t_p		6	ns		Note 4
Set-up time	t_s		2.5	ns		Note 4
Release time	t_r		3	ns		Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8720B tested at 25°C only.
4. Guaranteed but not tested.

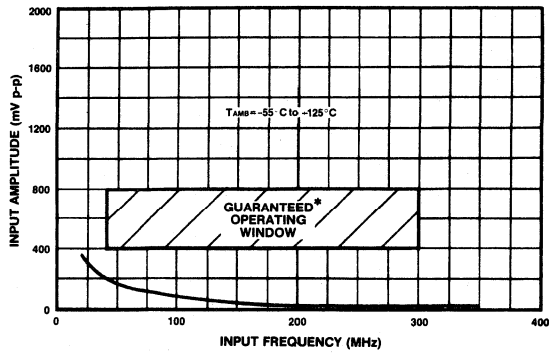


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	4
H	L	3
L	H	3
H	H	3

Fig.3 Timing diagram

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷3 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷4 mode is obtained.



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics SP8720A

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2k pulldown resistor at each output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8720 varies as a function of frequency. See Fig. 5.

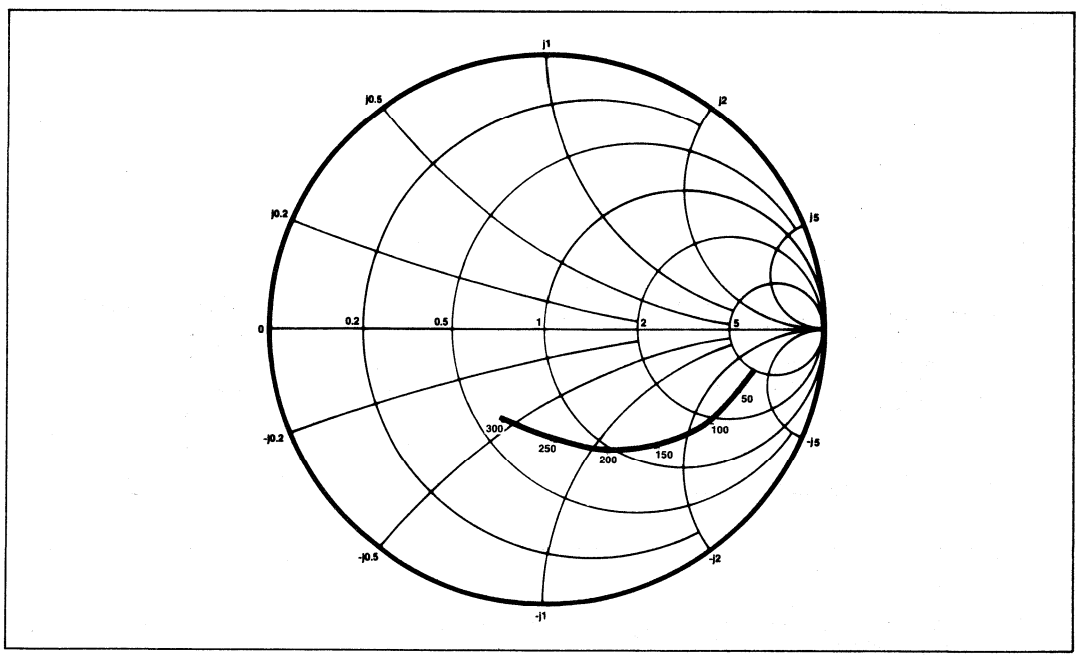


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

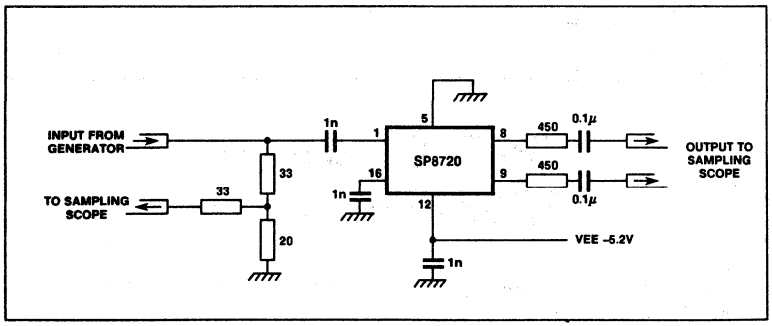


Fig. 6 Test circuit

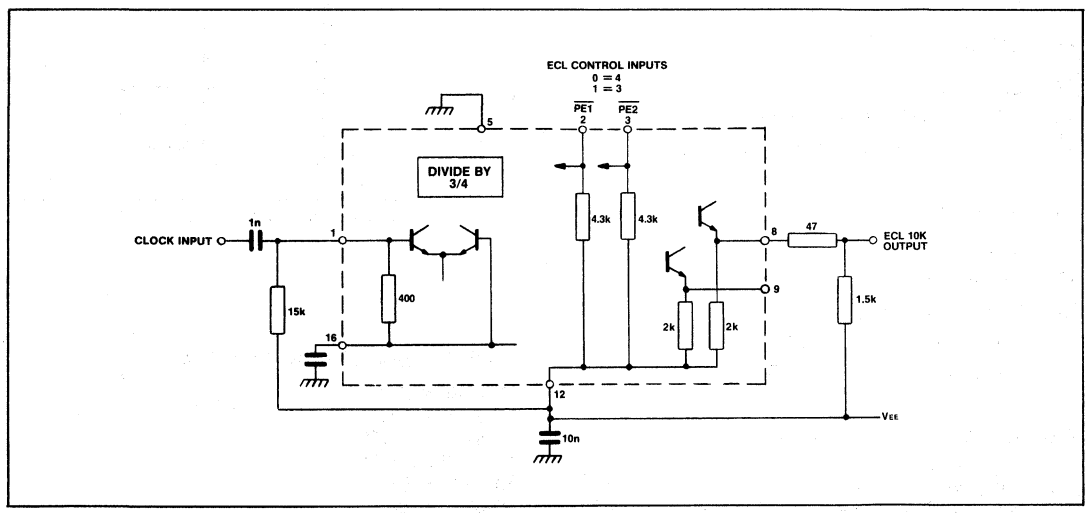


Fig.7 Typical applications circuit showing interfacing

SP8740 300MHz ÷ 5/6
SP8741 300MHz ÷ 6/7

The SP8740 and SP8741 are ECL counters with ECL 10K compatible output. The SP8740/SP8741 divide by 5 and 6 respectively when either control input is in the high state and by 6 and 7 respectively when both inputs are in the low state (or open circuit). An AC coupled input of 600mV is required.

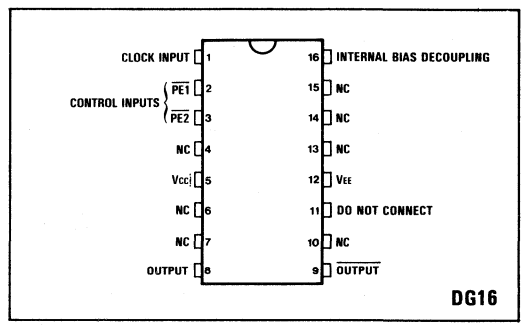


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- ECL Compatible Control Inputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8740 A DG
SP8740 B DG
SP8740 AB DG
SP8740 AC DG
SP8741 A DG
SP8741 B DG
SP8741 AB DG
SP8741 AC DG

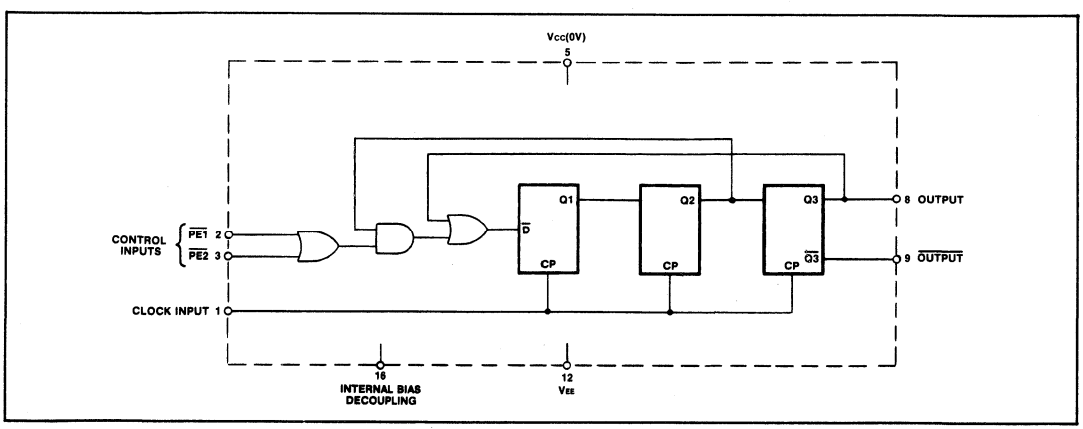


Fig.2 Functional diagram (SP8740)

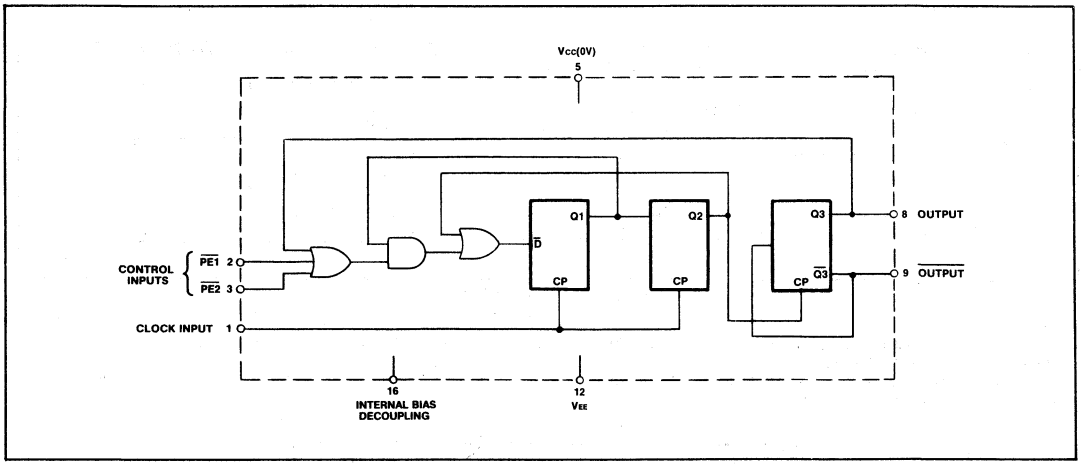


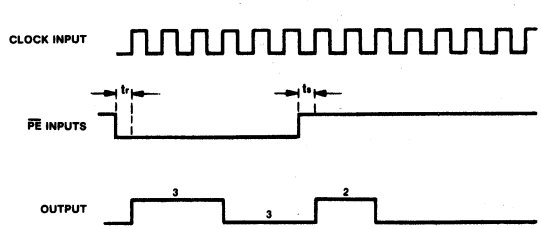
Fig.3 Functional diagram (SP8741)

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	300		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		60	mA		Note 3
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE}=-5.2V(25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE}=-5.2V(25°C)	
PE input high voltage	V_{INH}	-0.93		V	V_{EE}=-5.2V(25°C)	
PE input low voltage	V_{INL}		-1.62	V	V_{EE}=-5.2V(25°C)	
Clock to ECL output delay	t_p		6	ns		Note 4
Set-up time	t_s		2.5	ns		Note 4
Release time	t_r		3	ns		Note 4

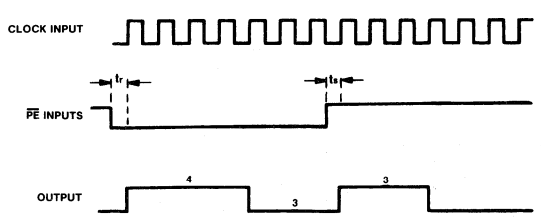
NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over the full specified supply, frequency and temperature range of both SP8740 and SP8741.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and V_{IN} = +1.22mV/°C but these are not tested.
3. SP8740/1B tested at 25°C only.
4. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	6
H	L	5
L	H	5
H	H	5

Fig.4 Timing diagram SP8740



TRUTH TABLE FOR CONTROL INPUTS

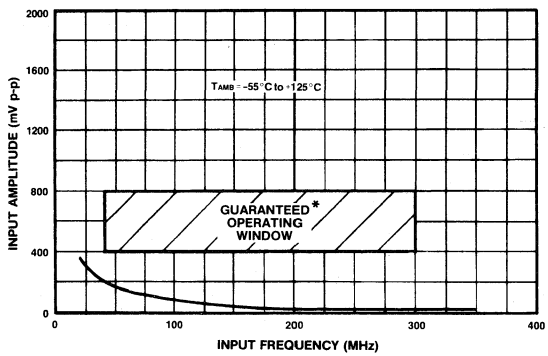
$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	7
H	L	6
L	H	6
H	H	6

Fig.5 Timing diagram SP8741

NOTE:

The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷5 or 6 mode is obtained.

The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷6 or 7 mode is obtained.



*Tested as specified in table of Electrical Characteristics

Fig.6 Typical input characteristics SP8740/1A

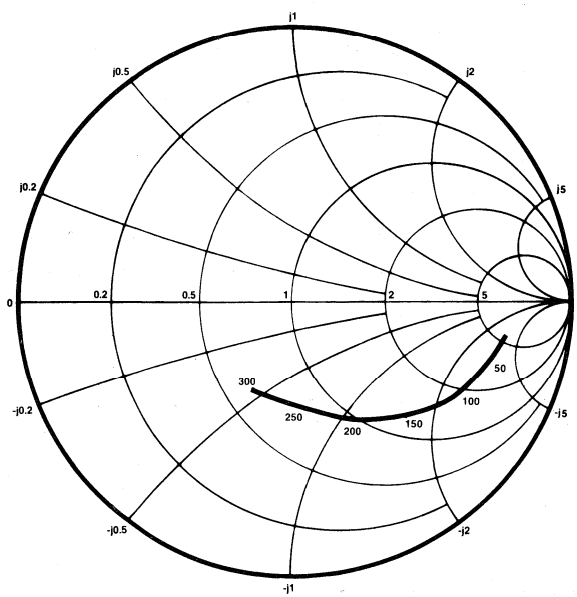


Fig.7 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/us.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 9. There is an internal circuit equivalent to a load of 2k pulldown resistor at load output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8740/1 varies as a function of frequency. See Fig. 7.
7. The SP8740 is not suitable for use in a fixed divide by 6 mode.

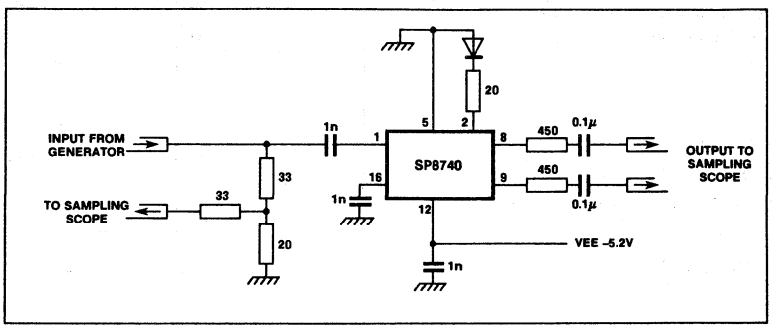


Fig. 8 Test circuit

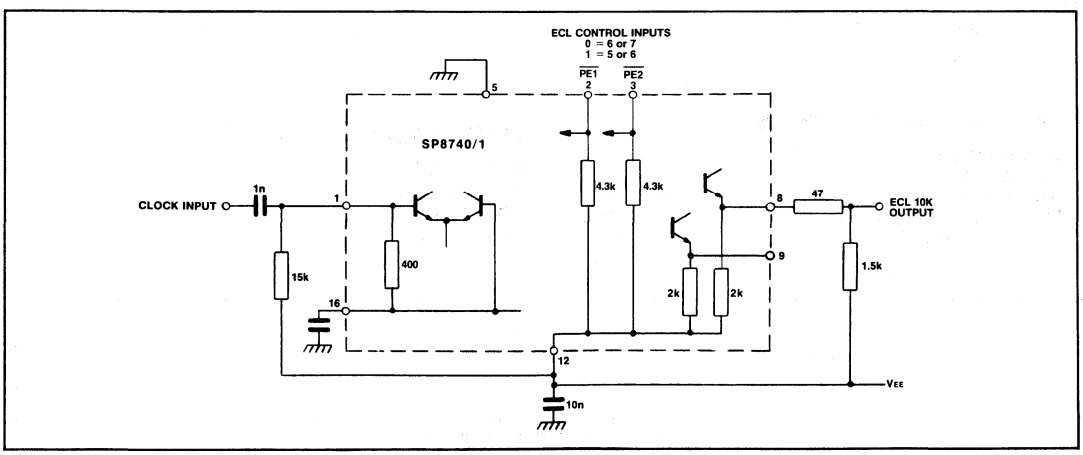


Fig.9 Typical applications circuit showing interfacing

SP8743A 450MHz ÷ 8/9
SP8743B 500MHz ÷ 8/9

The SP8743 is an ECL counter with ECL 10K compatible outputs. It divides by 8 when either control input is in the high state and by 9 when both inputs are low (or open circuit). An AC coupled input of 600mV p-p is required.

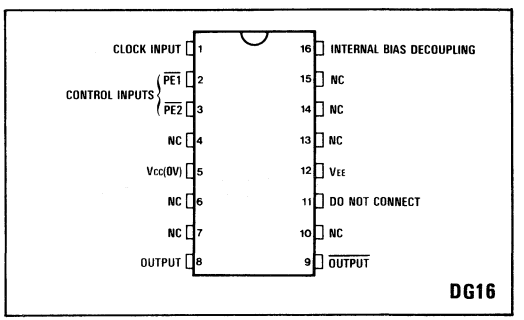


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- ECL Compatible Control Inputs
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8743 A DG
SP8743 B DG
SP8743 AB DG
SP8743 AC DG

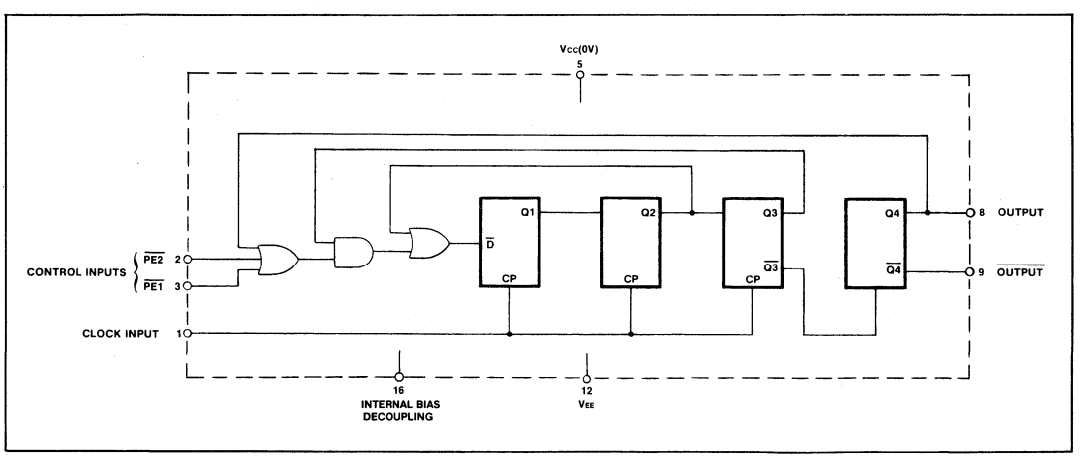


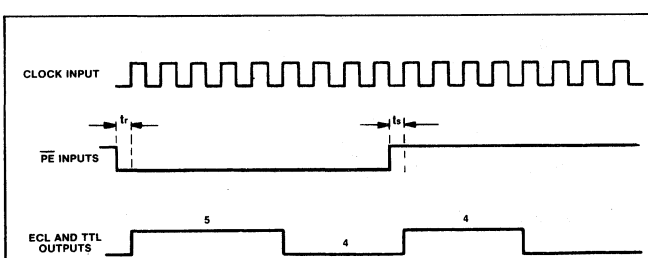
Fig.2 Function diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency	f_{max}	450		MHz	A	Input = 400 - 800mV p-p	Note 4
sinewave input		500		MHz	B	Input = 400 - 800mV p-p	Note 4
Minimum frequency	f_{min}		40	MHz	Both	Input = 400 - 800mV p-p	Note 5
sinewave input							
Power supply current	I_{EE}		60	mA	Both	V_{EE} = -5.2V	Note 6
ECL output high voltage	V_{OH}	-0.85	-0.7	V	Both	V_{EE} = -5.2V(25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	Both	V_{EE} = -5.2V(25° C)	
PE input high voltage	V_{INH}	-0.93		V	Both	V_{EE} = -5.2V(25° C)	
PE input low voltage	V_{INL}		-1.62	V	Both	V_{EE} = -5.2V(25° C)	
Clock to ECL output delay	t_p		6	ns	Both		Note 5
Set-up time	t_s	1		ns	Both		Note 5
Release time	t_r	2.5		ns	Both		Note 5

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C.
3. The test configuration for dynamic testing is shown in Fig.6.
4. Tested at low and high temperature only (not at 25°C)
5. Guaranteed but not tested.
6. Tested at 25°C only.

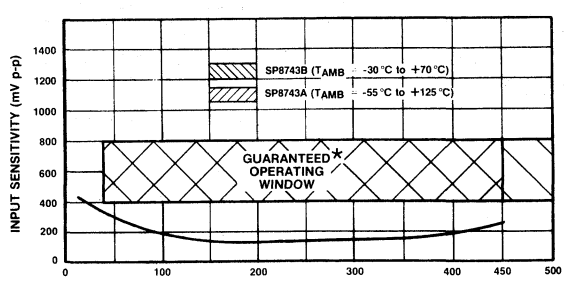


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	9
H	L	8
L	H	8
H	H	8

Fig.3 Timing diagram

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷8 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷9 mode is obtained.



* Tested as specified in Table of Electrical Characteristics

Fig.4 Typical input characteristics of SP8743

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2k pulldown resistor at each output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8743 varies as a function of frequency. See Fig. 5.

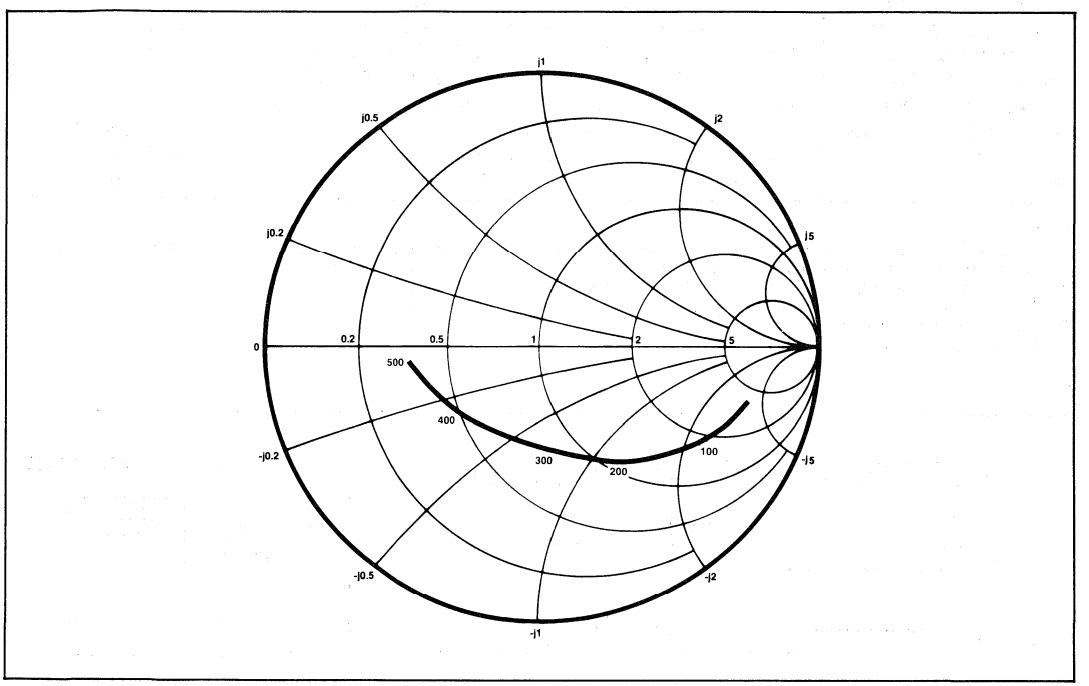


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

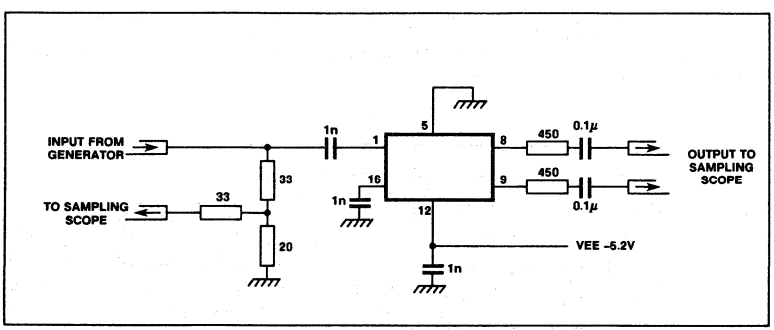


Fig. 6 Test circuit

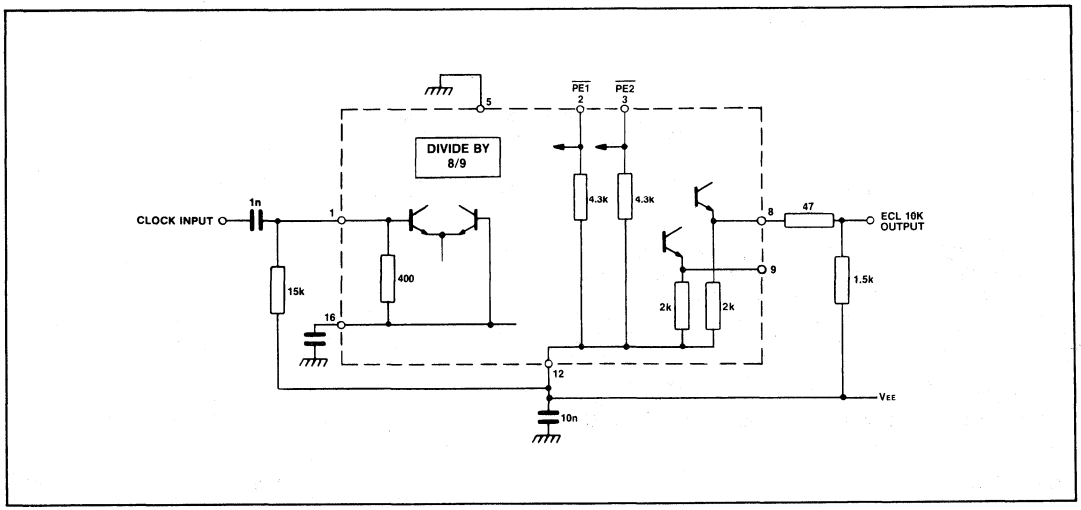


Fig.7 Typical applications circuit showing interfacing

SP8782A & B

1GHz ÷ 16/17, 32/33 MULTI-MODULUS DIVIDER

The SP8782 is a 1GHZ multi-modulus divider which divides by 16/17 when the Ratio select pin is low and 32/33 when this pin is high. The Modulus control pin selects either a divide by 16 or 32 when the pin is high or 17 or 33 when the pin is low. The device uses resynchronisation techniques to reduce the effects of propagation delays in frequency synthesis. The 'A' Grade device is characterised over the full military temperature range of -55°C to +125°C, the 'B' Grade over the industrial range of -40°C to +85°C.

FEATURES

- Advanced Resynchronising Techniques to Negate Loop Delay Effects
- CMOS Compatible Output Capability
- Multi-Modulus Division

QUICK REFERENCE DATA

- Supply Voltage Range: 4V to 5.5V
- Full Military Temperature Range:-55°C to +125°C

ORDERING INFORMATION

SP8782 A DG
SP8782 B DP
SP8782 AC DG

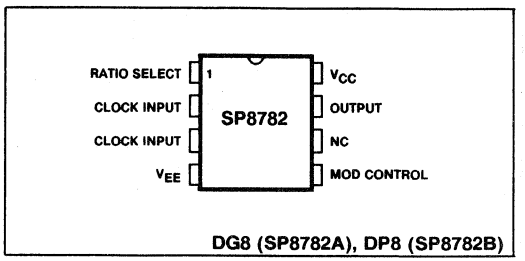


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V
Clock input level	2.5V p-p
Junction temperature	+175°C
Storage temperature range	
SP8782A	-55°C to +150°C
SP8782B	-55°C to +125°C

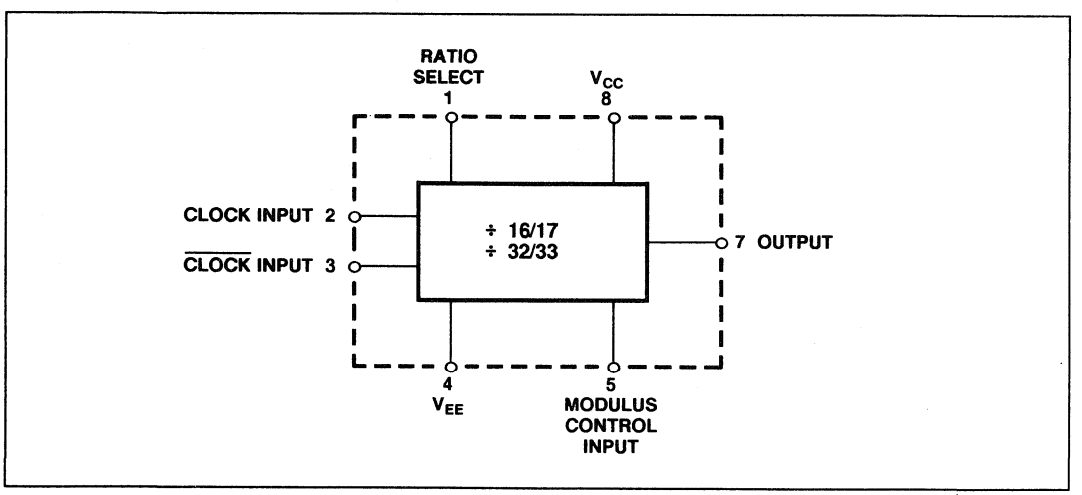


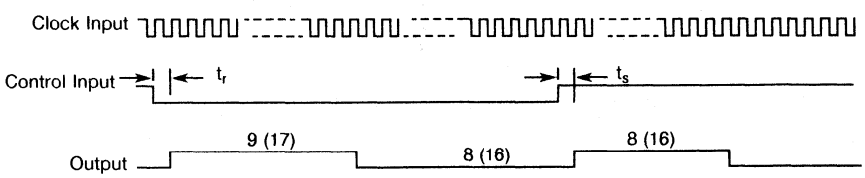
Fig.2 SP8782 functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = SP8782A: -55°C to +125°C, SP8782B -40°C to +85°C, V_{CC} = +4V to +5.5V

Characteristic	Pin	Value		Units	Conditions
		Min.	Max.		
Max. sinewave input frequency	2,3	1		GHz	Input = 200mV - 1200mV p-p
Min. sinewave input frequency	2,3		50	MHz	Input = 400mV - 1200mV p-p
Min. slew rate for LF operation	2,3		100	V/μs	
Power supply current I_{EE}	8		60	mA	Outputs unloaded, V_{CC} = 5.5V
Output low voltage	7	0	1.7	V	
Output high voltage	7	V_{CC}-1.4	V_{CC}	V	
Modulus control input high voltage	5	0.7V_{CC}	V_{CC}	V	At driver end of 3k resistor
Modulus control input low voltage	5	0	0.3V_{CC}	V	At driver end of 3k resistor
Modulus control input high current	5	0.6	1.2	mA	Via 3kΩ to V_{CC}
Modulus control input low current	5	-0.6	-1.2	mA	Via 3kΩ to 0V
Ratio select input high voltage	1	0.6V_{CC}	V_{CC}	V	
Ratio select input low voltage	1	0	0.4V_{CC}	V	
Ratio select input current	1	-10	10	μA	
Clock to output propagation delay	2,3,7		3	ns	
Set up time	5,7	3		ns	
Release time	5,7	3		ns	



TRUTH TABLE FOR CONTROL INPUTS

Modulus Control input	Ratio Control Input	
	0	1
0	÷17	÷33
1	÷16	÷32

Fig 2 Timing diagram SP8782A/B

NOTE

The set up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L → H clock pulse transition to ensure that the 16 (32) mode is selected.

The release time t_r is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the 17 (33) mode is selected.

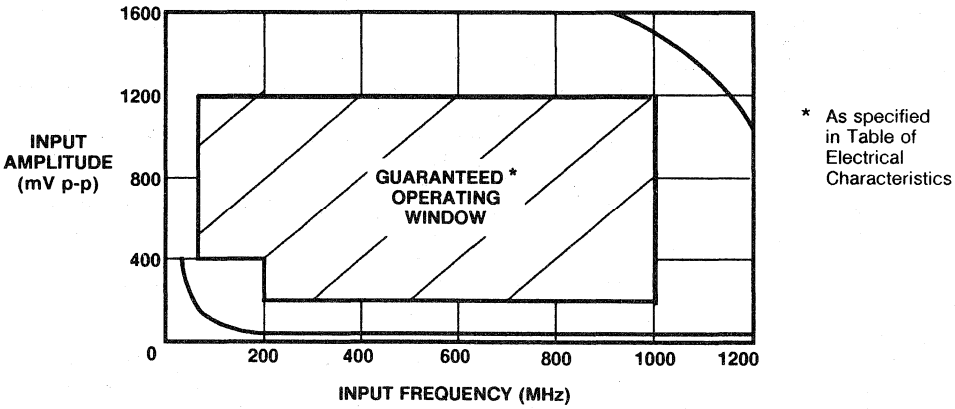


Fig.3 Typical input characteristics SP8782

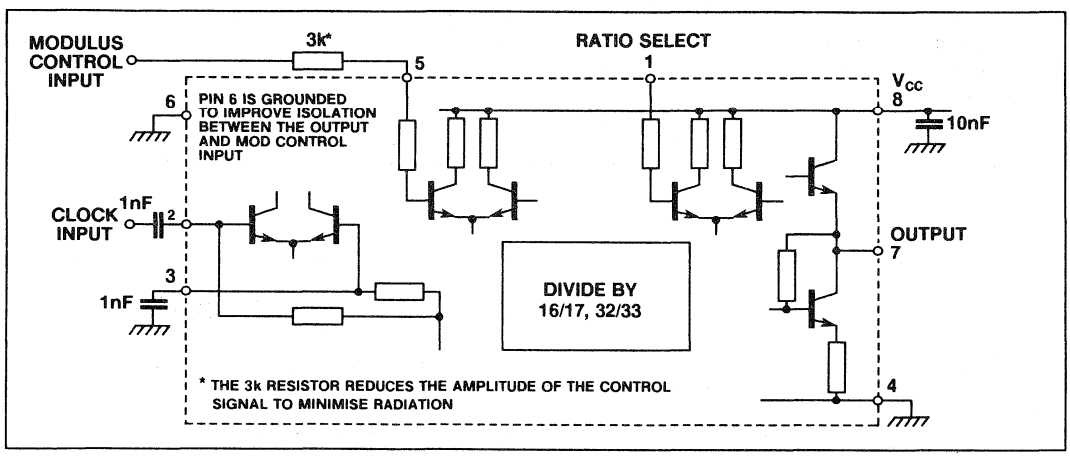


Fig.4 Typical applications showing interfacing

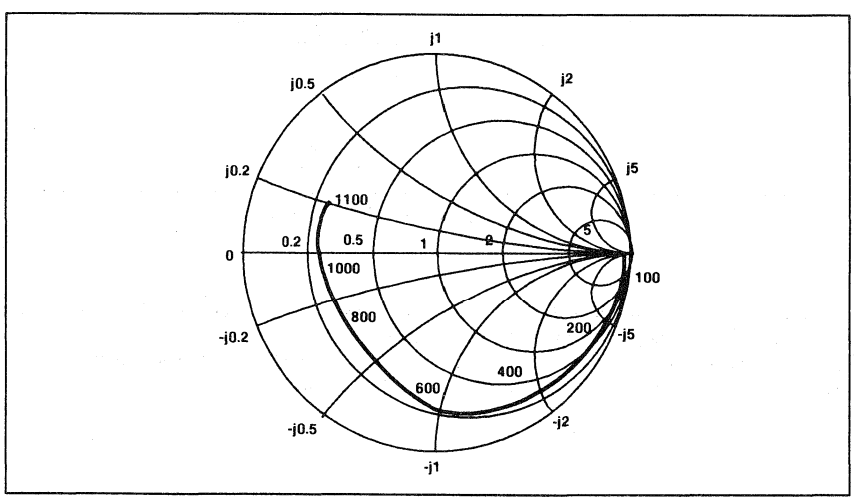


Fig.5 Typical Input Impedance. Test conditions: supply voltage 5V, ambient temperature 25°C, frequencies in MHz, impedencies normalised to 50 Ohms

SP8785 1000MHz ÷ 20/22
SP8786 1300MHz ÷ 20/22

The SP8785 and SP8786 are high speed 2 modulus counters for use up to 1.0 and 1.3GHz respectively. They feature ECL compatible control inputs and outputs and are available in either the -30°C to +70°C (B Grade) or -55°C to +125°C (A Grade) temperature ranges.

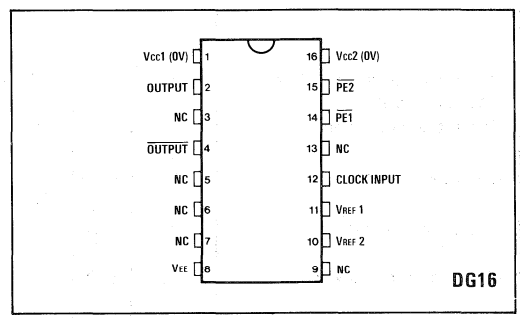


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Input
- Control Inputs ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 450mW (Typ.)
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8785 A DG
SP8785 B DG
SP8785 AA DG
SP8786 A DG
SP8786 B DG
SP8786 AA DG

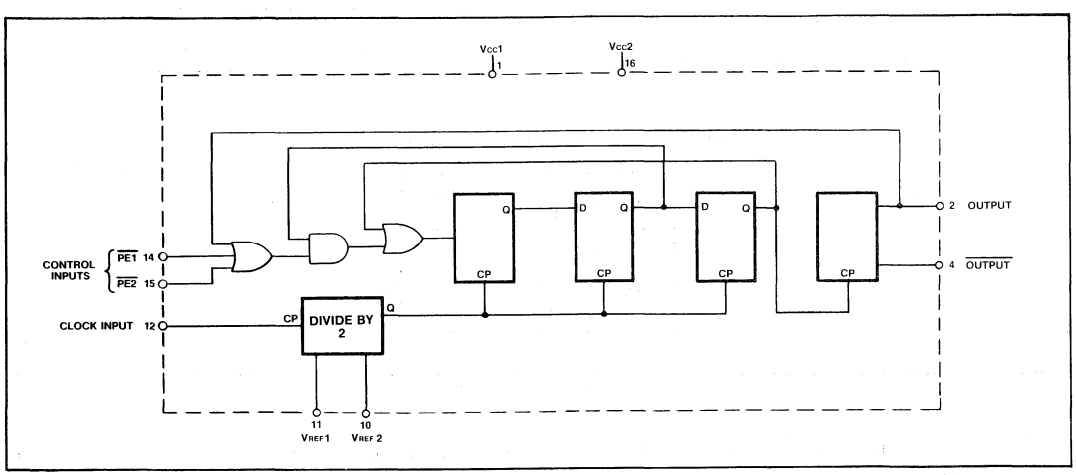


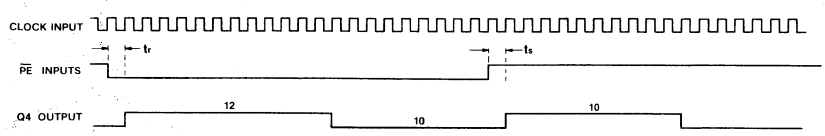
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A grade T_{case} = -55°C to +125°C (case temperature)
B grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum toggle frequency sinewave input	f_{max}	1.0		GHz	SP8785	Input = 400-1200mV p-p	Note 4
		1.3		GHz	SP8786A	Input = 600-1200mV p-p	Note 4
		1.3		GHz	SP8786B	Input = 400-1200mV p-p	Note 4
Minimum toggle frequency sinewave input	f_{min}		150	MHz	All	Input = 400-1200mV p-p	Note 5
Current consumption	I_{EE}		115	mA	All	V_{EE} = -5.2V outputs unloaded	Note 6
Output low voltage	V_{OL}	-1.85	-1.62	V	All	V_{EE} = -5.2V output load = 430Ω	
Output high voltage	V_{OH}	-0.93	-0.78	V	All	V_{EE} = -5.2V(25° C) output load = 430Ω	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE} = -5.2V(25° C) output load = 430Ω	Note 4
Clock to output delay	t_p		4	ns	All	V_{EE} = -5.2V	Note 5
Set up time	t_s	1		ns	All	V_{EE} = -5.2V	Note 5
Release time	t_r	1		ns	All	V_{EE} = -5.2V	Note 5
PE input high voltage	V_{INH}	-0.93		V	All	V_{EE} = -5.2V(25° C)	
PE input low voltage	V_{INL}		-1.62	V	All	V_{EE} = -5.2V(25° C)	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The A grade devices must be used with a heat sink to maintain chip temperature below +150°C when operating at an ambient of +125°C.
3. The temperature coefficient of V_{INL} & V_{INH} = +0.8mV/°C, of V_{OH} = +1.2mV/°C but these are not tested.
4. Tested at low and high temperatures only.
5. Guaranteed but not tested.
6. Tested at 25°C only.

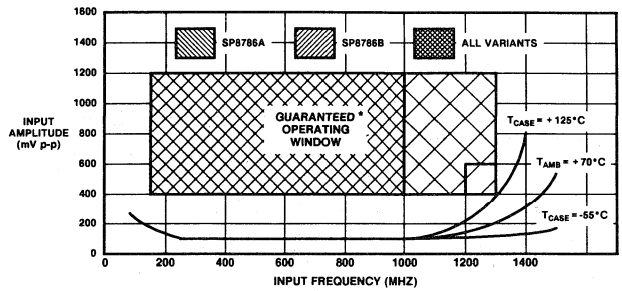


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	22
H	L	20
H	H	20
H	H	20

Fig.3 Timing diagram

NOTES
The set up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure ÷20 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷22 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical characteristics SP8786/8785

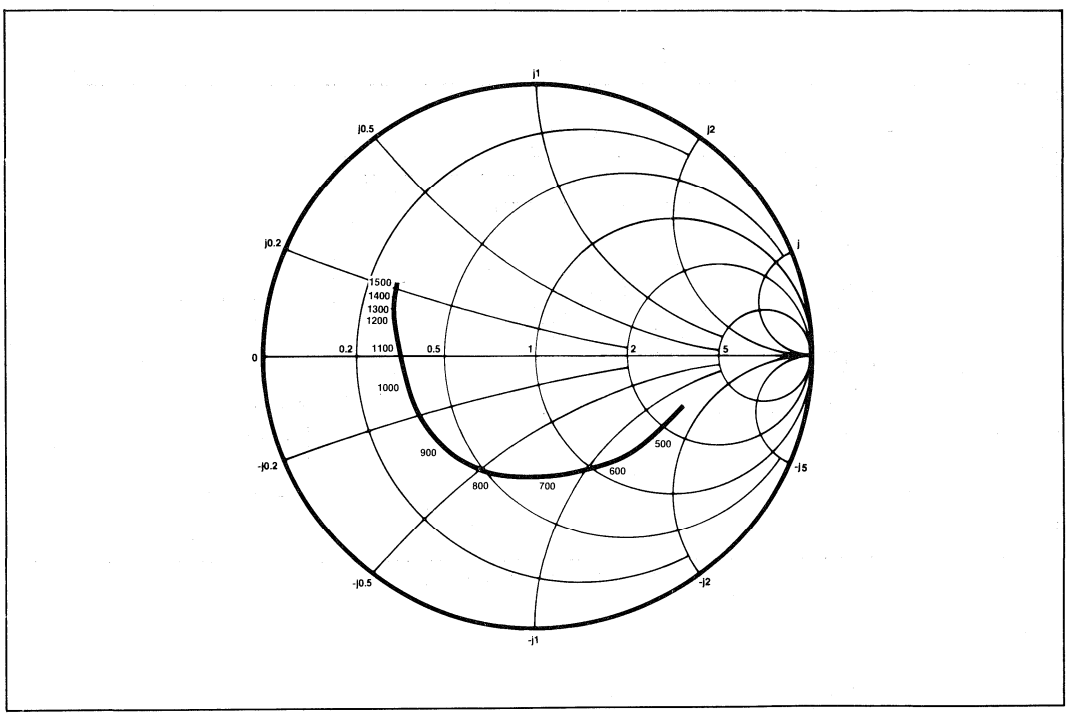


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 12) should be capacitively coupled to the signal source. The input signal path is completed by connecting a decoupling capacitor from $V_{REF}1$ (pin 11) to ground. $V_{REF}2$ (pin 10) should also be decoupled with a suitable capacitor, see Figs. 6 and 7.
2. If no signal is present the circuit device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. pin 12 to pin 8).
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The emitter follower outputs require a 430Ω pull-down resistor and are compatible with ECL III/10K. An equal load on an unused output will reduce distortion.
5. The PE inputs are ECL III/10K compatible and include a 4.3k pull-down resistor. Unused inputs can therefore be left open.
6. The input impedance of the SP8785/6 is a function of frequency, see Fig. 5. These impedance variations may give the effect of large variations in sensitivity because of the loading of the source by the device. For best results impedance matching should be used.
7. Note that all components should be suitable for the frequency in use.

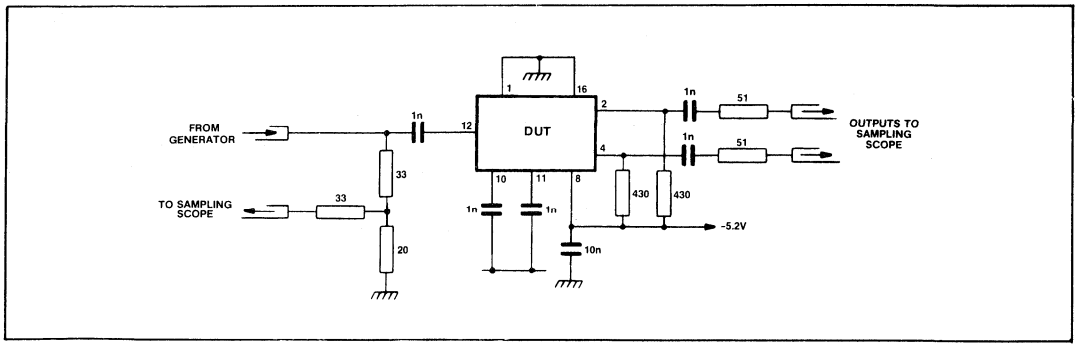


Fig.6 Toggle frequency test circuit

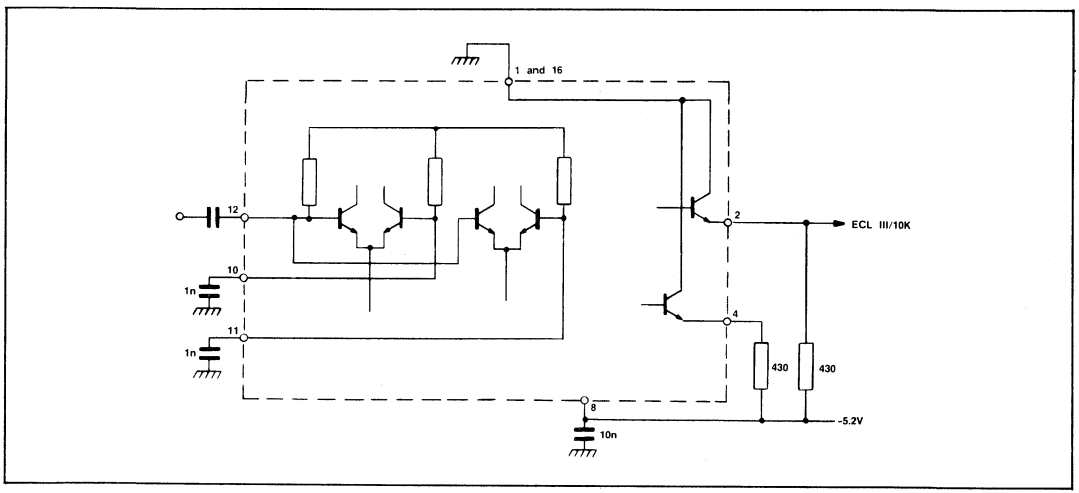


Fig.7 Typical application circuit showing interfacing

SP8789

200MHz ÷ 20/21 TWO MODULUS DIVIDER

The SP8789A is a low power programmable ÷20/21 counter which operates over the full Military temperature range. It divides by 20 when the control input is in the high state and by 21 when in the low state.

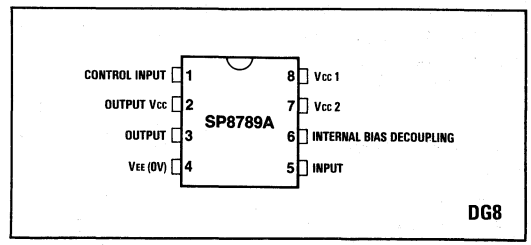


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply voltage: +5.2V
- Power consumption: 26mW Typical
- Temperature range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	6.0V Pins 7 & 8 tied
Storage temperature range:	-55° C to +150° C
Max. junction temperature:	+175° C
Max. clock input voltage:	2.5V p-p

ORDERING INFORMATION

SP8789 A DG
SP8789 AC DG

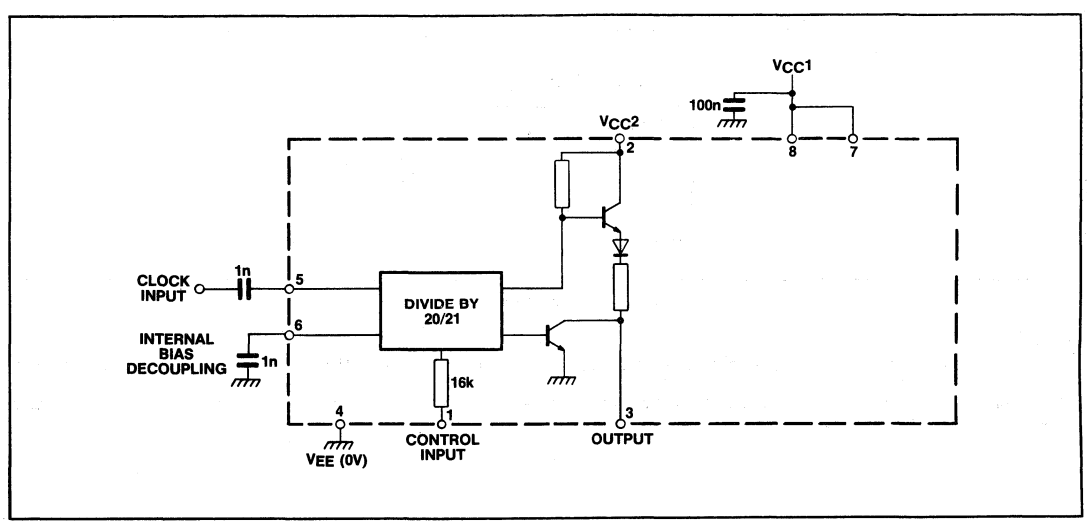


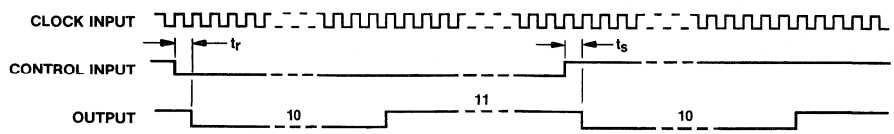
Fig.2 Function diagram SP8789A

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V; V_{EE} = 0V; Temperature T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency	f_{max}	200		MHz		Input = 200-400mV p-p
(sinewave input)		150		MHz	Note 3	Input = 200-800mV p-p
Minimum frequency	f_{min}		20	MHz	Note 3	Input = 400mV p-p
(sinewave input)			50	MHz		Input = 200mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4	5.2	V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

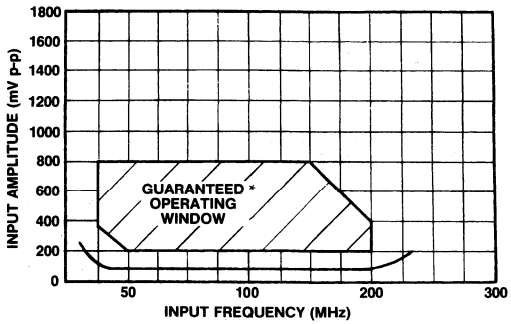


TRUTH TABLE FOR CONTROL INPUTS

Control inputs	Division ratio
0	21
1	20

Fig.3 Timing diagram SP8789A

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷20 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷21 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8789

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

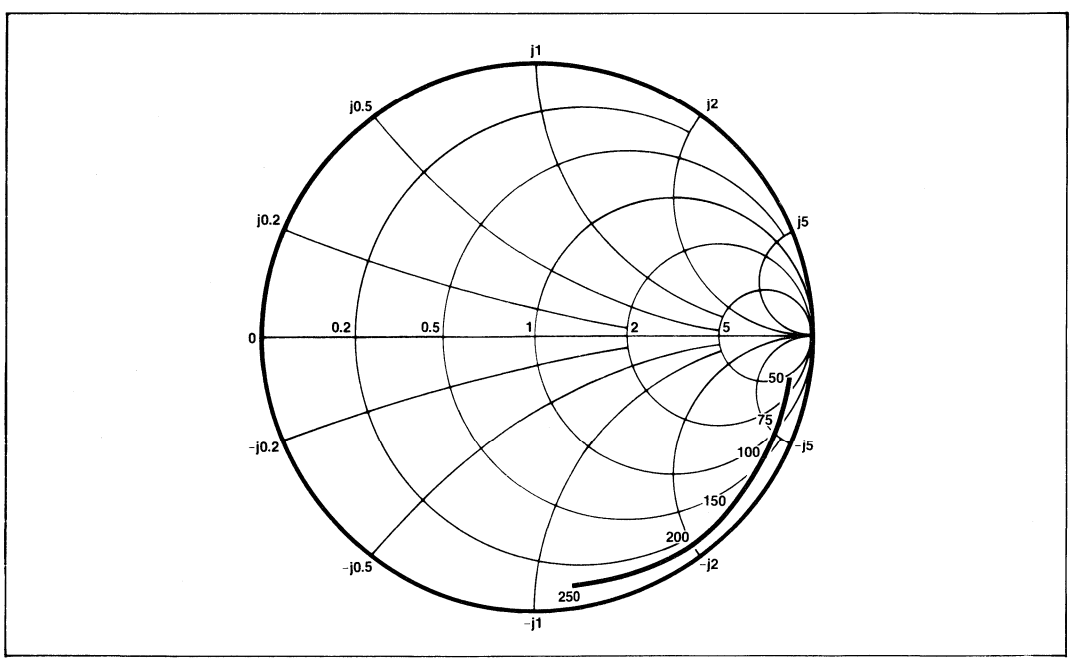


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

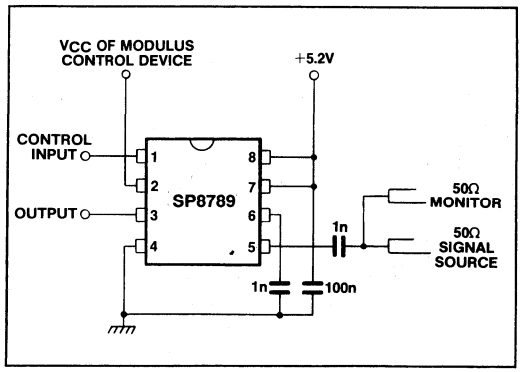


Fig.6 Toggle frequency test circuit

SP8792 200MHz ÷ 80/81
SP8793 200MHz ÷ 40/41

The SP8792A and SP8793A are low power programmable ÷80/81 and ÷40/41 counters which operate over the full Military temperature range. They divide by 80(40) when the control input is in the high state and by 81(41) when in the low state.

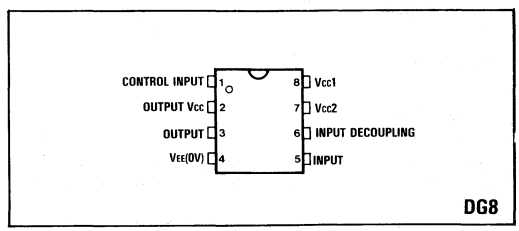


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply Voltage: +5.2V
- Power Consumption: 26mW typical
- Temperature Range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V pins 7 & 8 linked
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8792 A DG
SP8792 AB DG
SP8792 AC DG
SP8793 A DG
SP8793 AB DG
SP8793 AC DG

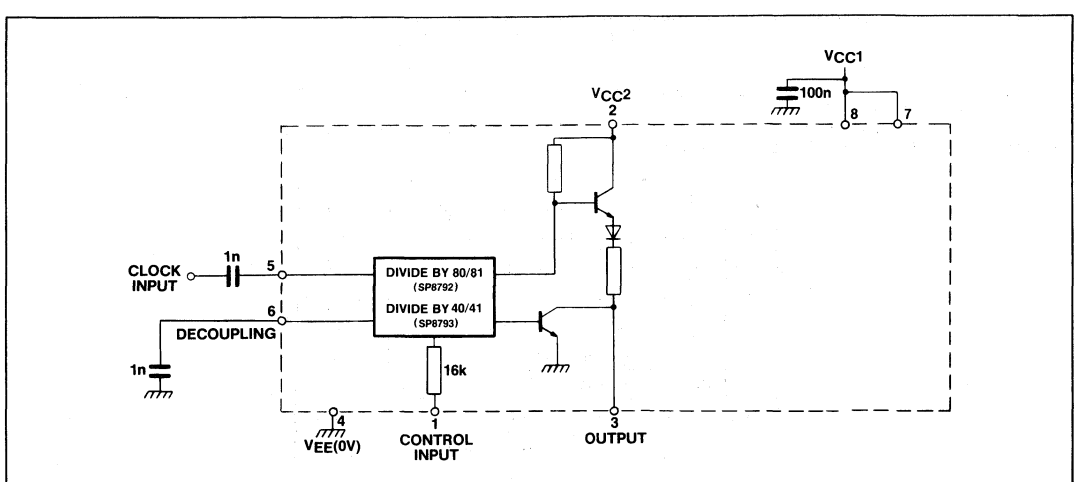


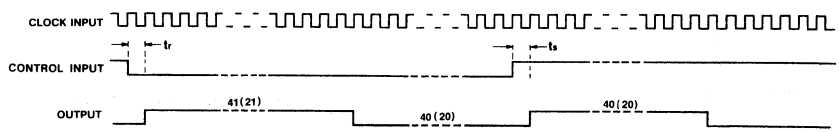
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.25V V_{EE} = 0V
Temperature: T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	200		MHz	Input =200 - 400mV p-p	
		150		MHz	Input =200 - 800mV p-p	Note 3
Minimum frequency (sinewave input)	f_{min}		20	MHz	Input =400mV p-p	
Power supply current	I_{EE}		7	mA		Note 4
Control input high voltage	V_{INH}	4		V		Note 4
Control input low voltage	V_{INL}		2	V		Note 4
Output high voltage	V_{OH}	2.4		V	Pins 2,7 and 8 linked V_{CC}= 4.95V I_{OH}= -100μA	Note 4
Output low voltage	V_{OL}		0.5	V	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA	Note 4
Set-up time	t_s	14		ns	25° C	Note 3
Release time	t_r	20		ns	25° C	Note 3
Clock to output propagation time	t_p		45	ns	25° C	Note 3

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

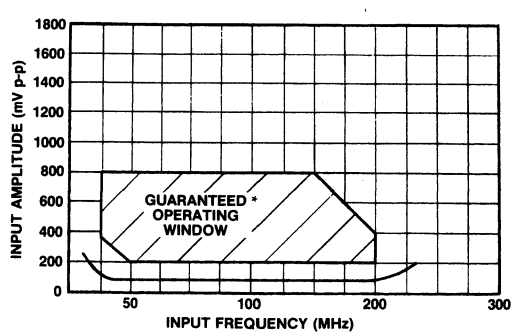


TRUTH TABLE FOR CONTROL INPUTS

Control Inputs	Division Ratio	
	SP8792A	SP8793A
0	81	41
1	80	40

Fig.4 Input sensitivity (SP8792/3A)

NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L → H transition of the control input and the next L→H clock pulse transition to ensure that the ÷80(40) mode is selected.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷81(41) mode is selected.



OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, pin 6 to ground.
2. The output stage which is normally open collector (pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k or greater resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then pin 2, 7, and 8 should be connected together to give a fan-out = 1. Alternatively, the open collector output may be used with a pull-up resistor.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the circuit will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8792/3 to be used at supply voltages up to 9.5V is NOT available for use in the A Grade device: the SP8792A and SP8793A are ONLY available for operation from 5.2V supply, and therefore pins 7 and 8 should always be externally connected together.

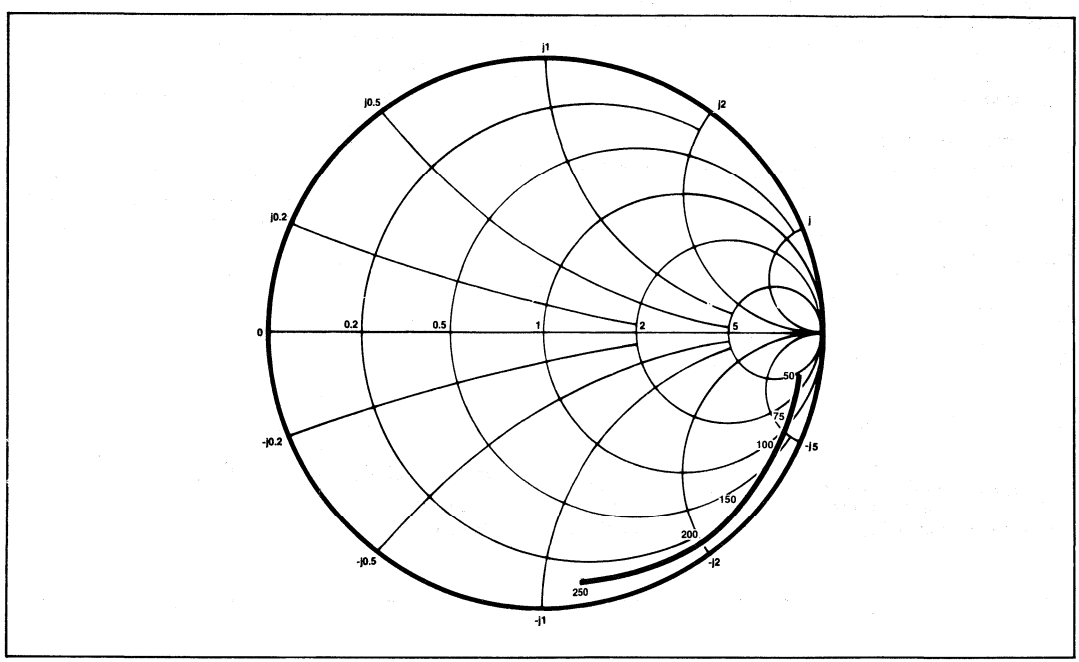


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

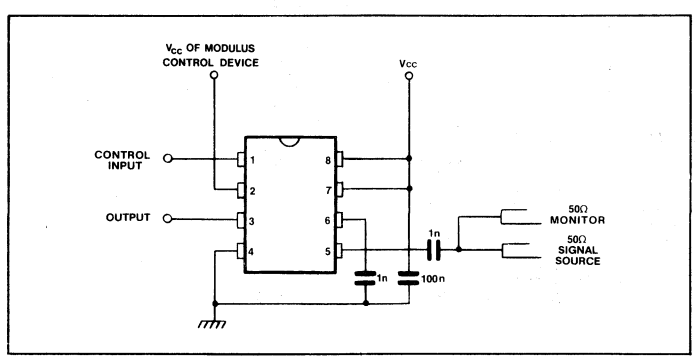


Fig.6 Toggle frequency test circuit

SP8795

200MHz ÷ 32/33 TWO MODULUS DIVIDER

The SP8795A is a low power programmable ÷32/33 counter which operates over the full Military temperature range. It divides by 32 when the control input is in the high state and by 33 when in the low state.

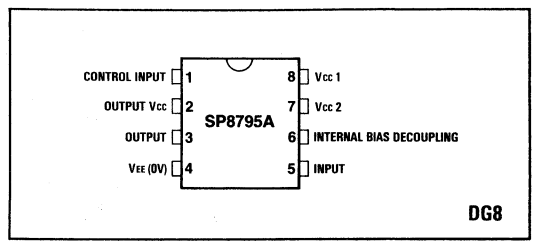


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply voltage: +5.2V
- Power consumption: 26mW typical
- Temperature range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	6.0V Pins 7 & 8 tied
Storage temperature range:	-55°C to +150°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p

ORDERING INFORMATION

SP8795 A DG
SP8795 AC DG

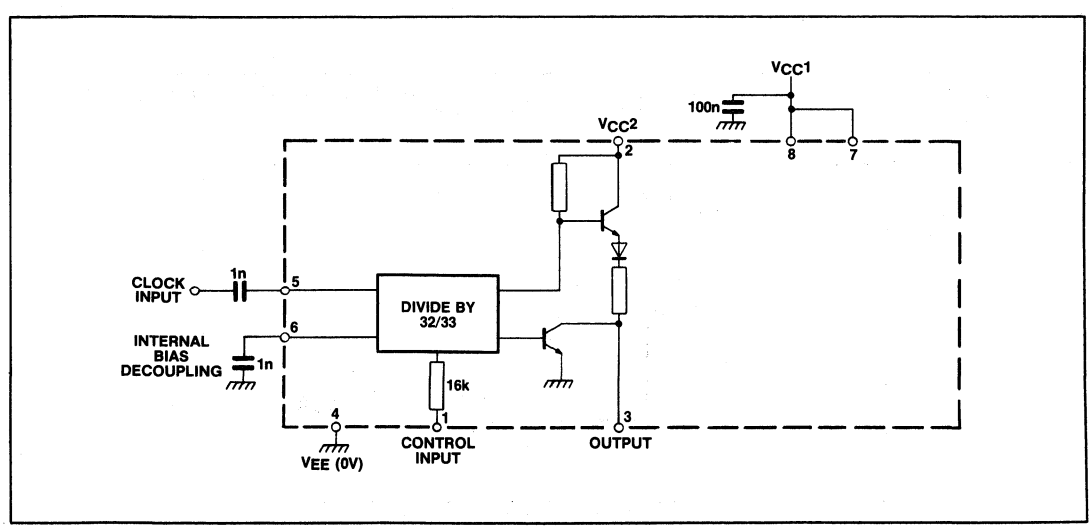


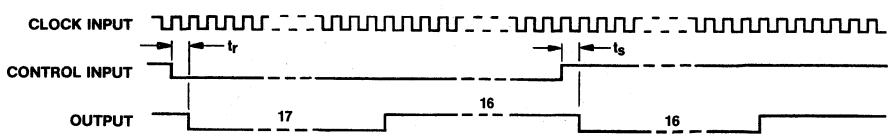
Fig.2 Function diagram SP8795A

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V; V_{EE} = 0V; Temperature T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency	f_{max}	200		MHz		Input = 200-400mV p-p
(sinewave input)		150		MHz	Note 3	Input = 200-800mV p-p
Minimum frequency	f_{min}		20	MHz	Note 3	Input = 400mV p-p
(sinewave input)			50	MHz		Input = 200mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4	5.2	V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

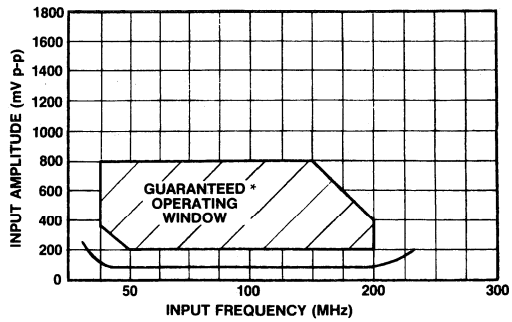


TRUTH TABLE FOR CONTROL INPUTS

Control inputs	Division ratio
0	33
1	32

Fig.3 Timing diagram SP8795A

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷32 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷33 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8795A

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8795 to be used at supply voltages up to 9.5V is *NOT* available for use in the A Grade device: the SP8795A is *ONLY* available for operation from 5.2V supply, and therefore Pins 7 and 8 should always be externally connected together.

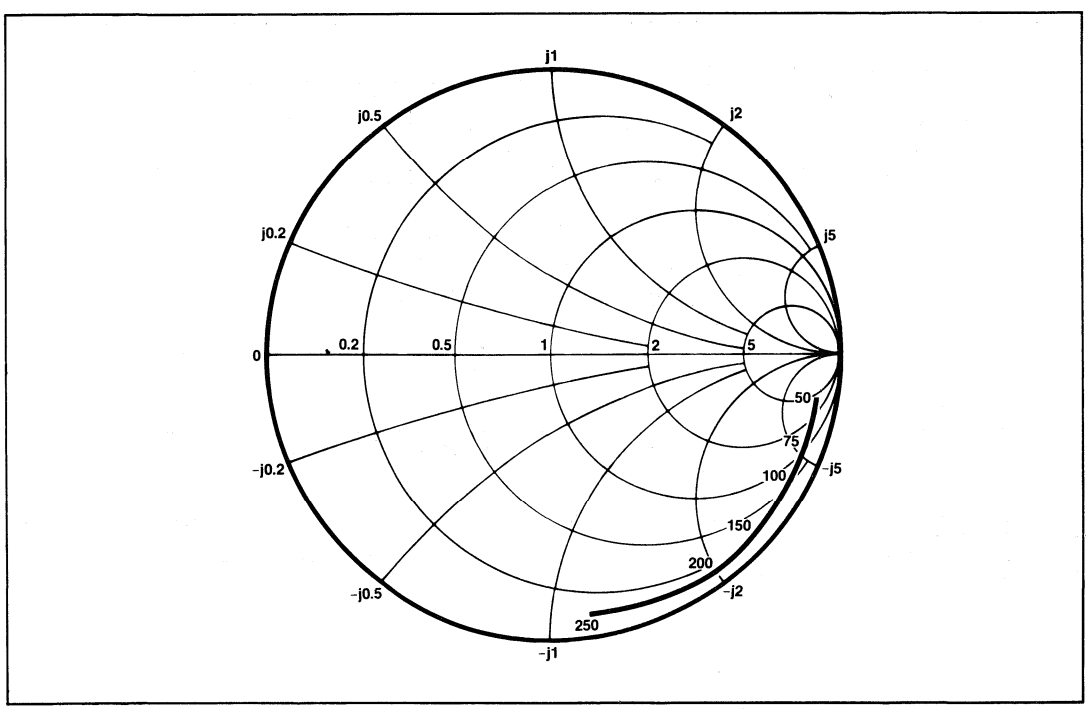


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

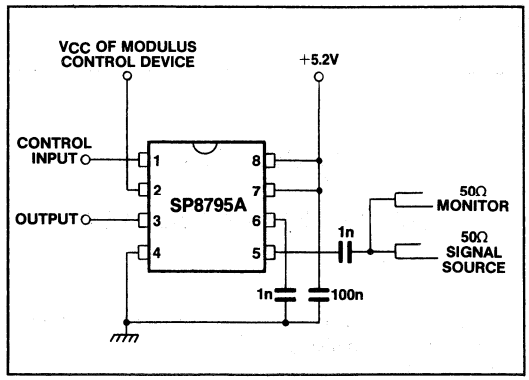


Fig.6 Toggle frequency test circuit

SP8797

225MHz ÷ 32/33 PRESCALER

The SP8797 is a low power programmable ÷32/33 counter which operates over the full military temperature range. It divides by 32 when the control input is in the high state and by 33 when in the low state.

FEATURES

- Very Low Power
- Control Input and Output CMOS and TTL Compatible
- AC Coupled Input
- Buffer Amp for Good Reverse Isolation
- Operation Up to 9.5V Using Internal Regulator

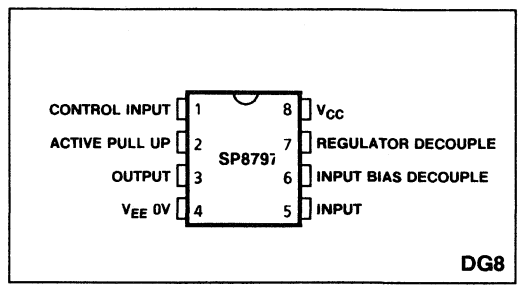


Fig 1 Pin Connections - top view

QUICK REFERENCE DATA

- Supply voltage: 4.5V to 9.5V
- Power consumption 65mW at V_{CC} = 9.5V
- Temperature range: -55°C to +125°C

ORDERING INFORMATION

SP8797 A DG

ABSOLUTE MAXIMUM RATINGS

Supply voltage pin 7	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C
Supply Voltage pin 8	13.5V

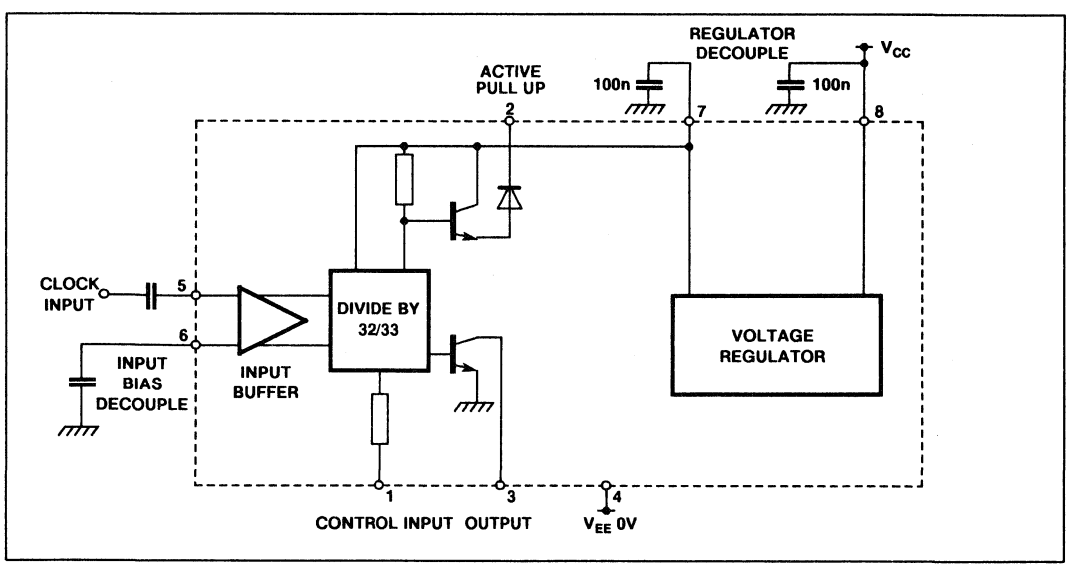
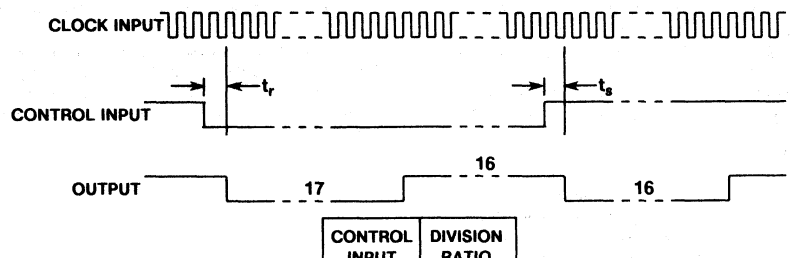


Fig 2 SP8797 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} = +4.5V to 5.5V Tamb = -55°C to +125°C

Characteristic	Sym	Value		Units	Conditions
		Min.	Max.		
Supply current	I_{CC}		7.8	mA	
Maximum frequency (sinewave input)	f_{MAX}	225		MHz	Input = 200mV to 800mV p-p
Minimum frequency (sinewave input)	f_{MIN}		20	MHz	Input = 200mV to 800mV p-p
Control input high voltage	V_{INH}	2	5.5	V	Pin 7 Voltage = 5.5V
Control input low voltage	V_{INL}	0	0.8	V	
Output high voltage	V_{OH}	2.5		V	Pin 2 connected to pin 3 V_{CC} = 4.5V I_{OH} = 100µA
Output low voltage	V_{OL}		0.5	V	Pin 2 connected to pin 3 IOL = 1.6mA
Set up time	t_s	14		ns	25°C
Release time	t_r	20		ns	25°C
Clock to output propagation time	t_p		45	ns	25°C



CONTROL INPUT	DIVISION RATIO
0	33
1	32

TRUTH TABLE FOR CONTROL INPUTS

Fig.3 Timing diagram SP8797A

NOTES

The set up time t_s is defined as the minimum time that can elapse between the LOW to HIGH transition of control input and the next LOW to HIGH clock pulse transition to ensure ÷32 mode is selected.

The release time t_r is defined as the minimum time that can elapse between the HIGH to LOW transition of the control input and the next LOW to HIGH clock pulse transition to ensure ÷33 mode is selected.

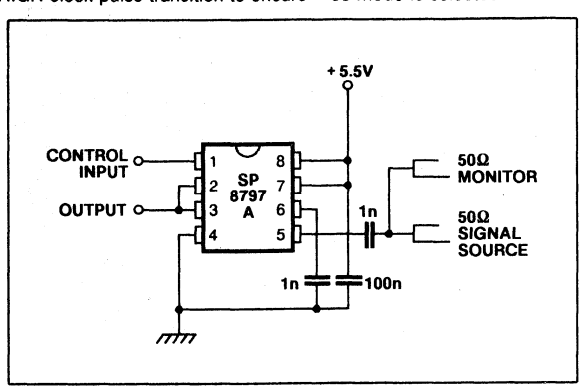


Fig.4 Toggle frequency test circuit

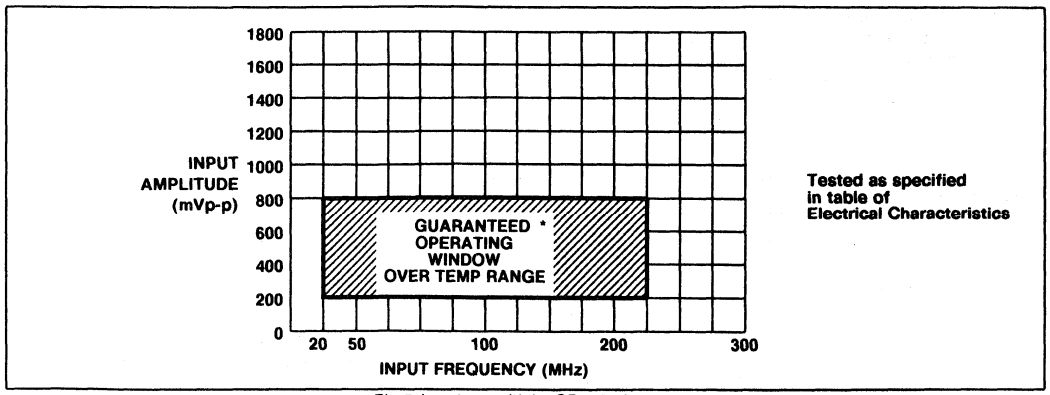


Fig.5 Input sensitivity SP8797A

OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output on pin 3 is an open collector and can be interfaced to CMOS by connecting a pull up resistor to a positive supply of up to +9.5V. The sink current through this resistor should not exceed 2mA. When an interface to TTL is required, the active pull up on pin 2 should be connected to pin 3, giving a fan out of 1. The supply current will be increased by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/µs is required on the clock input.
4. The mark to space ratio at the output is approximately 1.2:1 at 225 MHz.
5. Input impedance is a function of frequency. See Fig.6.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 680K resistor between the unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.

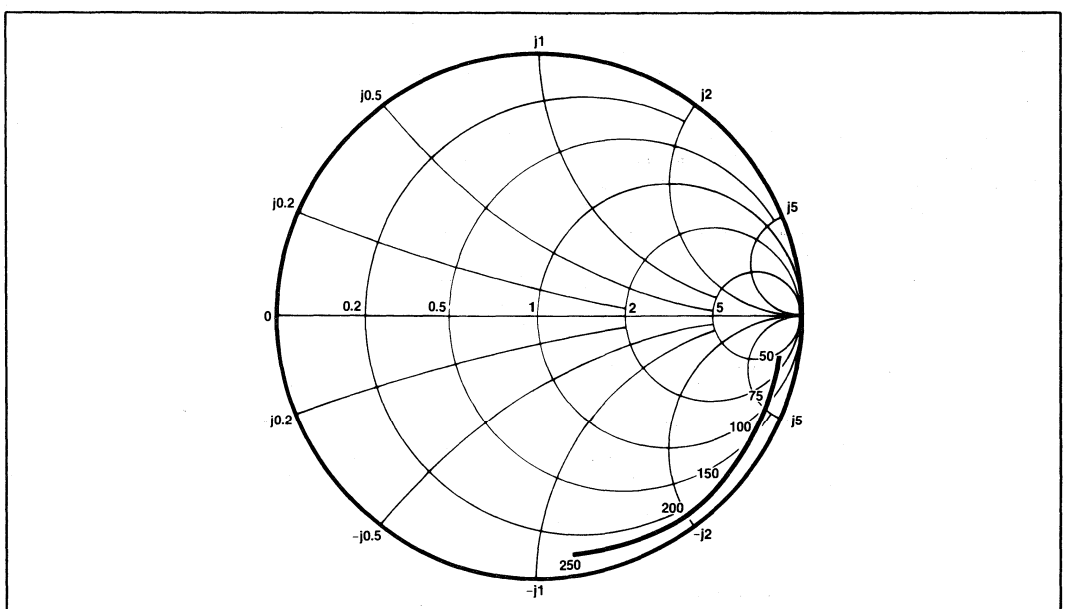


Fig.6 Typical input impedance. Test conditions: supply voltage 5.2V,ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

SP8799

200MHz ÷ 10/11 TWO MODULUS DIVIDER

The SP8799A is a low power programmable ÷10/11 counter which operates over the full Military temperature range. It divides by 10 when the control input is in the high state and by 11 when in the low state.

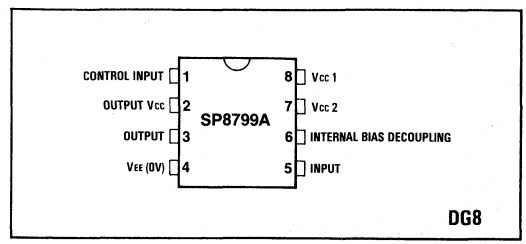


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply voltage: +5.2V
- Power consumption: 26mW typical
- Temperature range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	6.0V Pins 7 & 8 tied
Storage temperature range:	-55°C to +150°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p

ORDERING INFORMATION

SP8799 A DG
SP8799 AC DG
Please contact your local GPS Sales Office for details of plastic variants

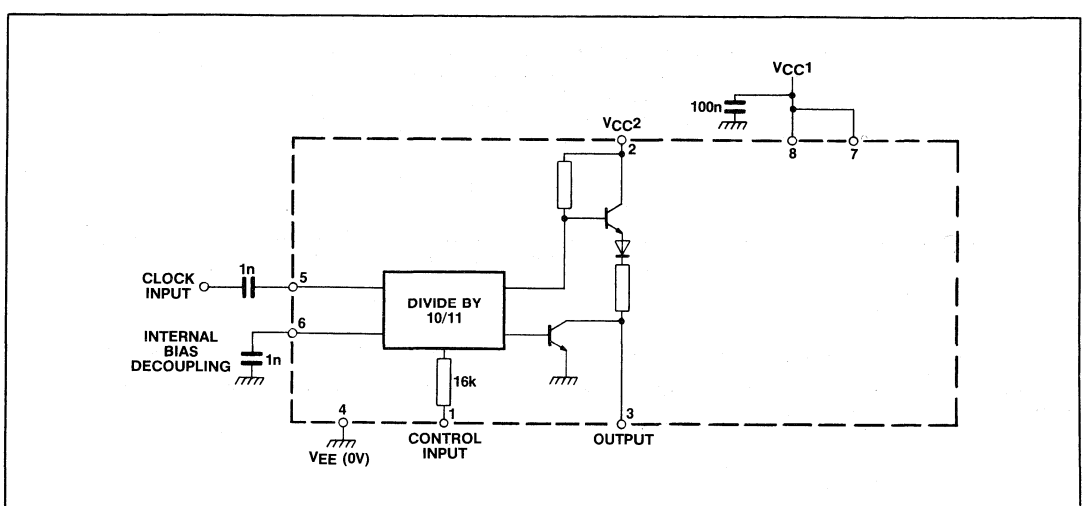


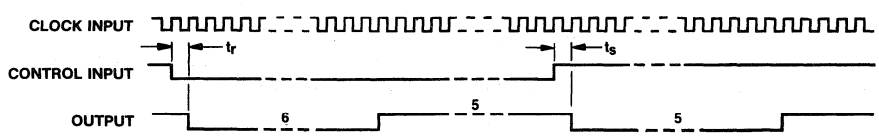
Fig.2 Function diagram SP8799A

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V; V_{EE} = 0V; Temperature T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency	f_{max}	200		MHz		Input = 200-400mV p-p
(sinewave input)		150		MHz	Note 3	Input = 200-800mV p-p
Minimum frequency	f_{min}		20	MHz	Note 3	Input = 400mV p-p
(sinewave input)			50	MHz		Input = 200mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4	5.2	V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

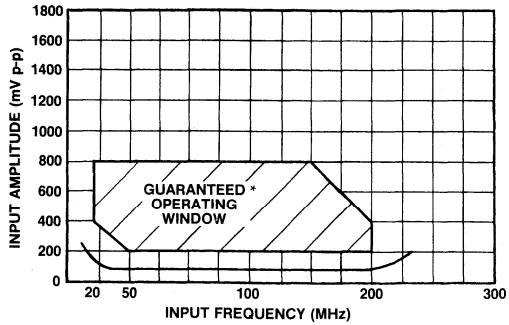


TRUTH TABLE FOR CONTROL INPUTS

Control inputs	Division ratio
0	11
1	10

Fig.3 Timing diagram SP8799A

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷10 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷11 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8799A

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the Input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8799 to be used at supply voltages up to 9.5V is *NOT* available for use in the A Grade device: the SP8799A is *ONLY* available for operation from 5.2V supply, and therefore Pins 7 and 8 should always be externally connected together.

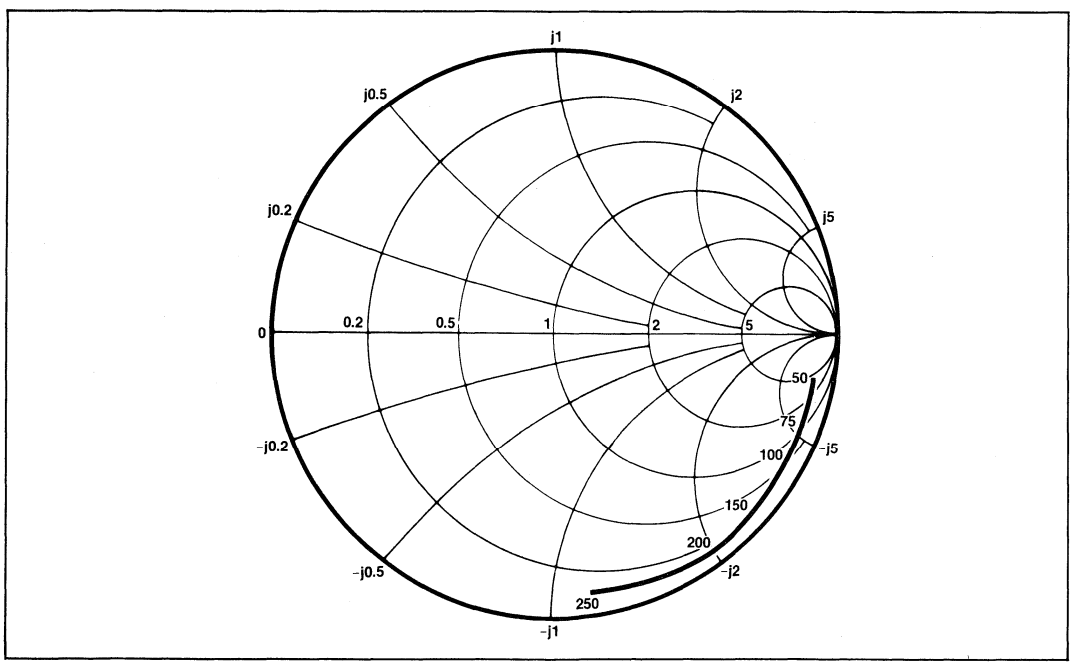


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

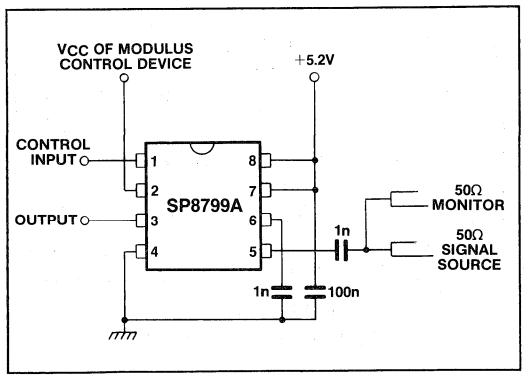


Fig.6 Toggle frequency test circuit

SP8600

250MHz ÷ 4

(NOT RECOMMENDED FOR NEW DESIGNS)

The SP8600 is an asynchronous ECL counter with open collector outputs. It requires external input bias and an AC coupled input signal of 600mV p-p.

FEATURES

- Open Collector Output
- AC Coupled Input

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Max. Input Frequency: 250MHz
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

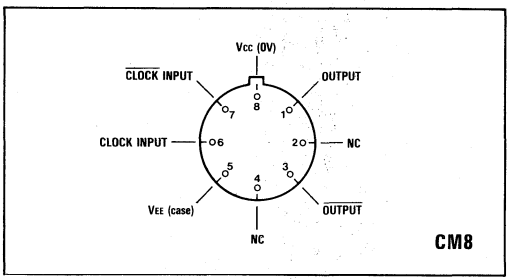


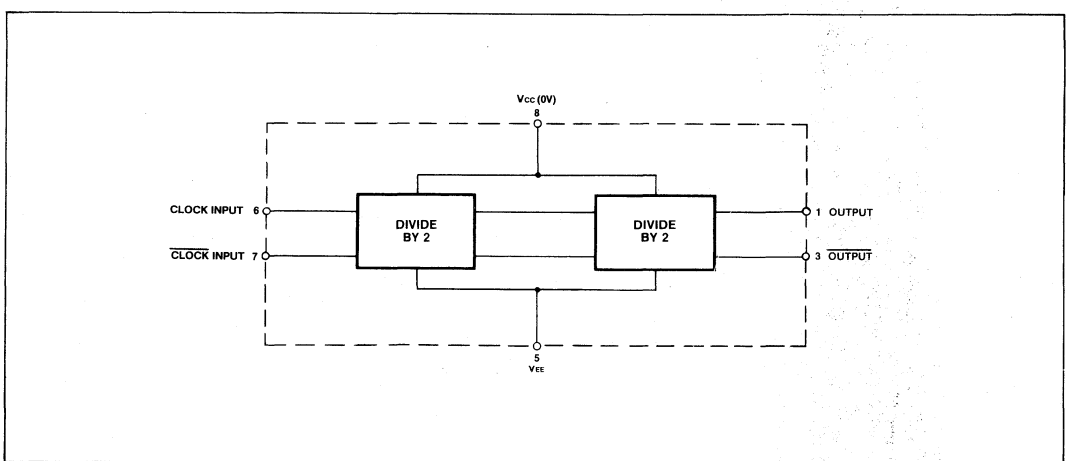
Fig.1 Pin connections - bottom view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-10V
Output voltage (Pins 1 and 3)	VEE +14V
Storage temperature range	-55°C to +175°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8600 A CM
SP8600 B CM
SP8600 AB CM
SP8600 AC CM

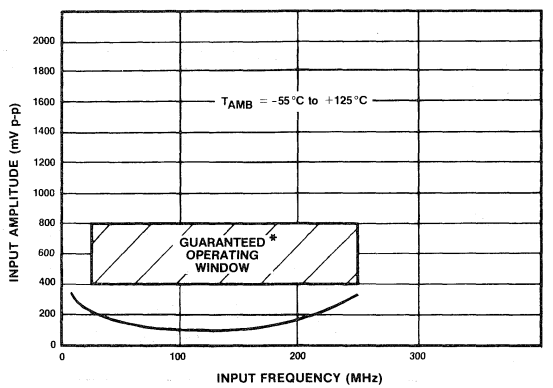


ELECTRICAL CHARACTERISTICS

Supply voltage: V_{EE} = -5.2V ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV
Minimum frequency (sinewave input)	f_{min}		25	MHz	Input = 400-800mV
Power supply current	I_{EE}		25	mA	V_{EE} = -5.2V
Output current	I_{OUT}	1.65		mA	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig. 5.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics of SP8600A

OPERATING NOTES

1. The input is normally AC coupled to one of the inputs or, if complementary signals are available, to both inputs. The inputs require an external bias as shown in Fig.5.
2. If no signal is present the device will self-oscillate. If this is undesirable this can be prevented by offsetting the two inputs by approximately 40mV as shown in Fig. 6.
3. The outputs are in the form of complementary free collectors with about 2mA available from them over full temperature range. The outputs can be interfaced to ECL or Schottky TTL as shown in Fig. 7.
4. For maximum frequency operation the output load resistor values must be such that the output transistors will not saturate. If the output load resistors are connected to 0V then saturation occurs with resistor values greater than 600 ohms. If only one output is used the other output can be connected to 0V.
5. The input can be operated down to DC but input slew rate must be better than 20V/µs.
6. The input impedance varies as a function of frequency. See Fig. 4.

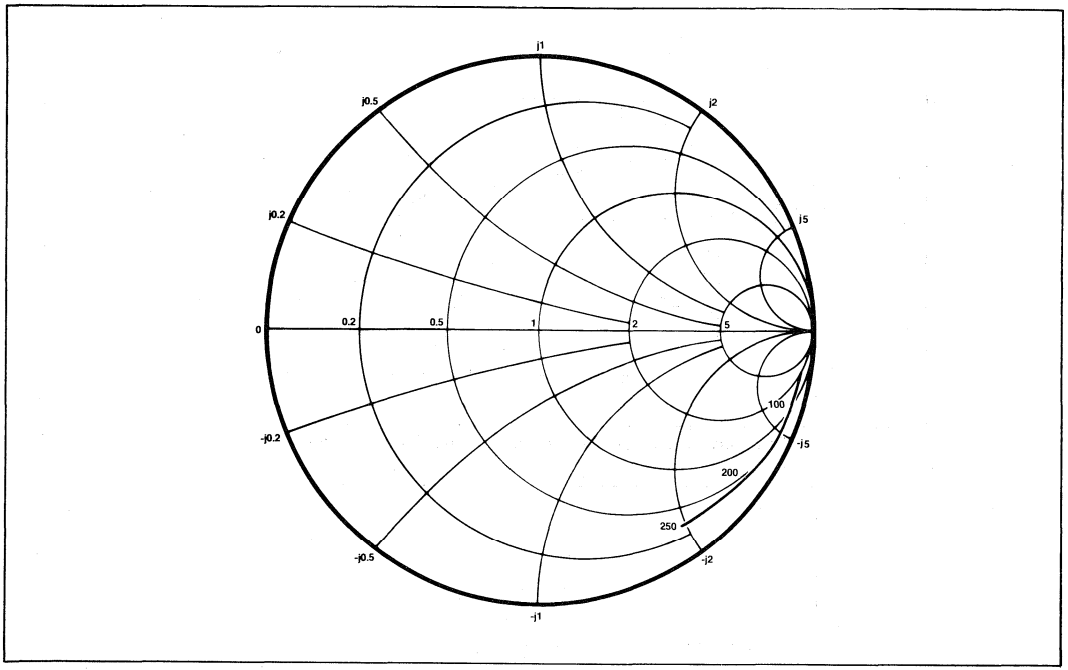


Fig.4 Typical input impedance: supply voltage -5.2V, temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

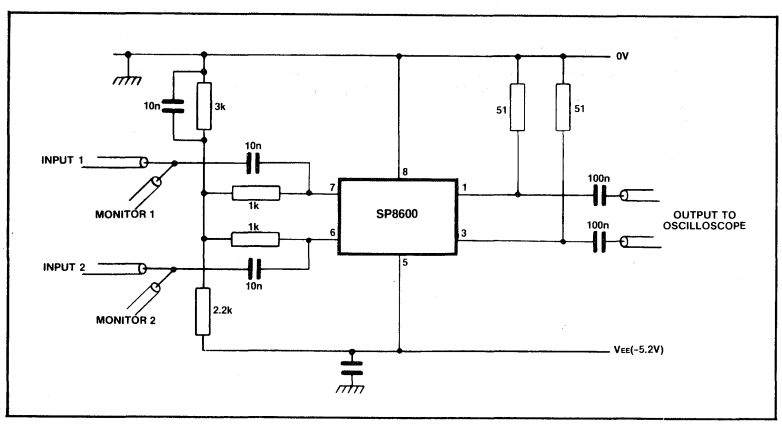


Fig.5 Test circuit

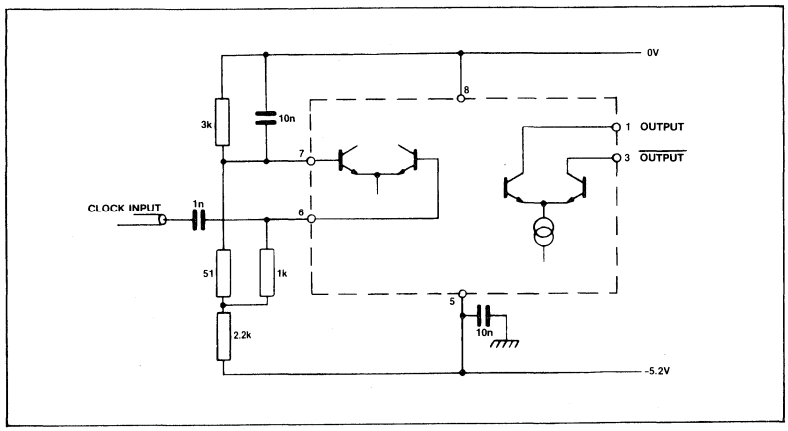


Fig.6 Biasing to prevent oscillation under no signal conditions

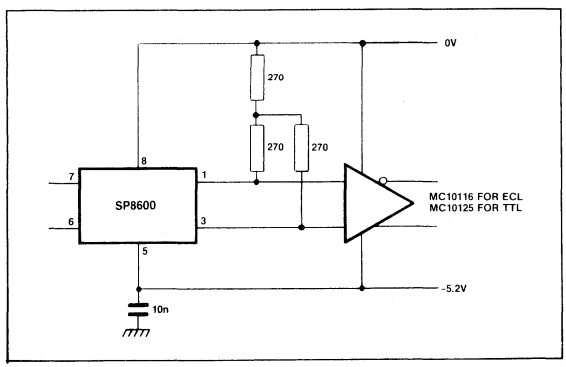


Fig.7 Interfacing to ECL and Schottky TTL

SP8601

150MHz ÷ 4

(NOT RECOMMENDED FOR NEW DESIGNS)

The SP8601 is an asynchronous ECL counter with a current steered output which can be used to drive TTL or CMOS. Biased externally, it may be directly driven from an ECL II source.

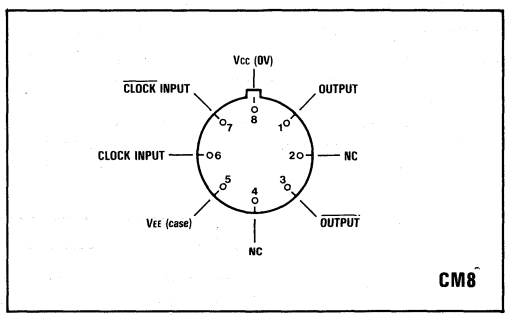


Fig.1 Pin connections - bottom view

FEATURES

- Current steered output can drive TTL or CMOS
- AC or DC Coupled Input
- Inputs ECL II Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-10V
Output voltage (Pins 1 and 3)	VEE +14V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8601 A CM
SP8601 B CM
SP8601 AB CM
SP8601 AC CM

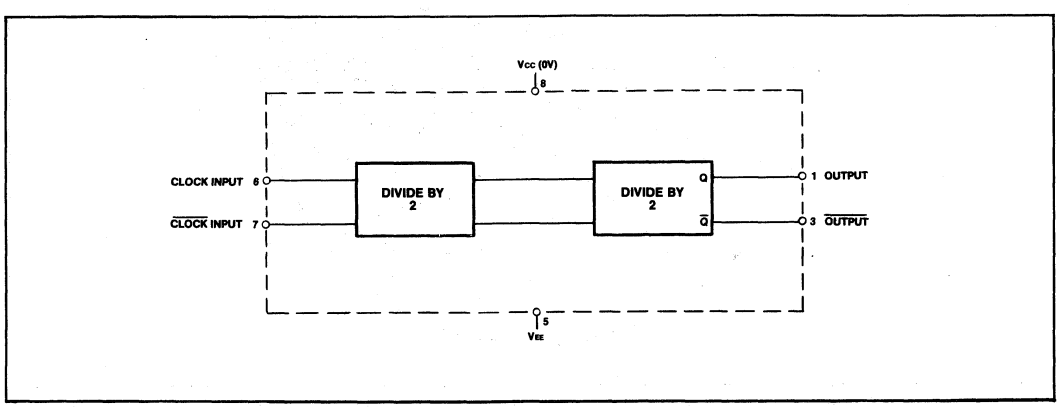


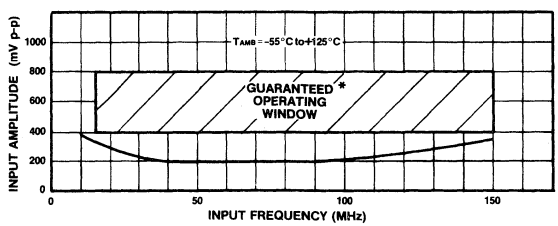
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input = 400-800mV p-p
Minimum frequency (sinewave input)	f_{min}		15	MHz	Input = 400-800mV p-p
Power supply current	I_{EE}		25	mA	V_{EE} = -5.2V
Output current	I_{OUT}	1.6		mA	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig. 5.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical characteristic of SP8601A

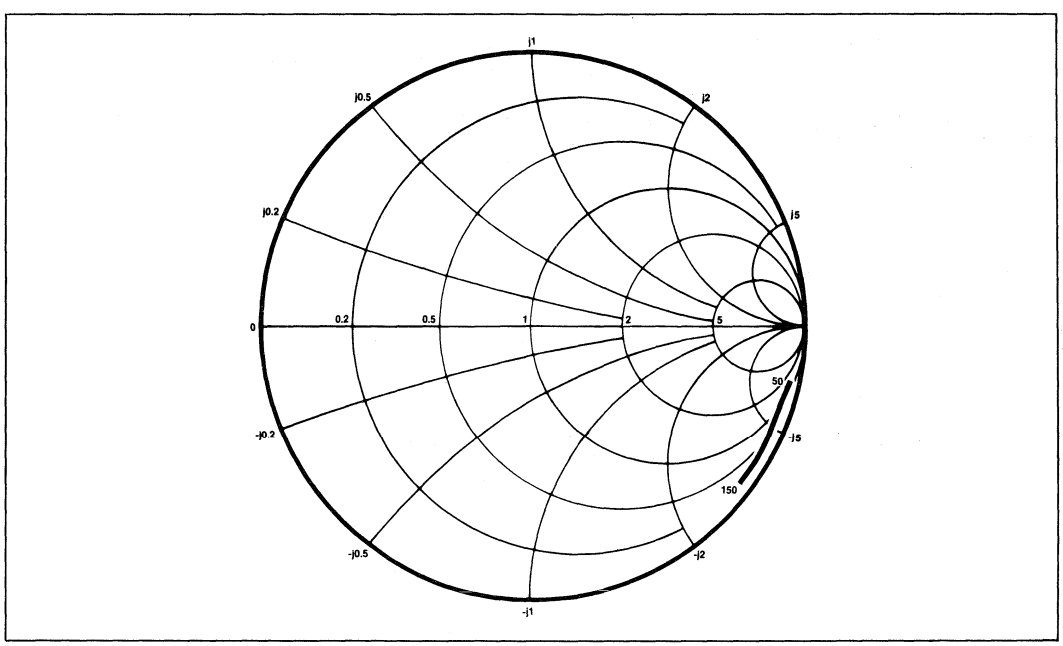


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The signal source can be capacitively coupled to the clock input if input bias is provided (See Fig.6) but is normally directly coupled with ECL II levels. The inputs can be operated either singly or with double complementary input drive.
2. The outputs are in the form of complementary free collectors with 1.6mA available from them over full military temperature range (A grade). The outputs can be interfaced to ECL or Schottky TTL as shown in Figs. 6 and 7. Interfacing to TTL at frequencies above 20MHz requires low capacitance interconnections and the use of Schottky TTL.
3. For maximum frequency operation the output load resistor values must be such that the output transistors will not saturate. If the output load resistors are connected to 0V then saturation will occur with resistor values greater than 600Ω. If only one output is used the other output can be connected to 0V. See Table 1 for typical variation of maximum input frequency with output load resistor.

Minimum Output Voltage (mV)	Load Resistor (ohms)	Input Frequency (MHz)
1100	1000	120
320	200	150
80	50	180

Table 1

4. Input impedance is a function of frequency. See Fig.4.
5. The input can be operated down to DC but input slew rate must be better than 20V/μs.
6. All components should be suitable for the frequency in use.

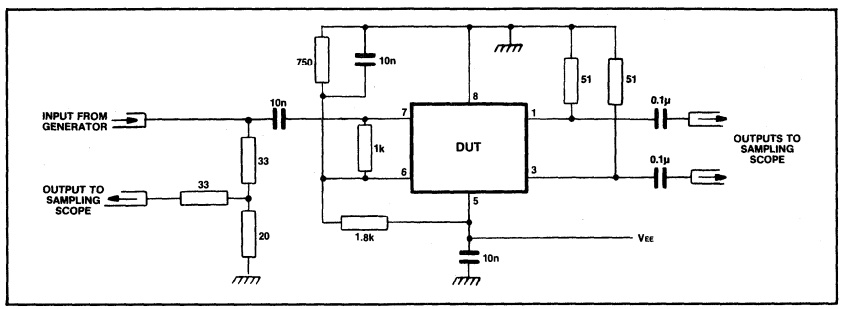


Fig.5 Test circuit

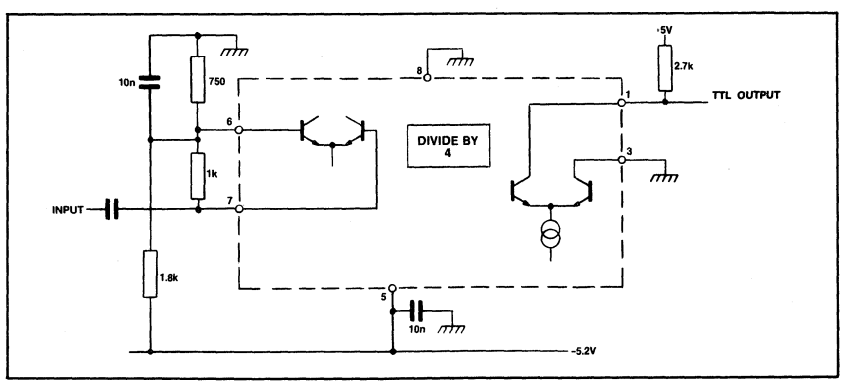


Fig.6 Typical application showing interfacing

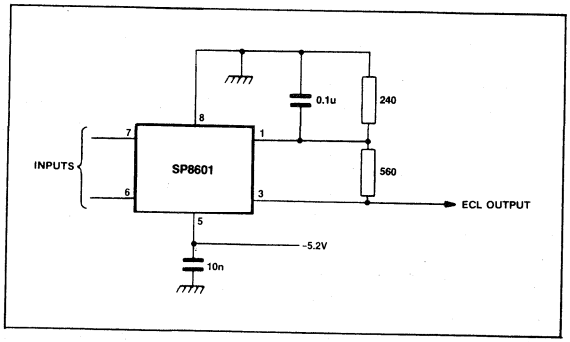


Fig.7 Interfacing to ECL

SP8602 500MHz ÷ 2
SP8604 300MHz ÷ 2

The SP8602 and SP8604 are emitter coupled logic dividers which feature ECL 10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

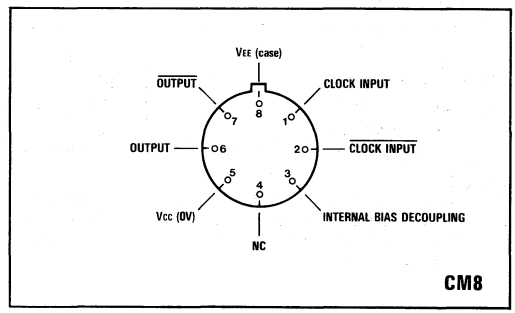


Fig.1 Pin connections - bottom view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	10mA
Storage temperature range	-55°C to +175°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8602 A CM
SP8602 B CM
SP8602 AB CM
SP8602 AC CM
SP8604 A CM
SP8604 B CM
SP8604 AB CM
SP8604 AC CM

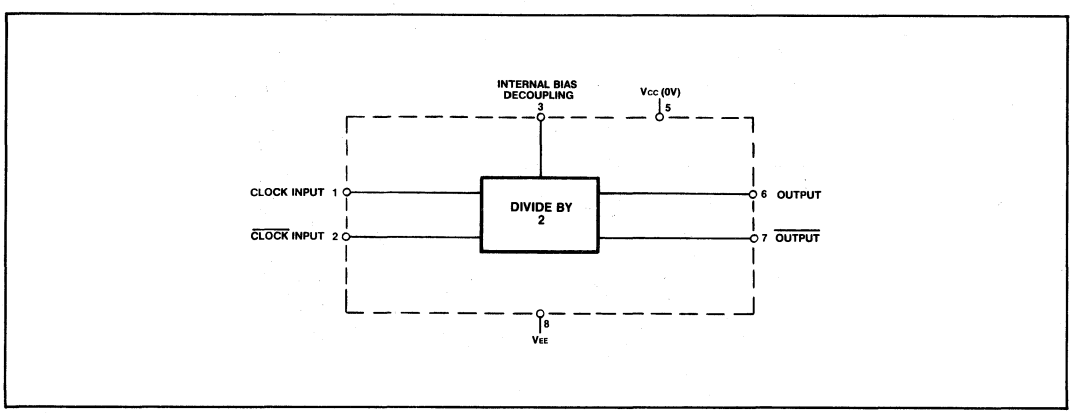


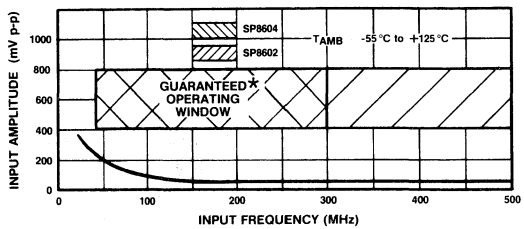
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} A Grade = -55°C to +125°C
B Grade = -30°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency (sinewave input)	f_{max}	500		MHz	SP8602	Input = 400-800mV p-p	
		300		MHz	SP8604		
Minimum frequency (sinewave input)	f_{min}		40	MHz	All	Input = 400-800mV p-p	
Power supply current	I_{EE}		18	mA	All	V_{EE} = 5.2V Outputs unloaded	
Output low voltage	V_{OL}	-1.8	-1.4	V	All	V_{EE} = -5.2V	Note 4
Output high voltage	V_{OH}	-0.85	-0.7	V	All	V_{EE} = -5.2V	Note 4
Minimum output swing	V_{OUT}	400		mV	All	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.34mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical characteristic of SP8602 and SP8604

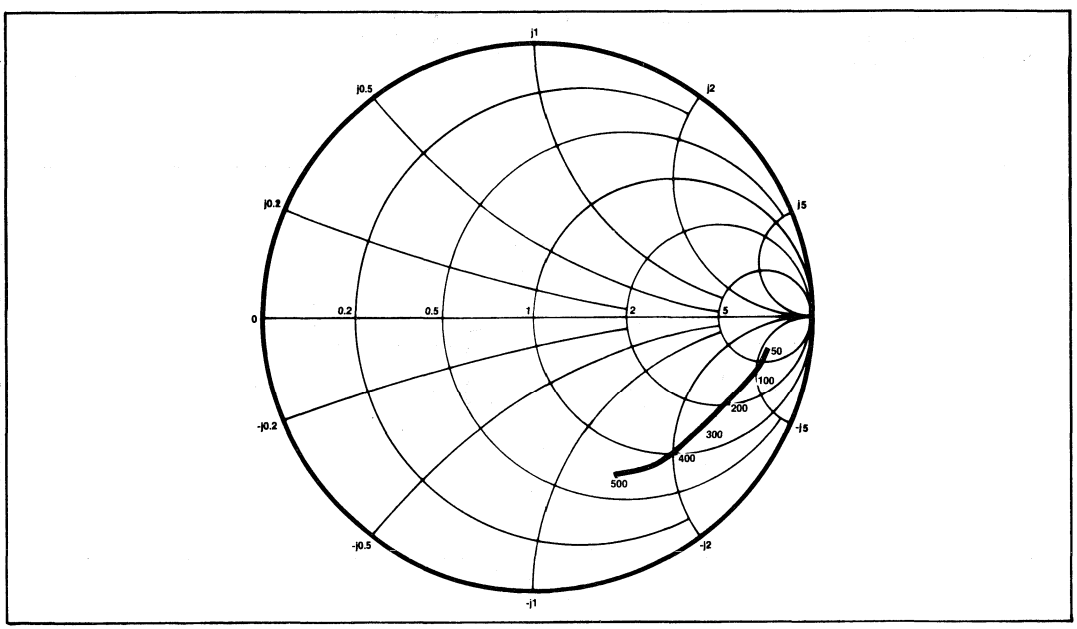


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

SP8605 1000MHz ÷ 2
SP8606 1300MHz ÷ 2

The SP8605 and SP8606 are emitter coupled logic dividers with ECL III compatible outputs. Specified from -55°C to +125°C (A Grade), these devices feature AC coupled inputs and 600mV p-p clock input sensitivity.

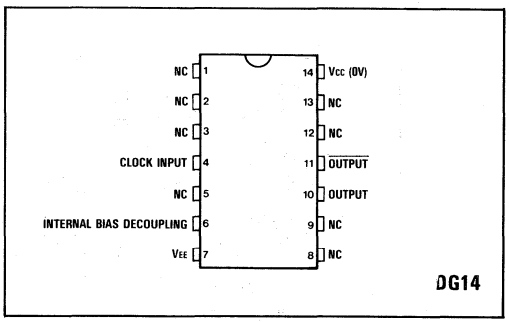


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 320mW
- Max. Input Frequency: 1300MHz (SP8606)
- Temperature Range:
  A Grade: -55°C to +110°C
  (125°C with suitable heat sink)
  B Grade: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8605 A DG
SP8605 B DG
SP8605 AA DG
SP8606 A DG
SP8606 B DG
SP8606 AA DG

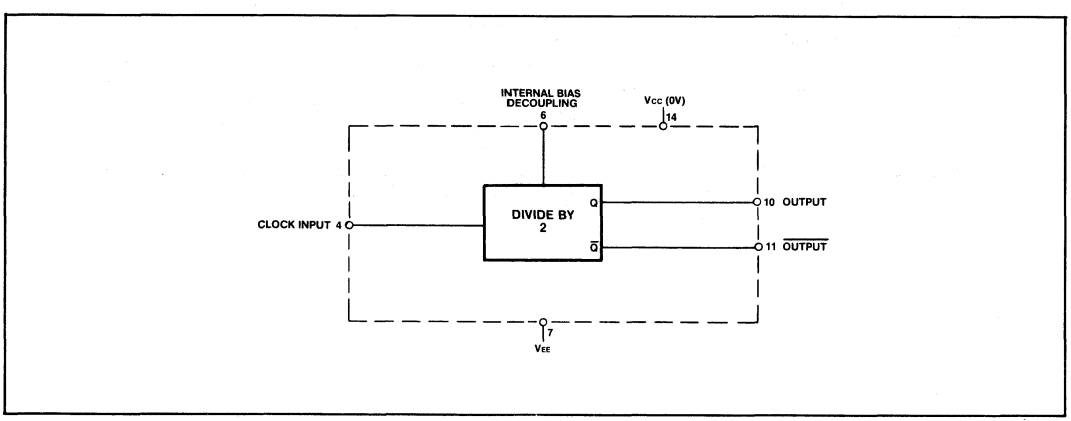


Fig.2 Functional diagram

OPERATING NOTES

1. The clock inputs (pins 1 and 2) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the unused input to V_{EE} (ie pin 1 or 2 to pin 8). This causes a drop in sensitivity of about 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k on each output. The outputs can be interfaced to ECL 10K by addition of a pulldown resistor of 1.5k from the outputs to V_{EE} to increase output voltage swing.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

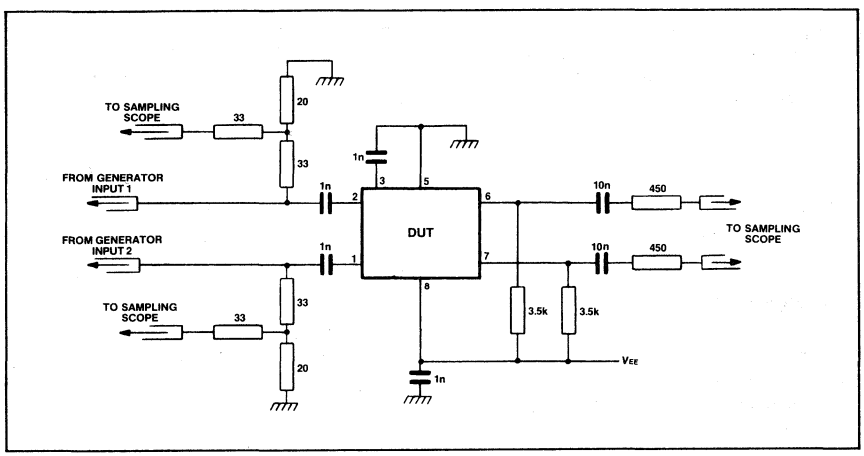


Fig.5 Test circuit

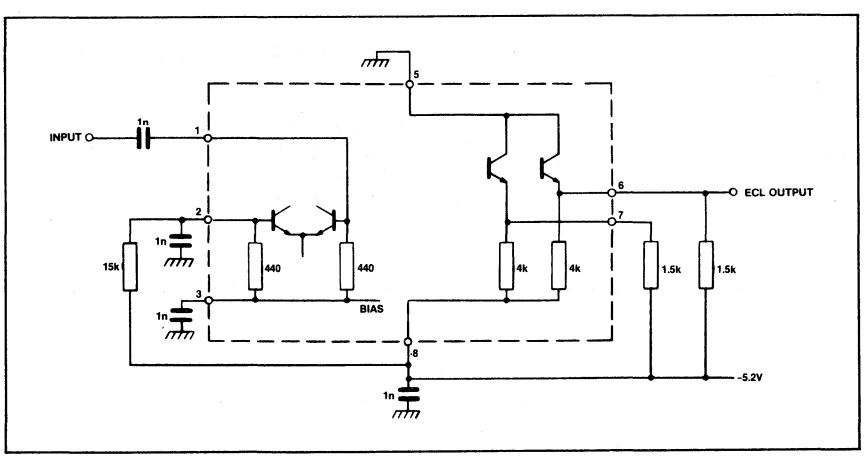


Fig.6 Typical application showing interfacing

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{case} = -55°C to +125°C (Note 2)
B Grade T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency (sinewave input)	f_{max}	1.0		GHz	SP8605A,B	Input = 400-1200mV p-p	Note 7
		1.3		GHz	SP8606A	Input = 800-1200mV p-p	Note 7
		1.3		GHz	SP8606B	Input = 400-1200mV p-p	Note 7
Minimum frequency (sinewave input)	f_{min}		150	MHz	All	Input = 600-1200mV p-p	Note 5
Current consumption	I_{EE}		100	mA	All	V_{EE} = -5.45V Outputs unloaded	Note 6
Output low voltage	V_{OL}	-1.92	-1.62	V	All	V_{EE} = -5.2V Outputs loaded with 430Ω(25°C)	
Output high voltage	V_{OH}	-0.93	-0.75	V	All	V_{EE} = -5.2V Outputs loaded with 430Ω(25°C)	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE} = -5.2V Outputs loaded with 430 ohms	Note 6

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The A grade devices must be used with a heat sink to maintain chip temperature below +150°C when operating in an ambient of +125°C.
3. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C but these are not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 25°C and +125°C only (+70°C for B grade).
6. Tested at 25°C only.
7. Tested at +125°C only (+70°C for B grade).

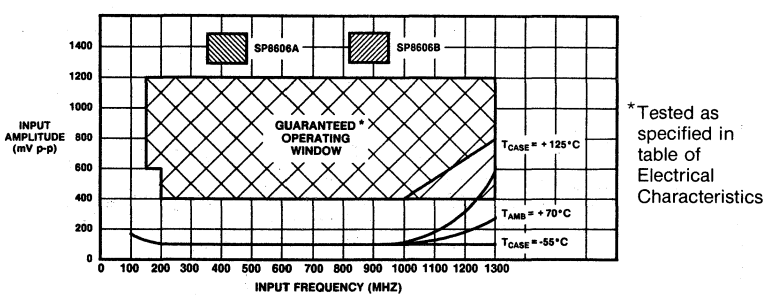


Fig.3 Typical characteristic of SP8606

THERMAL CHARACTERISTICS

θ_{JC} approximately 30°C/W
θ_{JA} approximately 110°C/W

OPERATING NOTES

1. The clock inputs (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the unused input to V_{EE} (ie pin 4 to pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8605/6 is a function of frequency. See Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 430 ohms is recommended. Interfacing to ECL III/10K is shown in Fig. 7.
6. These devices may be used with split supply lines and earth referenced input using the circuit shown in Fig. 6.
7. All components should be suitable for the frequency in use.

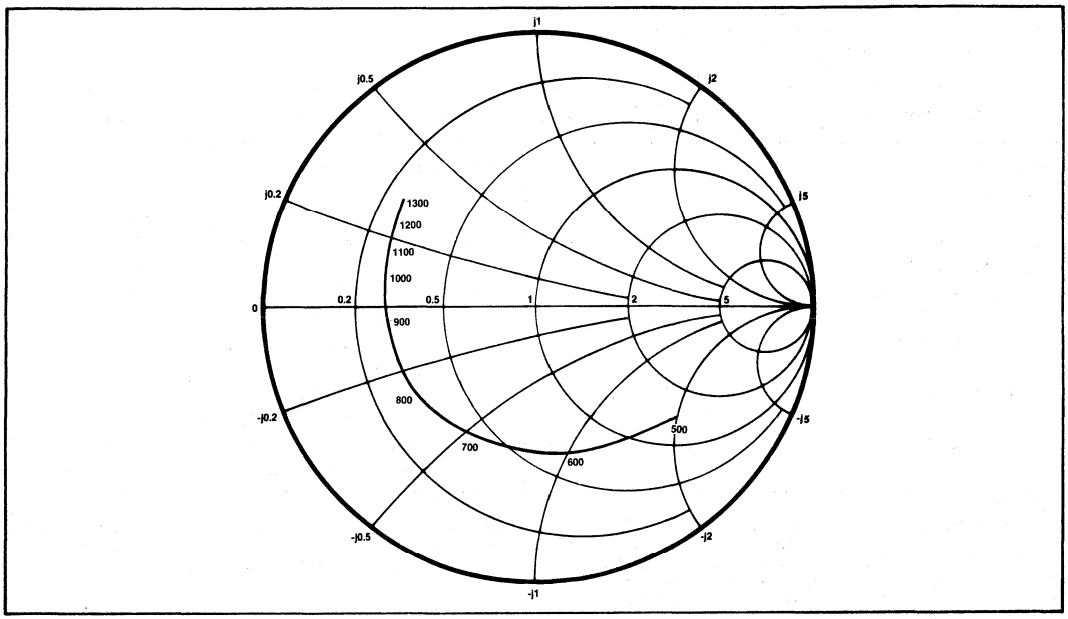


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

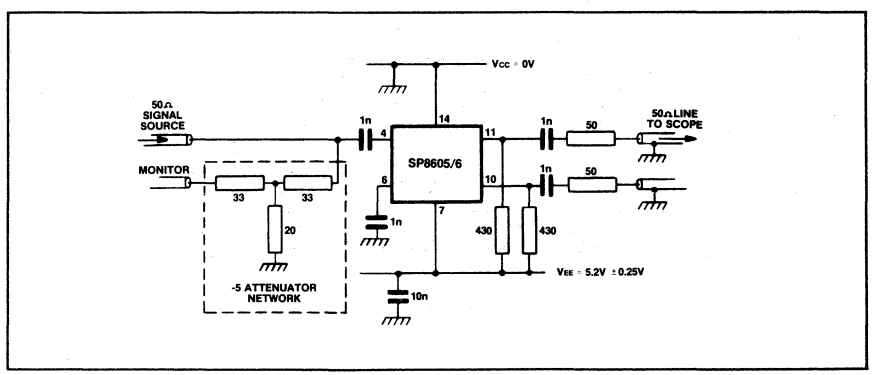


Fig.5 Toggle frequency test circuit

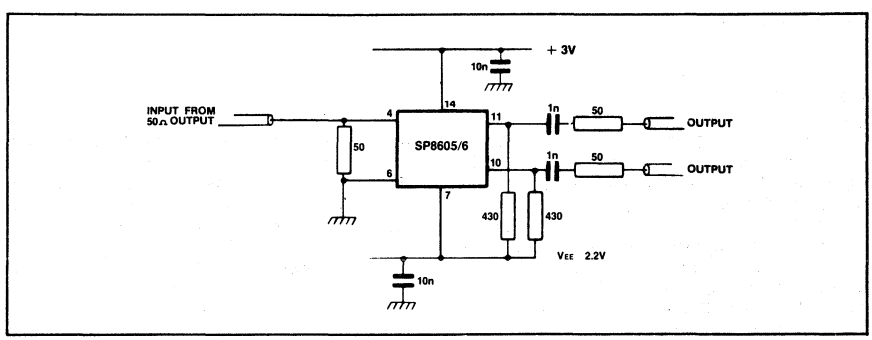


Fig.6 Circuit for using the input signal about ground potential

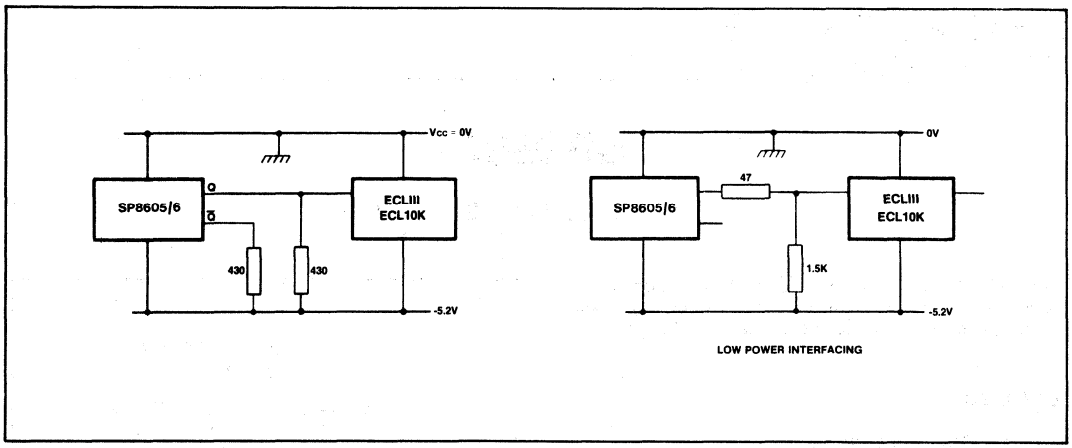


Fig.7 Interfacing SP8605/6 to ECL 10K and ECL III

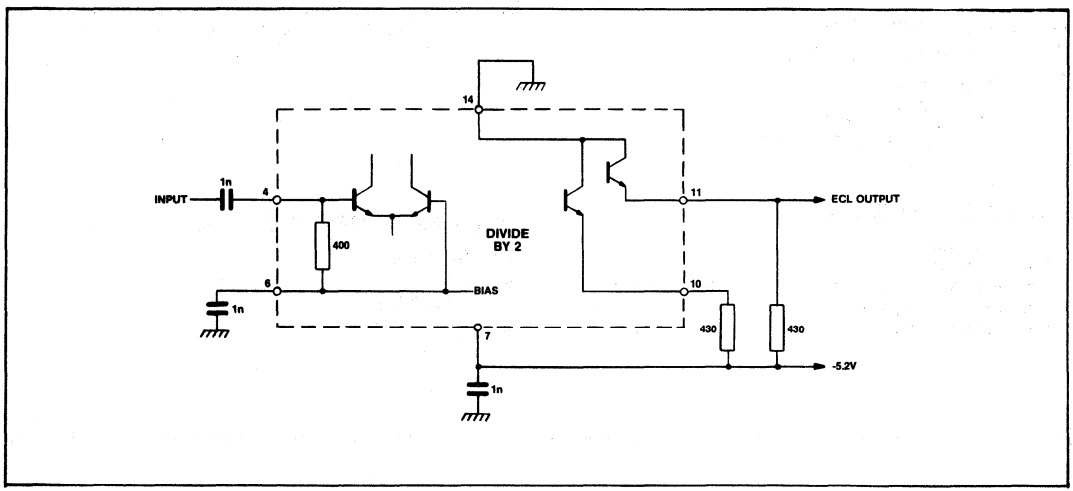


Fig.8 Typical application showing interfacing

SP8607

600MHz ÷ 2

The SP8607 is an emitter coupled logic divider which features ECL 10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

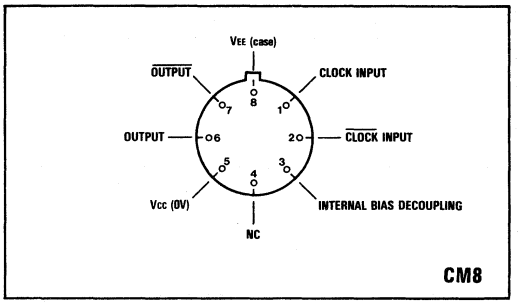


Fig.1 Pin connections - bottom view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 80mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8607 A CM
SP8607 B CM
SP8607 AB CM
SP8607 AC CM

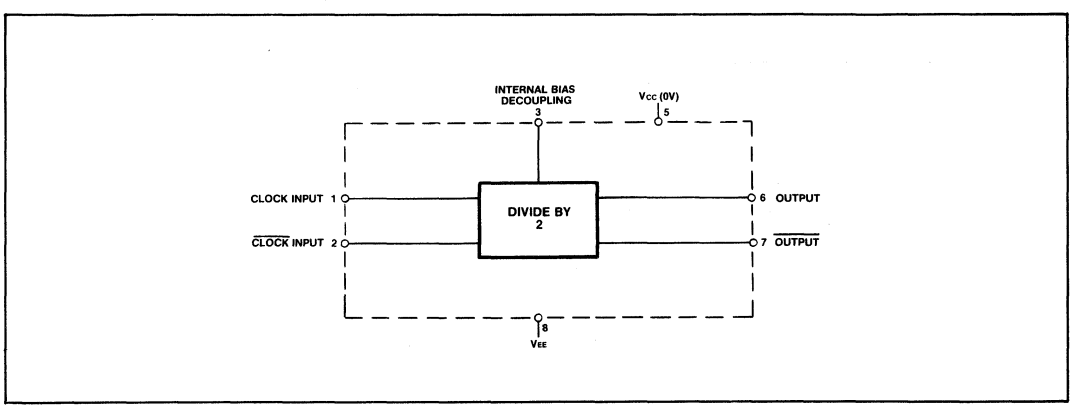


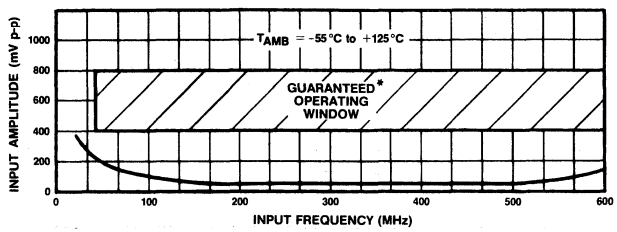
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} A Grade = -55°C to +125°C
B Grade = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		18	mA	V_{EE} = -5.2V Outputs unloaded	
Output low voltage	V_{OL}	-1.8	-1.4	V	V_{EE} = -5.2V	Note 4
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V	Note 4
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.34mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical characteristic of SP8607A

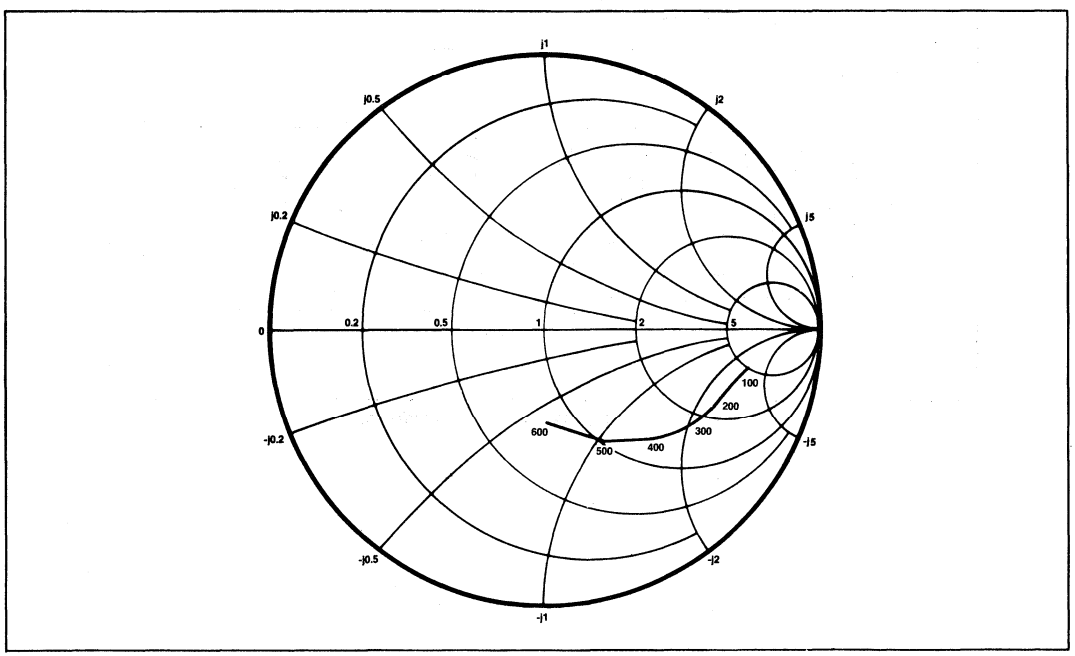


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 1 and 2) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the unused input to V_{EE} (ie pin 1 or 2 to pin 8). This causes a drop in sensitivity of about 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k on each output. The outputs can be interfaced to ECL 10K by addition of a pulldown resistor of 1.5k to the outputs to increase the output voltage swing.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

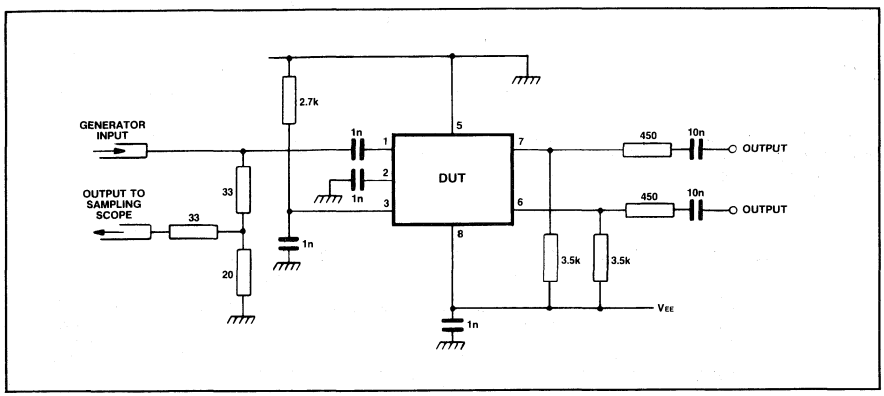


Fig.5 Test circuit

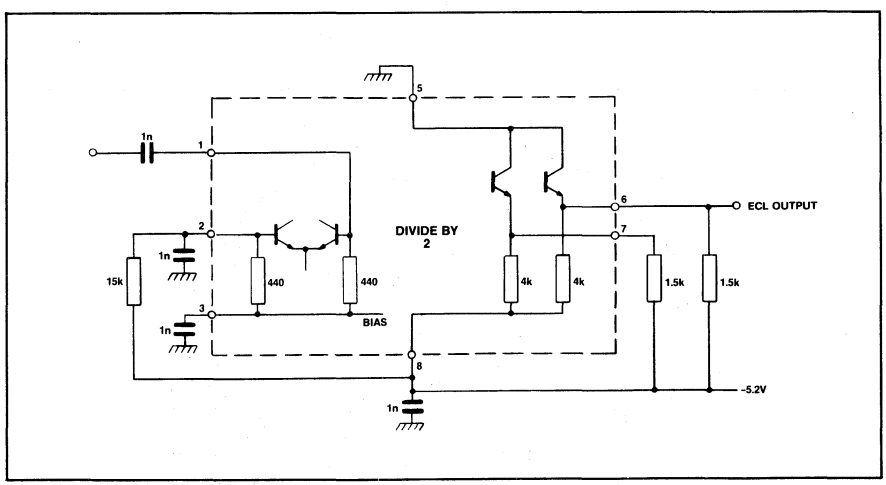


Fig.6 Typical application showing interfacing

SP8610 1000MHz ÷ 4
SP8611 1300/1500MHz ÷ 4

The SP8610/11 are asynchronous ECL divide by four circuits, with ECL compatible outputs which can also be used to drive 100 ohm lines. They feature input sensitivities of 600mV p-p (800mV p-p above 1300MHz).

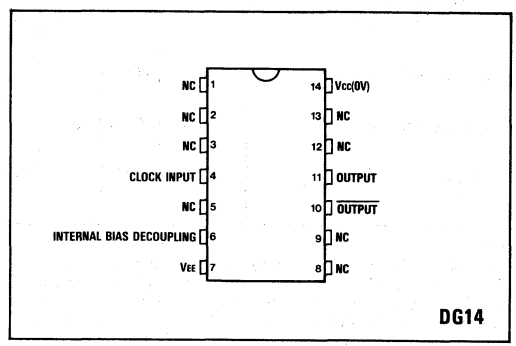


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Input (internal bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 380mW
- Max. Input Frequency: 1500MHz (SP8611B)
- Temperature Range:

  A Grade: -55°C to +110°C
  (+125°C with suitable heatsink)
  B Grade: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8610 A DG
SP8610 B DG
SP8610 AB DG
SP8610 AA DG
SP8611 A DG
SP8611 B DG
SP8611 AB DG
SP8611 AA DG

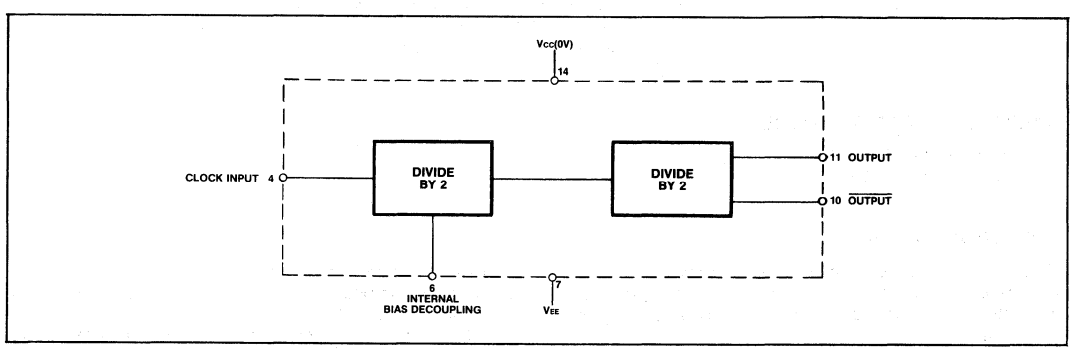


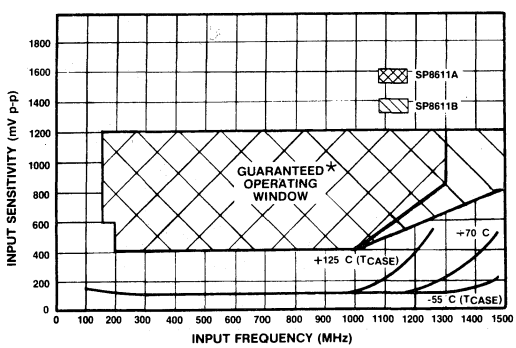
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{CASE} (A grade) = -55°C to +125°C (Note 2)
T_{amb} (B grade) = 0°C to +70°C

Characteristic	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Note
Maximum frequency	f_{max}	1.0		GHz	SP8610A,B	Input = 400-1200mV	Note 5
		1.3		GHz	SP8611A	Input = 800-1200mV	Note 7
		1.5		GHz	SP8611B	Input = 800-1200mV	Note 7
Minimum frequency	f_{min}		150	MHz	All	Input = 600-1200mV	Note 5
Current consumption	I_{EE}		100	mA	All	V_{EE} = -5.45V Outputs unloaded	Note 6
Output low voltage	V_{OL}	-1.92	-1.62	V	All	V_{EE} = -5.2V outputs loaded with 430Ω(25° C)	
Output high voltage	V_{OH}	-0.93	-0.75	V	All	V_{EE} = -5.2V outputs loaded with 430Ω(25° C)	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE} = -5.2V outputs loaded with 430Ω	Note 6

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The A grade devices must be used with a heat sink to maintain chip temperature below +150°C when operating in an ambient of +125°C.
3. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C but these are not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 25°C and +125°C only (+70°C for B grade).
6. Tested at 25°C only.
7. Tested at +125°C only (+70°C for B grade).



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics

THERMAL CHARACTERISTICS

θ_{JC} approximately 30°C/W
θ_{JA} approximately 110°C/W

OPERATING NOTES

1. The clock input (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. Pin 4 to Pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8610/11 is a function of frequency. See Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 430 ohms is recommended. Interfacing to ECL III/10K is shown in Fig. 7.
6. These devices may be used with split supply lines and ground referenced input by means of the circuit of Fig. 6.

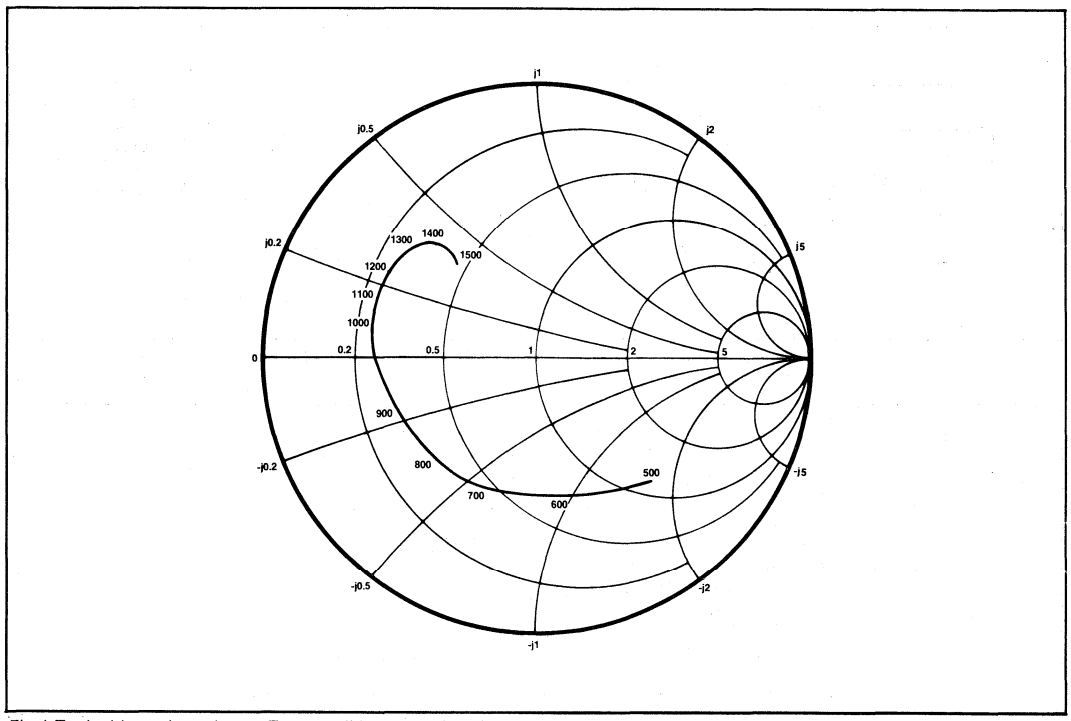


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

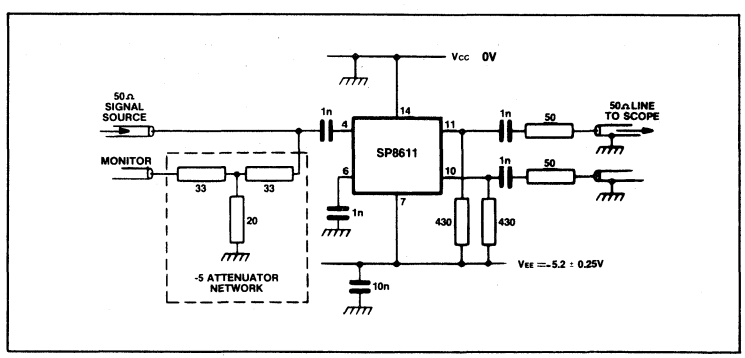


Fig.5 Toggle frequency test circuit

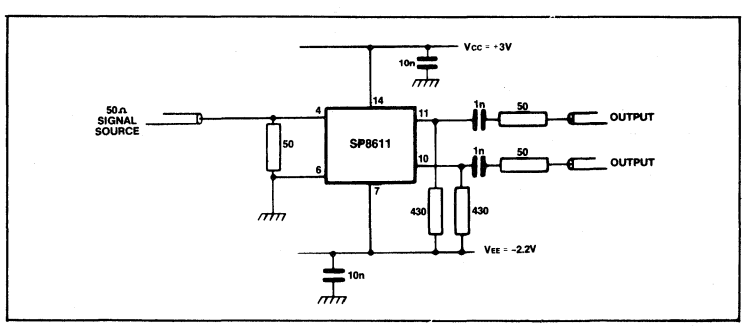


Fig.6 Circuit for using the input signal about earth potential

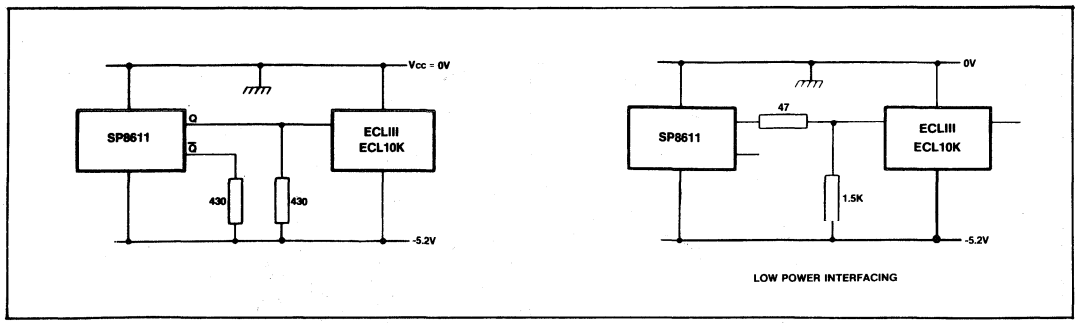


Fig.7 Interfacing SP8611 series to ECL 10K and ECL III

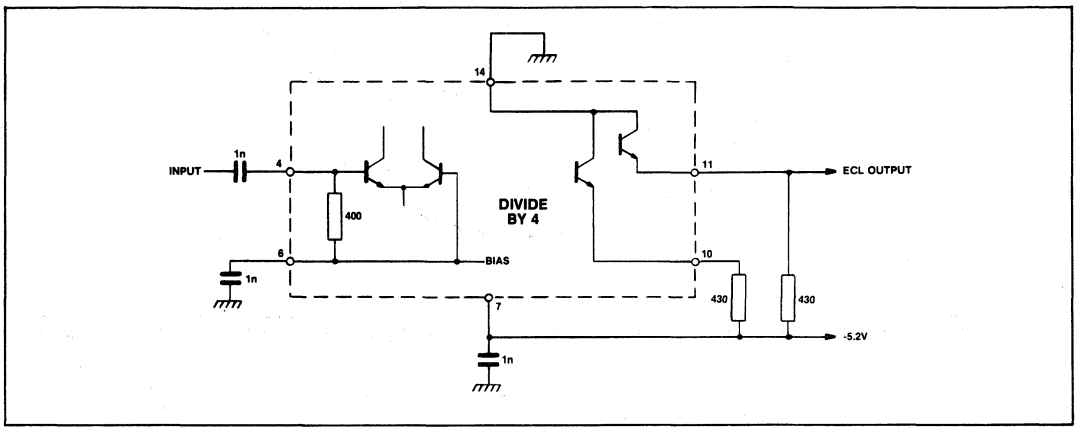


Fig.8 Typical application showing interfacing

SP8620

400MHz ÷ 5

The SP8620 is an asynchronous emitter coupled logic counter which provides an ECL compatible output when an external pulldown resistor is added. It requires an AC coupled input of 600mV p-p.

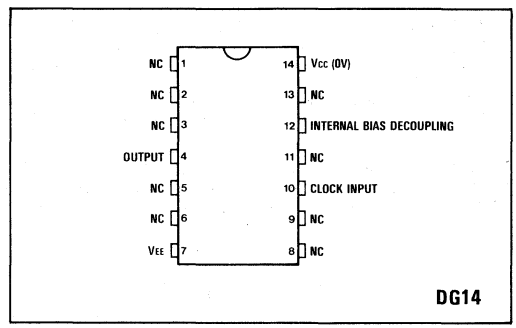


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 285mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8620 A DG
SP8620 B DG
SP8620 AB DG
SP8620 AC DG

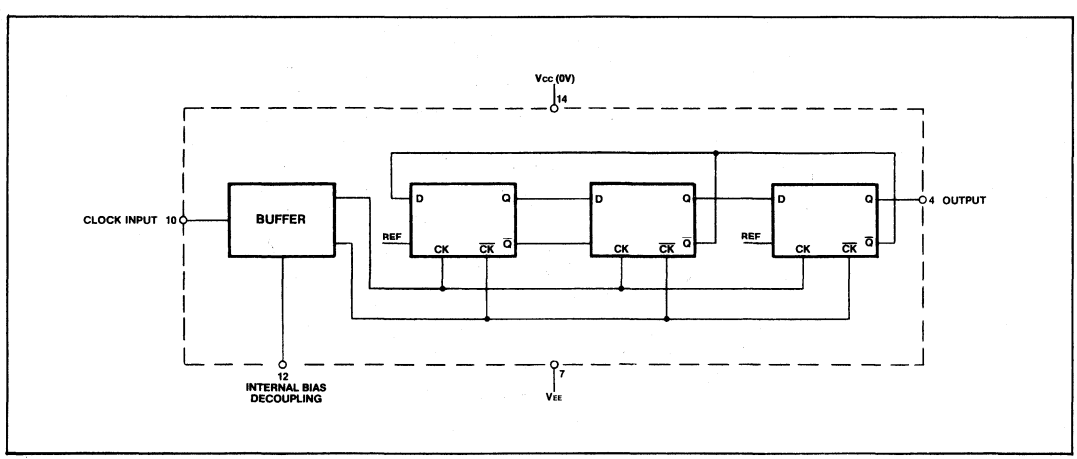


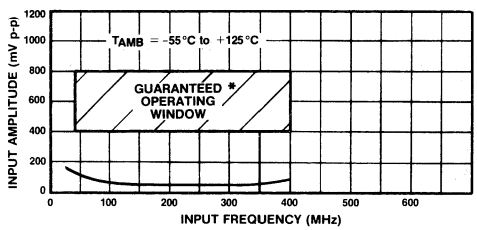
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Conditions	Note
Maximum frequency (sinewave input)	f_{max}	400		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		55	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8620A

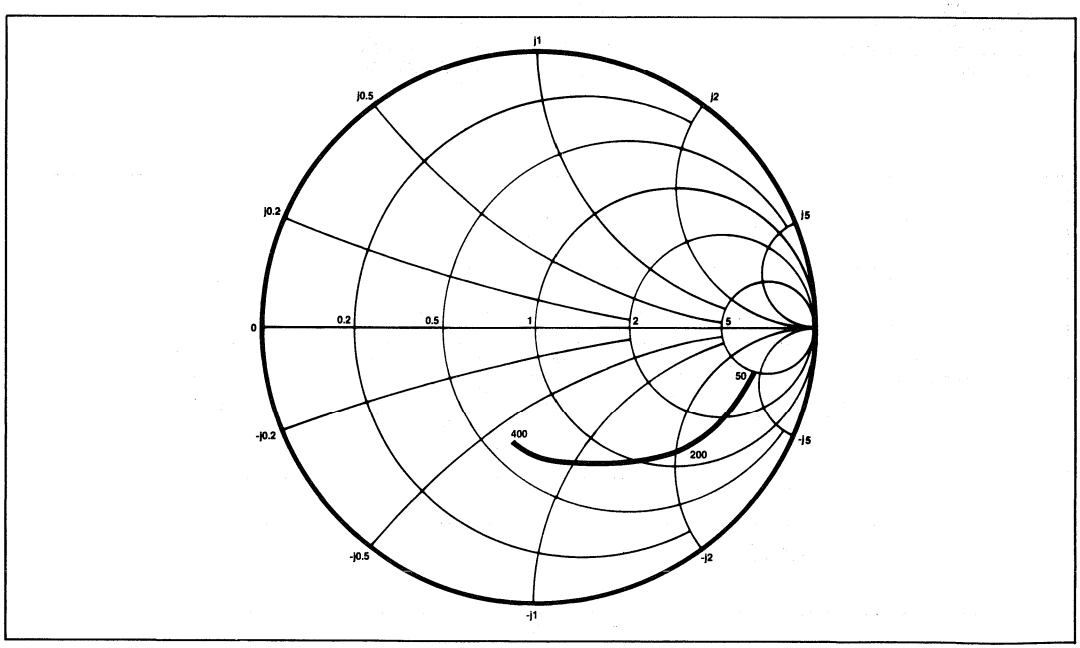


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. The circuit will operate down to DC but slew rate must be better than 100V/μs.
3. The outputs are compatible with ECL II. There is an internal load of 3k at the output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
4. Input impedance is a function of frequency. See Fig.4.
5. All components should be suitable for the frequency in use.

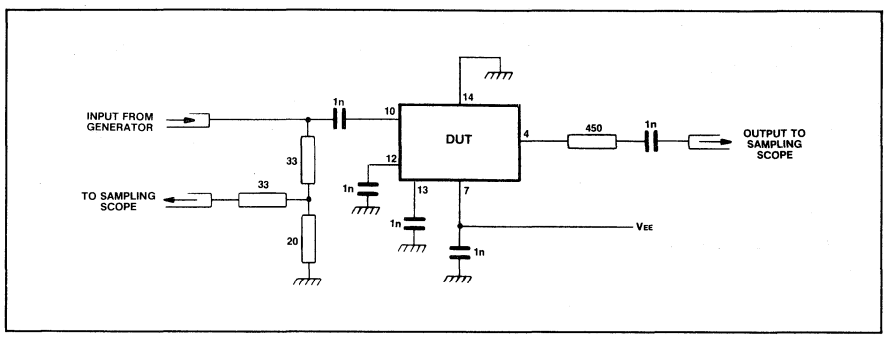


Fig.5 Test circuit

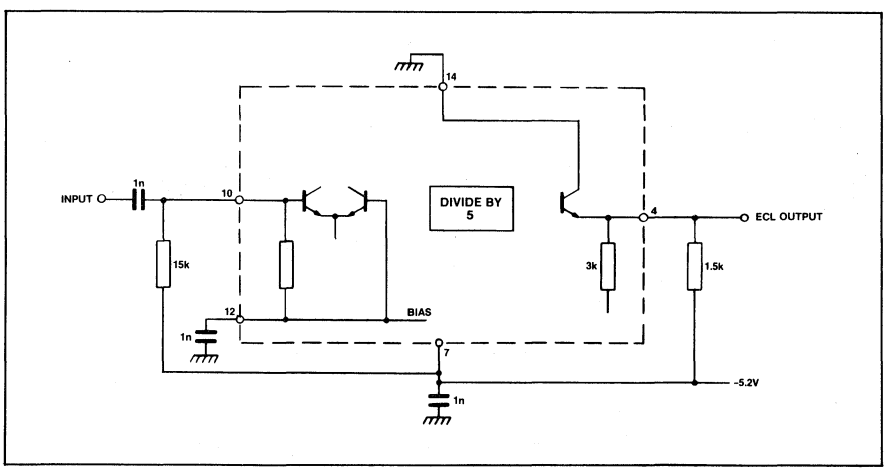


Fig.6 Typical application showing interfacing

SP8629

150MHz ÷ 100

The SP8629 is an ECL counter which provides a TTL compatible output, high input sensitivity and low power consumption. Pin compatible with DM8629, it features a much lower power consumption.

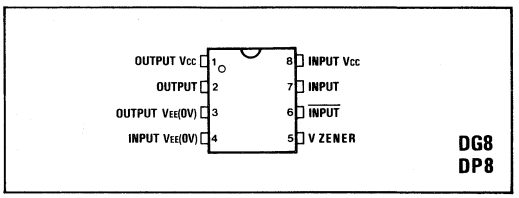


Fig.1 Pin connections - top view

FEATURES

- TTL/CMOS Compatible Output
- High Input Sensitivity
- Ideal Frequency Counter Prescaler
- On Chip Zener Diode

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 170mW
- Temperature Range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pins 1 and 8)	8V
Output current	40mA
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8629 DG
SP8629 DP

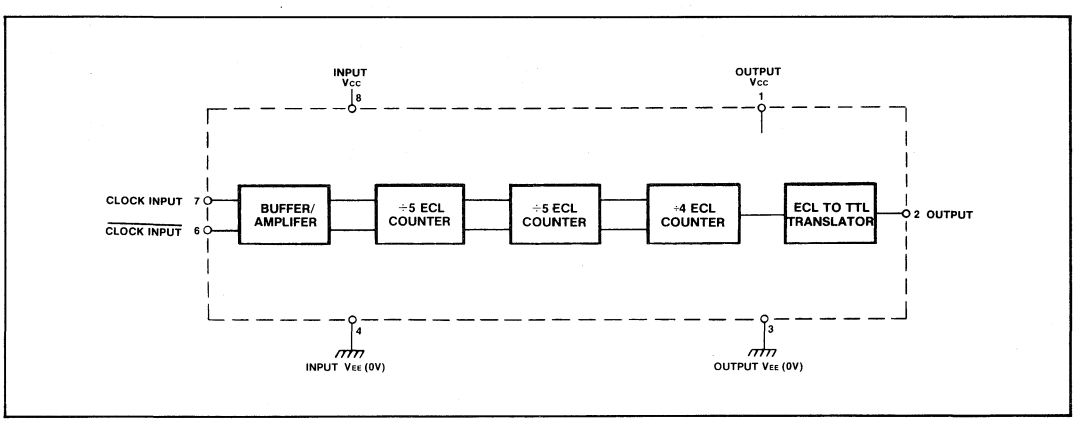


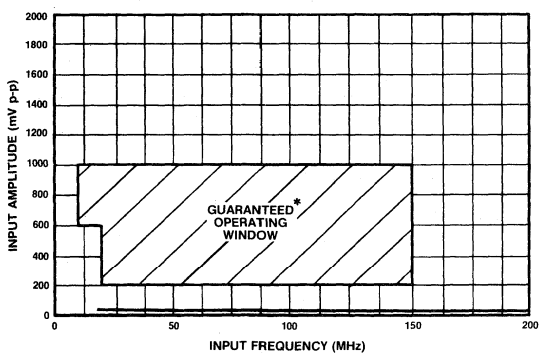
Fig.2 SP8629 logic diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.52V V_{EE} = 0V
Temperature: T_{amb} -40°C to +85°C

Characteristics	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum toggle frequency sinewave input	f_{max}	150		MHz	Input = 200-1000mV p-p
Minimum toggle frequency sinewave input	f_{min}		10	MHz	Input — 600-1000mV p-p
Power supply current	I_{EE}		45	mA	
Output high voltage	V_{OH}	2.4		V	V_{CC} = 4.68V I_{OH} = -400µA
Output high voltage	V_{OH}	2.0		V	V_{CC} = 4.68V I_{OH} = -1.6mA
Output low voltage	V_{OL}		0.5	V	V_{CC} = 5.72V I_{OL} = 8mA
Output short circuit current	I_{OS}	-10	-40	mA	V_{CC} = 5.72V
Internal zener voltage	V_Z	5.85	6.65	V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. All characteristics above are tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8629

OPERATING NOTES

1. Two V_{EE} and two V_{CC} connections are provided, separating the ECL stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two V_{EE} pins to a good ground plane and the V_{CC} pins to a wide V_{CC} bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimise stray inductance.
2. The signal source is usually capacitively coupled to the input as shown in Fig. 6. In the single-ended mode a capacitor of 0.01µF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be increased at lower frequencies. If the input is likely to be interrupted, it may be desirable to connect a 100k resistor between an input and ground.
3. In the single ended mode it is preferable to connect the resistor to the unused input. The addition of the 100k resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions.
4. The input waveform will normally be sinusoidal but below 10MHz correct operation depends on the slew rate of the input signal. A slew rate of 50V/µs will enable the device to operate down to DC. The device will operate with a TTL input signal as shown in Fig. 7 and is DC coupled to the input.

The device can be used in phase locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more useable level. A digital frequency display system can also be derived separately or in conjunction with a phase locked loop, and it can extend the useful range of many inexpensive frequency counters to, typically, 200MHz.

5. The on-chip Zener diode allows a simple stabilised power supply to be constructed with the addition of a few extra external components, as shown in Fig. 8, to the SP8629.
6. The INPUT is positive edge triggered while the $\overline{\text{INPUT}}$ triggers on the negative edge.

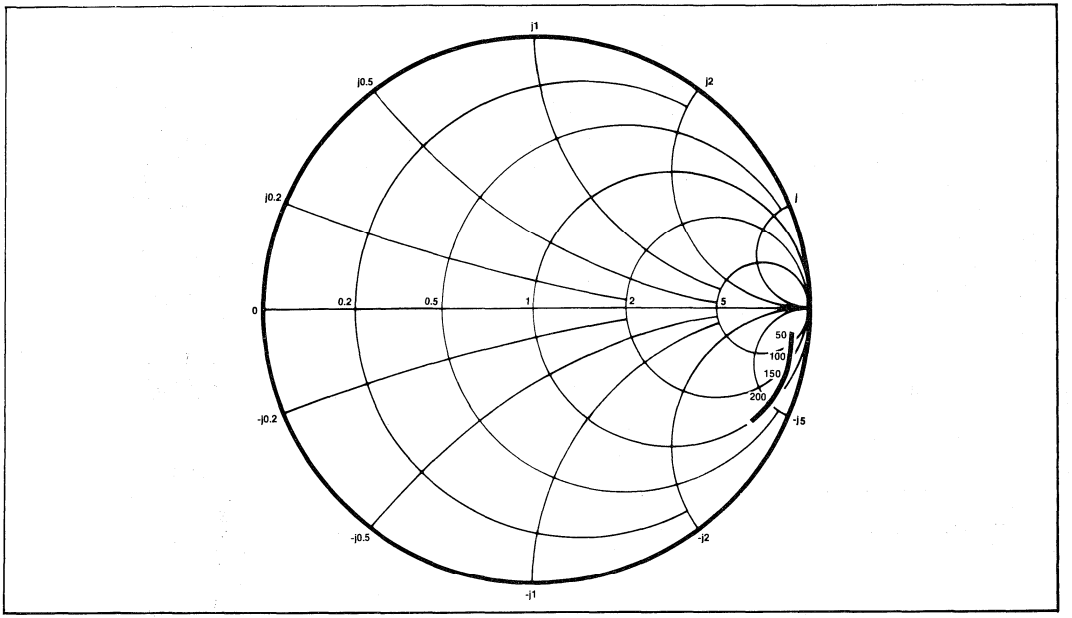


Fig.4 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C. Frequencies in MHz, impedances normalised to 50 ohms.

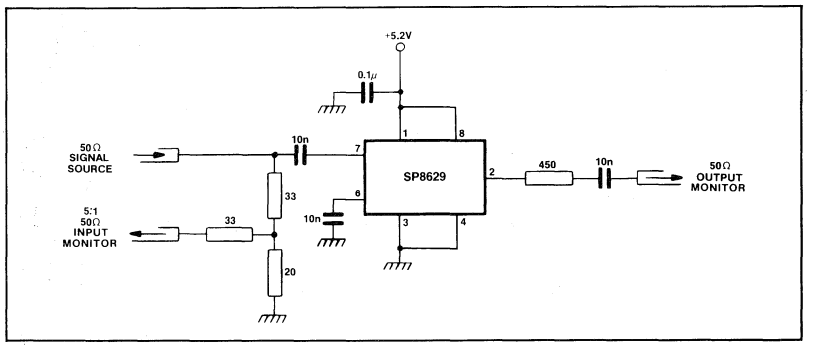


Fig.5 Test circuit

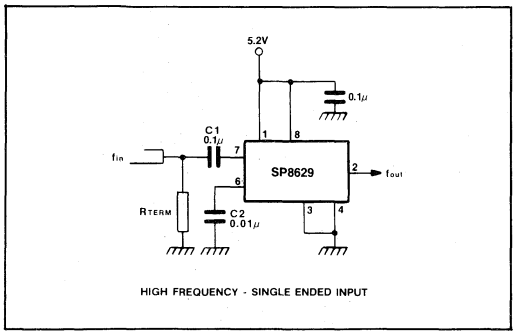


Fig.6 High frequency, single-ended input

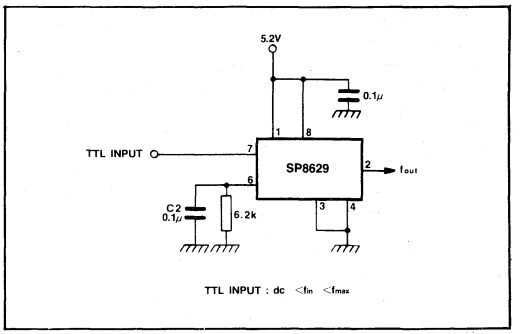


Fig.7 TTL inut (DC <f_{in} <f_{max})

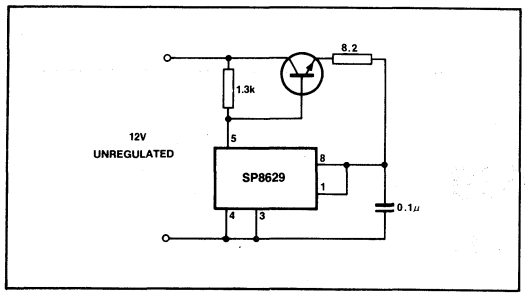


Fig.8 Use of on-chip zener diode for operation from unregulated supply

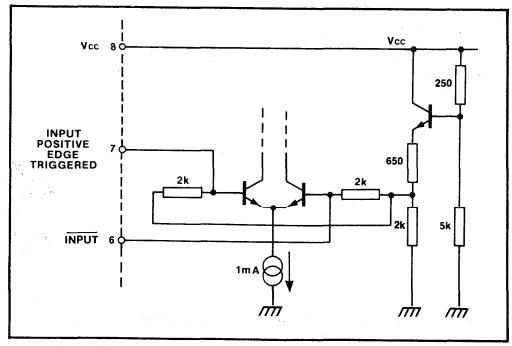


Fig.9 Input circuit diagram

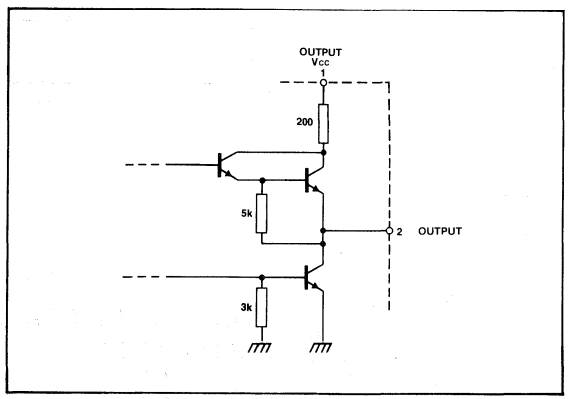


Fig.10 Output circuit diagram

SP8630

600MHz ÷ 10

The SP8630 is an asynchronous emitter coupled logic counter which provides an ECL compatible output when used with an external pulldown resistor. It requires an AC coupled input of 600mV p-p.

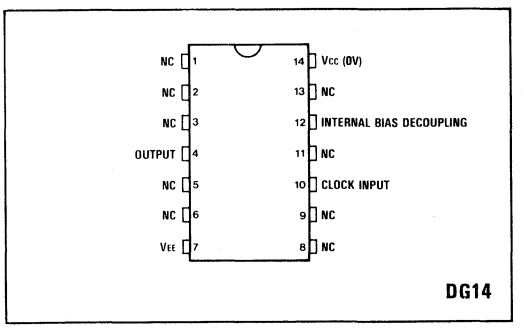


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 350mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	15mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8630 A DG
SP8630 B DG
SP8630 AB DG
SP8630 AC DG

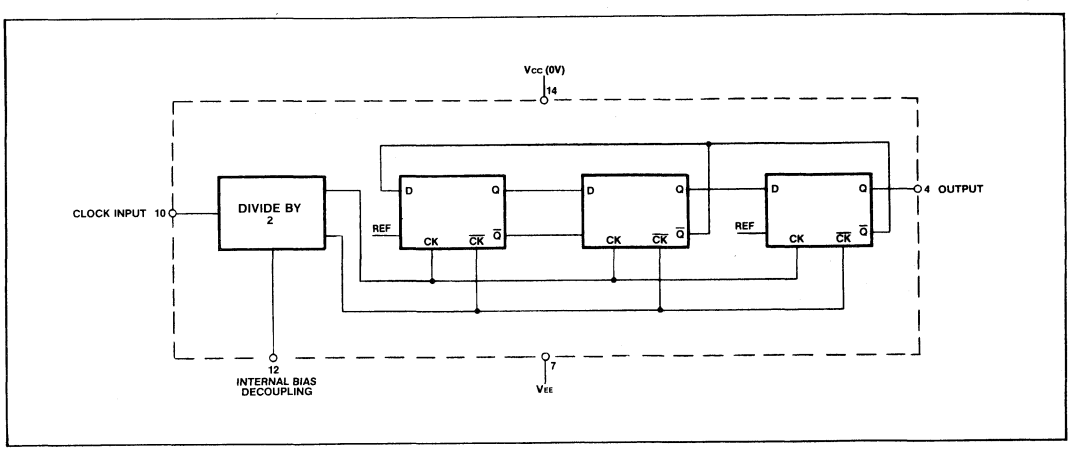


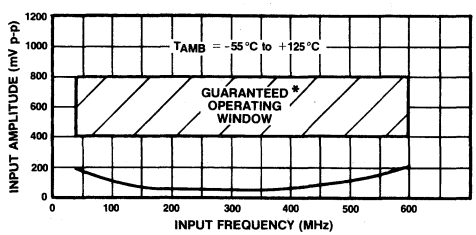
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Note
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		70	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8630A

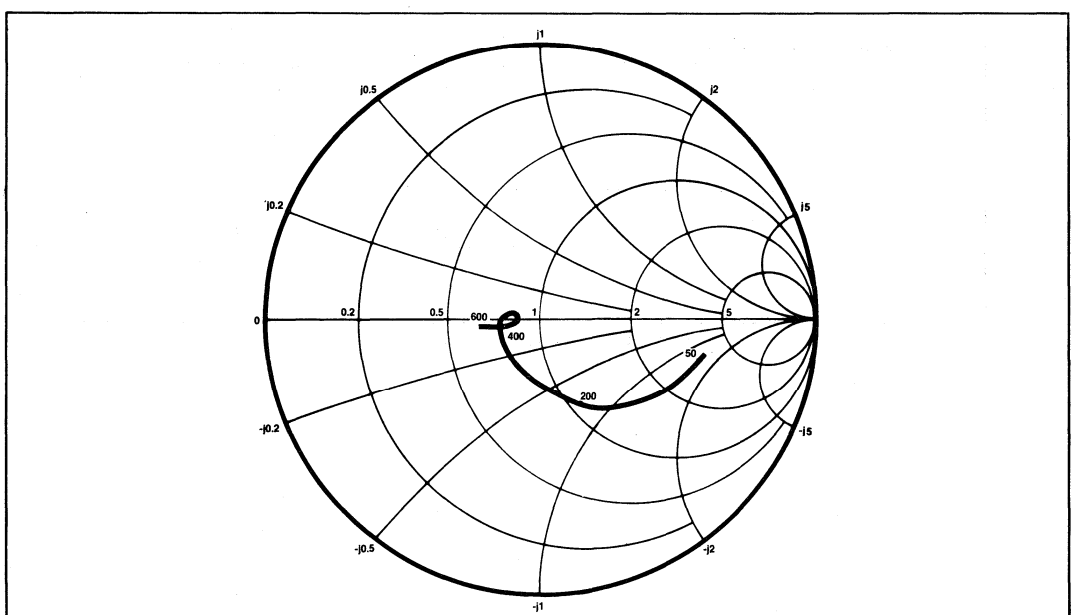


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. The circuit will operate down to DC but slew rate must be better than 100V/μs.
3. The outputs are compatible with ECL II. There is an internal load of 3k at output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
4. Input impedance is a function of frequency. See Fig.4.
5. All components should be suitable for the frequency in use.

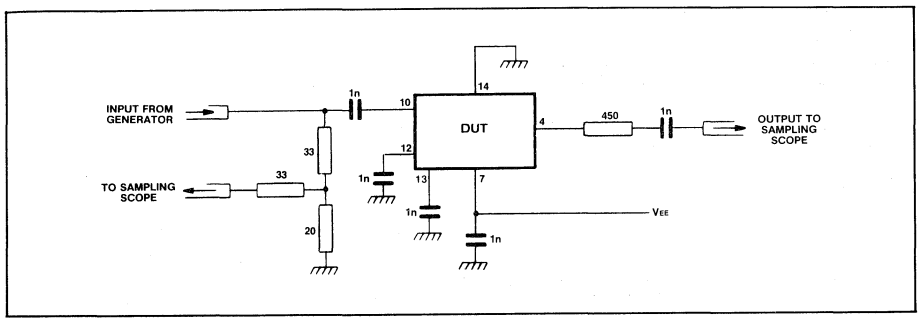


Fig.5 Test circuit

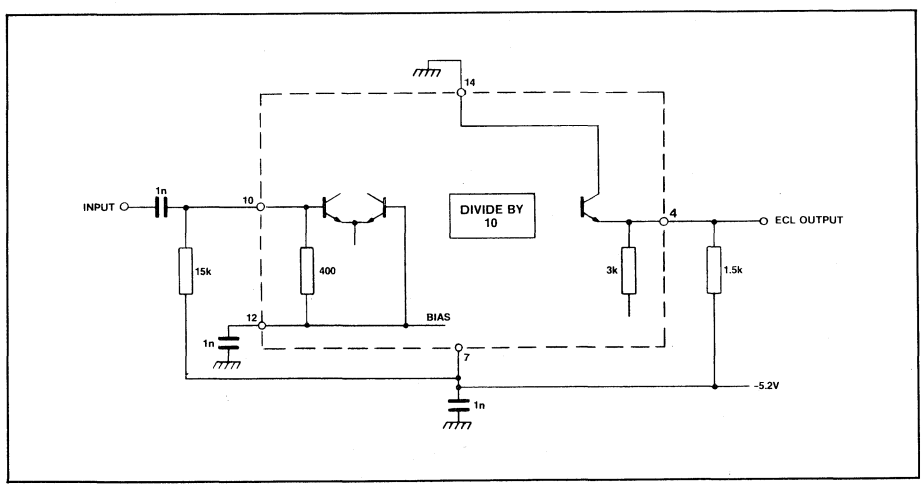


Fig.6 Typical application showing interfacing

SP8634 SP8635 SP8637

700/600/400MHz ÷ 10 (BCD OUTPUTS)

The SP8634/5 and 7 are ECL decade counters with TTL compatible BCD outputs. They require an AC coupled input of 600mV p-p and have an ECL 10K compatible inhibit input which inhibits the device when in the high state. Both ECL and TTL 'carry' outputs are provided and there is a TTL reset.

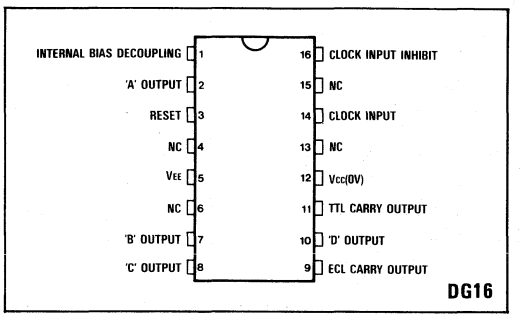


Fig.1 Pin connections - top view

FEATURES

- BCD Outputs TTL Compatible
- Reset Input TTL Compatible
- AC Coupled Input (Internal Bias)
- TTL and ECL Compatible Carry Outputs
- Clock Inhibit Input ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.2V
- Power Consumption: 400mW
- Temperature Range: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
BCD outputs voltage	V_{EE} +11V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8634 B DG
SP8635 B DG
SP8637 B DG

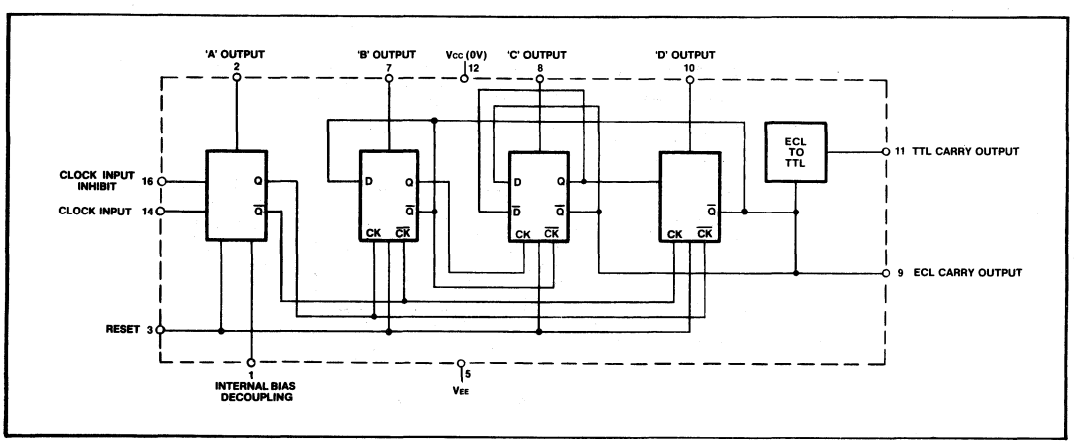


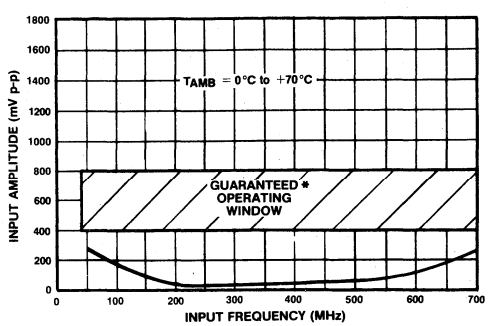
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum frequency sinewave input	f_{max}	700		MHz	SP8634B	Input = 400-800mV p-p	Note 5
		600		MHz	SP8635B		
		400		MHz	SP8637B		
Minimum frequency sinewave input	f_{min}		40	MHz	All	Input = 400-800mV p-p	Note 7
Power supply current	I_{EE}		90	mA	All	V_{EE} = -5.2V	Note 6
Clock inhibit high voltage	V_{INH}	-0.96		V	All	V_{EE} = -5.2V (25°C)	
Clock inhibit low voltage	V_{INL}		-1.65	V	All	V_{EE} = -5.2V (25°C)	
TTL output high voltage (pin 2,7,8,10)	V_{OH}	2.4		V	All	10kΩ from TTL output too +5V	Note 6
TTL output low voltage (pin 2,7,8,10)	V_{OL}		0.4	V	All	10kΩ from TTL output to +5V	Note 6
TTL output voltage (pin 11)	V_{OH}	2.4		V	All	5kΩ from TTL output to +5V	Note 6
TTL output low voltage (pin 11)	V_{OL}		0.4	V	All	5kΩ from TTL output to +5V	Note 6
ECL output high voltage (pin 9)	V_{OH}	-0.9	-0.7	V	All	V_{EE} = -5.2V (25°C)	
ECL output low voltage (pin 9)	V_{OL}	-1.8	-1.5	V	All	V_{EE} = -5.2V (25°C)	
Edge speed for correct operation at maximum frequency	t_E		2.5	ns	All	10% to 90%	Note 7
Reset on time for correct operation	t_{ON}	100		ns	All		Note 7
Reset input high voltage	V_{INH}	2.4		V	All		Note 6
Reset input low voltage	V_{INL}		0.5	V	All		Note 6

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} (ECL) = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
3. The temperature coefficient of inhibit threshold voltage = +0.24mV/°C but this is not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 0°C and +70°C only.
6. Tested at +25°C only.
7. Guaranteed but not tested.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8634

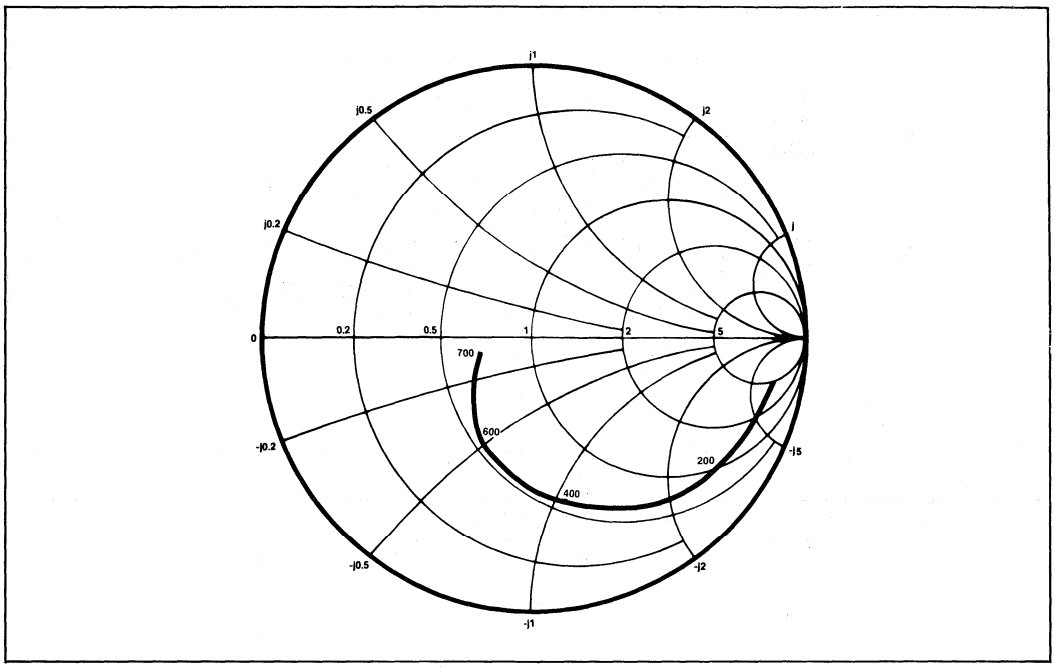


Fig.4 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C. Frequencies in MHz, impedances normalised to 50 ohms.

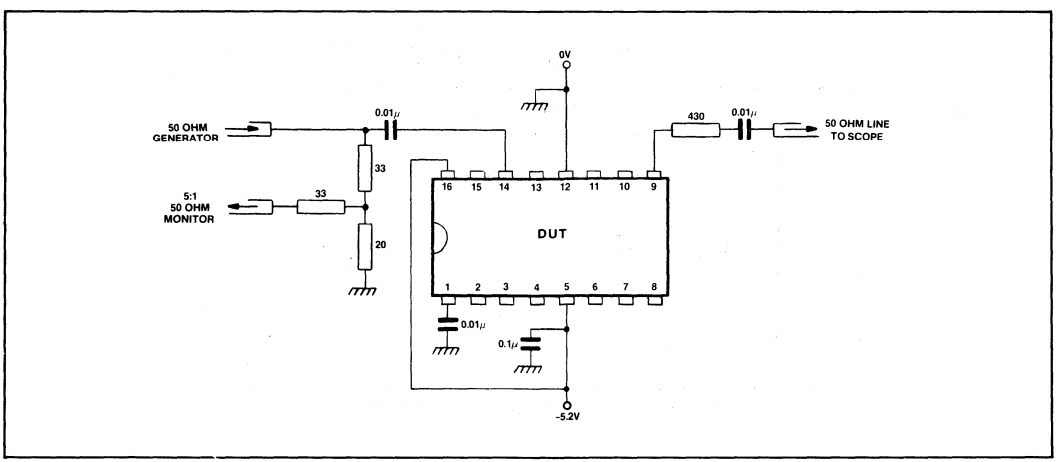


Fig.5 SP8634/5/7 high frequency test circuit

OPERATING NOTES

1. The clock input (pin 14) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 1, to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 68k resistor between the clock input, pin 14, and the negative supply (pin 5).
3. The device will operate down to DC but the input slew rate must be better than 100V/μs.
4. The Carry O/P is ECL II compatible but can be interfaced ECL III/10K by the inclusion of two resistors. See Fig. 7.
5. The clock inhibit is compatible with ECL III/10K throughout the temperature range.
6. The output (pins 2, 7, 8, 10 and 11) are current sources and can be made TTL compatible by addition of 10k and 5k (pin 11) to +5V. See Fig.6. This gives a fan-out of 1. This can be increased by buffering the output with a PNP emitter follower. See Fig.8.
7. The device is clocked on the positive transition of the clock input on pin 14, provided that the clock inhibit input (pin 16) is in the low state. It is important to note that the positive transition of clock inhibit must occur while the clock is in the high state to avoid spurious counting.

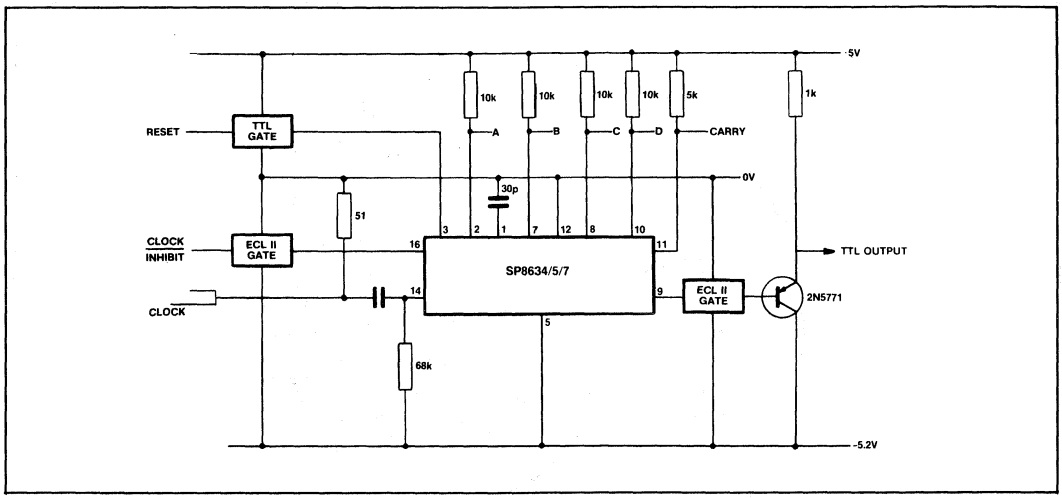


Fig.6 Typical application configuration

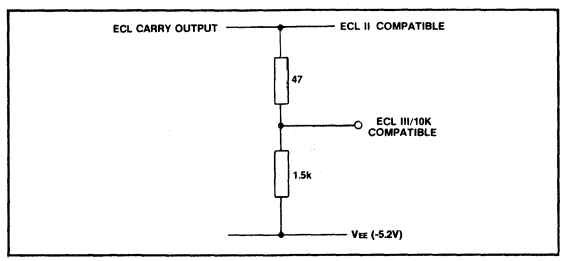


Fig.7 ECL III/10K interfacing

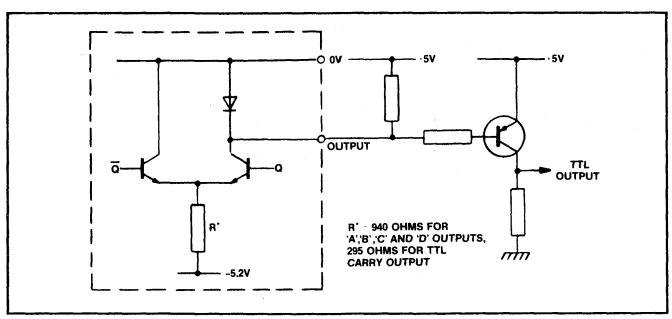


Fig.8 TTL output buffering for increased fan-out

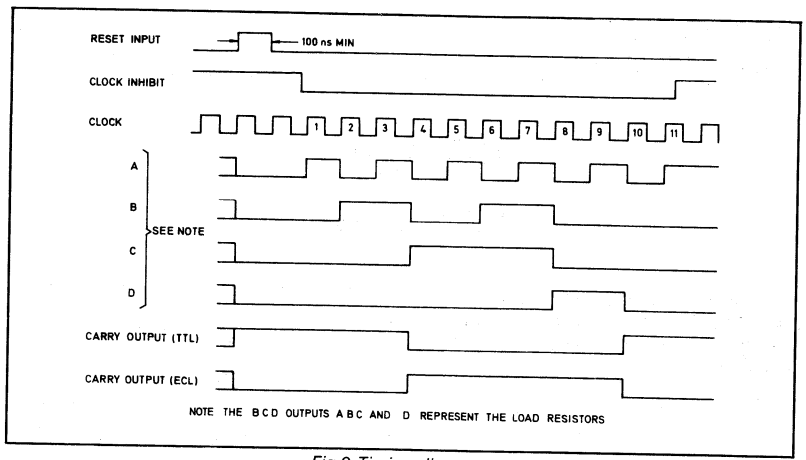


Fig.9 Timing diagram

SP8650

600MHz ÷ 16

The SP8650 is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs when external pulldown resistors are added. It requires an AC coupled input of 600mV p-p.

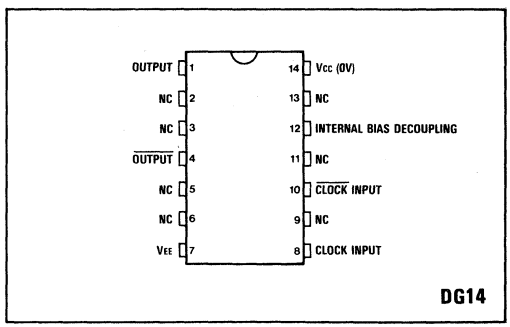


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 300mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8650 A DG
SP8650 B DG
SP8650 AB DG
SP8650 AC DG

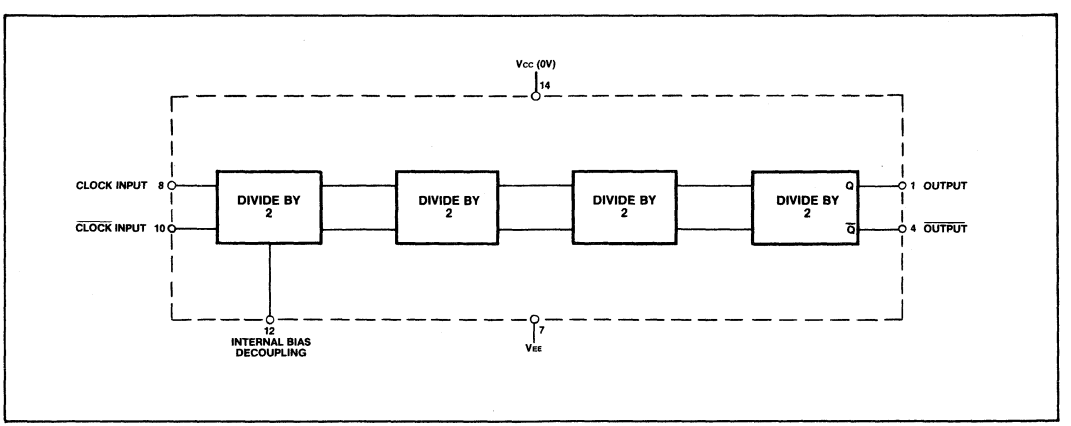


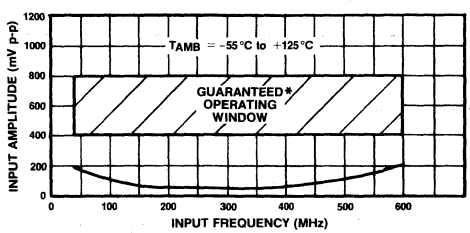
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		60	mA		Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25° only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8650A

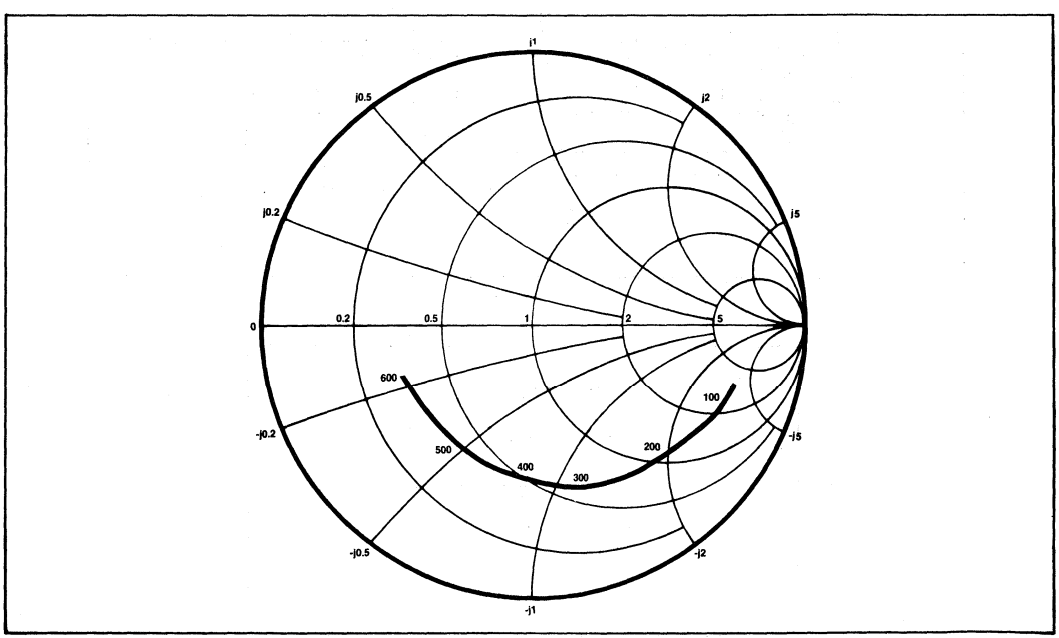


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 8 and 10) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from one of the inputs to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k at each output. The output can be interfaced to ECL 10K by addition of two resistors.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

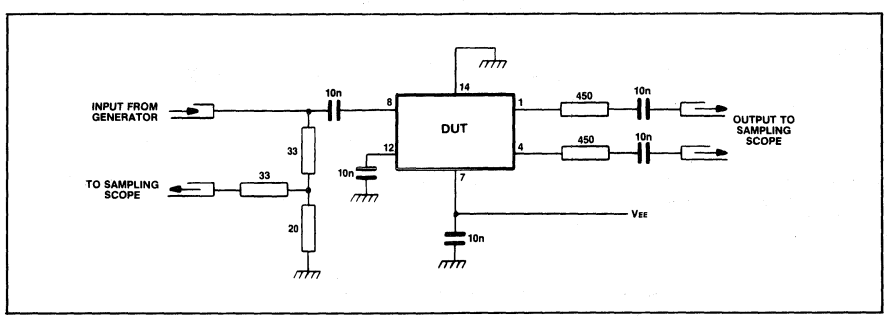


Fig.5 Test circuit

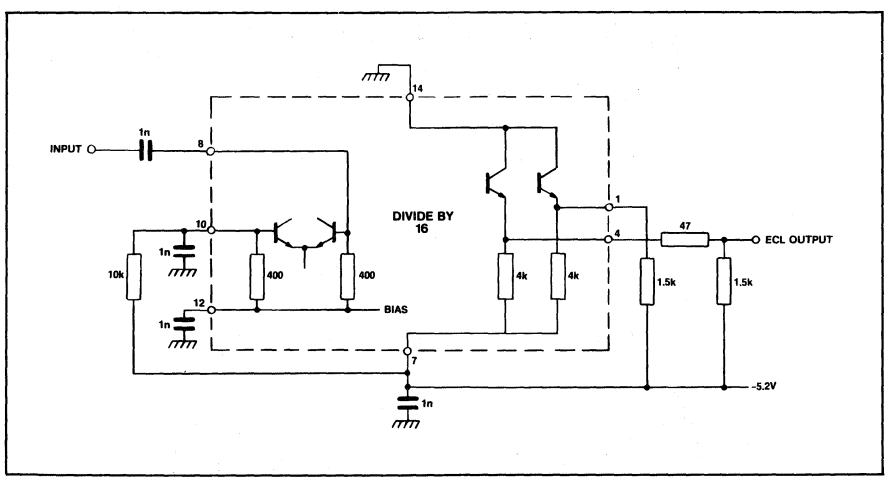


Fig.6 Typical application showing interfacing

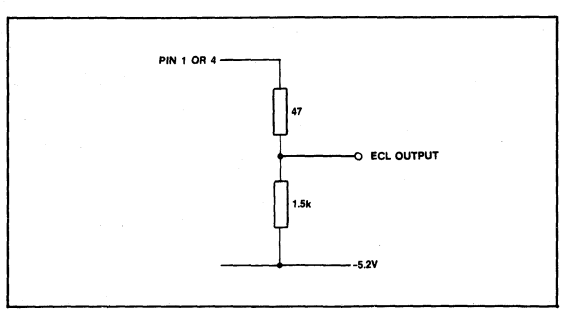


Fig.7 Interfacing to ECL 10K

SP8655 200MHz ÷ 32
SP8657 200MHz ÷ 20
SP8659 200MHz ÷ 16

The SP8655, 57 and 59 are low power emitter coupled logic counters with open collector outputs capable of driving TTL or CMOS. They are available in two temperature ranges: -55°C to +125°C (A grade) and -30°C to +70°C (B grade). It has internally biased inputs.

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ORDERING INFORMATION

See page 3-120

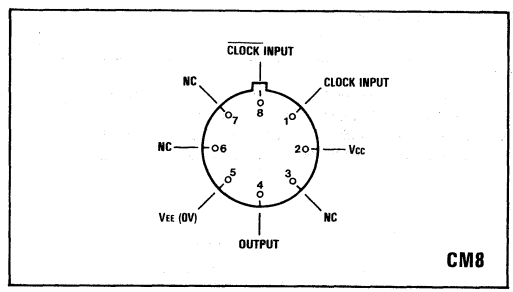


Fig.1 Pin connections - bottom view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p
Output sink current	10mA

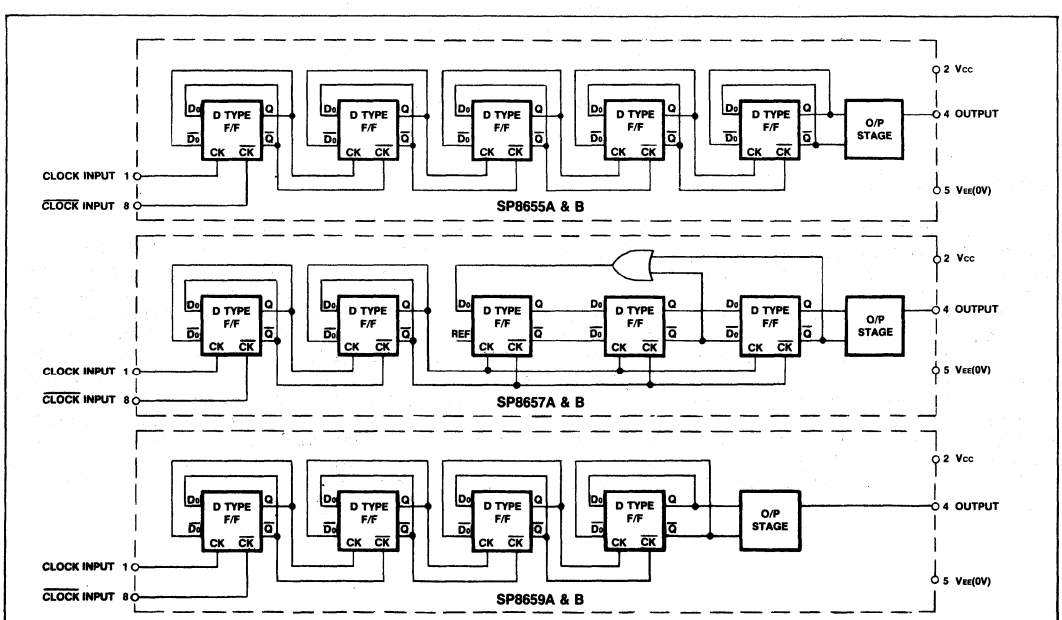


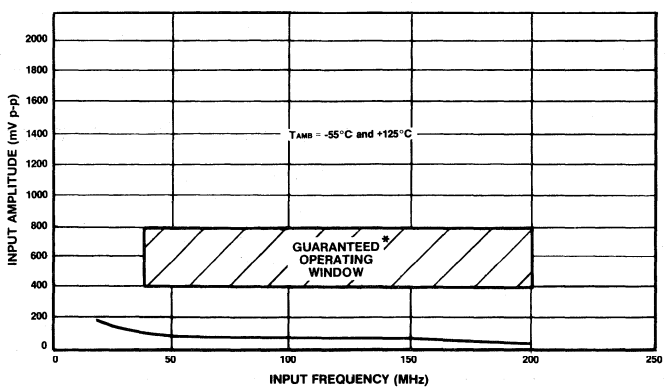
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{max}	200		MHz	Input =400 - 800mV
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input =400 - 800mV
Power supply current	I_{EE}		13	mA	V_{CC}= 5.25V
Output high voltage	V_{OH}	7.5		V	V_{CC}= 5V Note 4 Pin 4 = 1.5kΩ to 10V
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V Pin 4 = 1.5kΩ to 10V

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).
4. Open collector output not to be used above 15MHz. $C_{load} \leq 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to V_{CC} to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is typically 10ns.

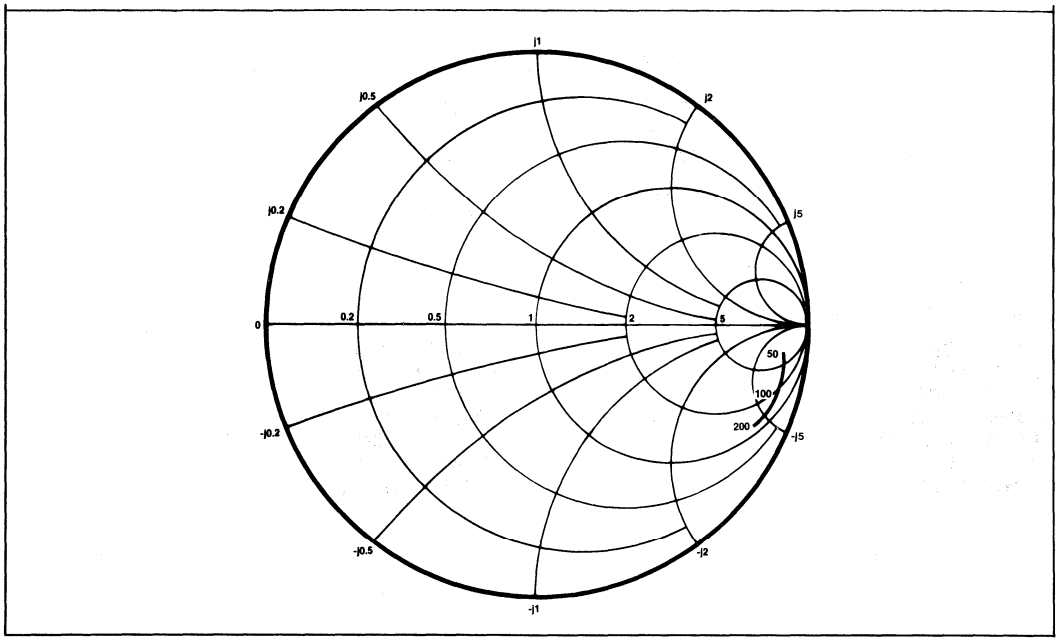


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

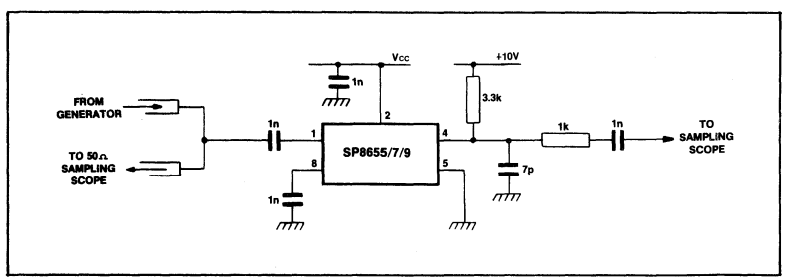


Fig.5 Test circuit

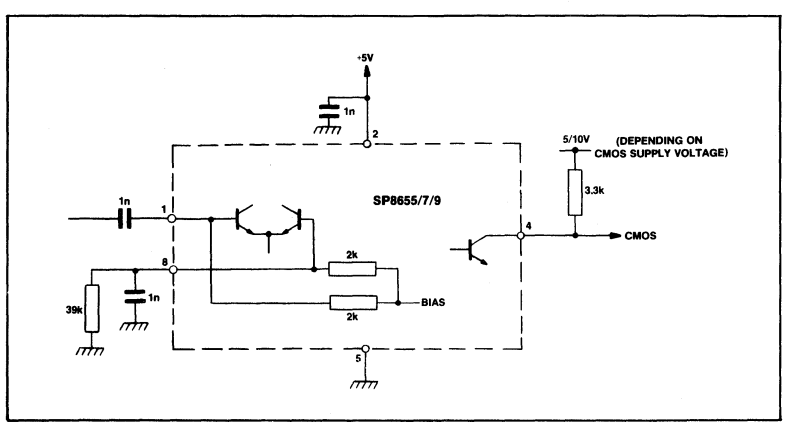


Fig.6 Typical application showing interfacing

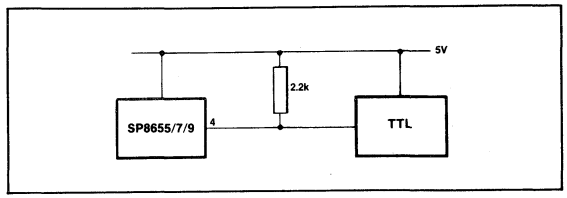


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

ORDERING INFORMATION

SP8655 A CM
SP8655 B CM
SP8655 AB CM
SP8655 AC CM
SP8655 ABSS2 CM
SP8657 A CM
SP8657 B CM
SP8657 AB CM
SP8657 AC CM
SP8659 A CM
SP8659 B CM
SP8659 AB CM
SP8659 AC CM
SP8659 ABSS2 CM

SP8660

150MHz ÷ 10

The SP8660 is a low power emitter coupled logic counter with an open collector output capable of driving TTL or CMOS. It has internally biased inputs and an open collector.

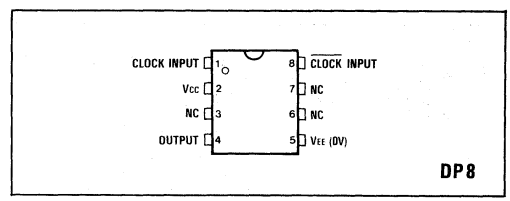


Fig.1 Pin connections - top view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range: -30°C to +70°C
- 8 Lead Plastic Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	-55°C to +125°C
Max. junction temperature	+175°C
Output sink current	10mA
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8660 DP

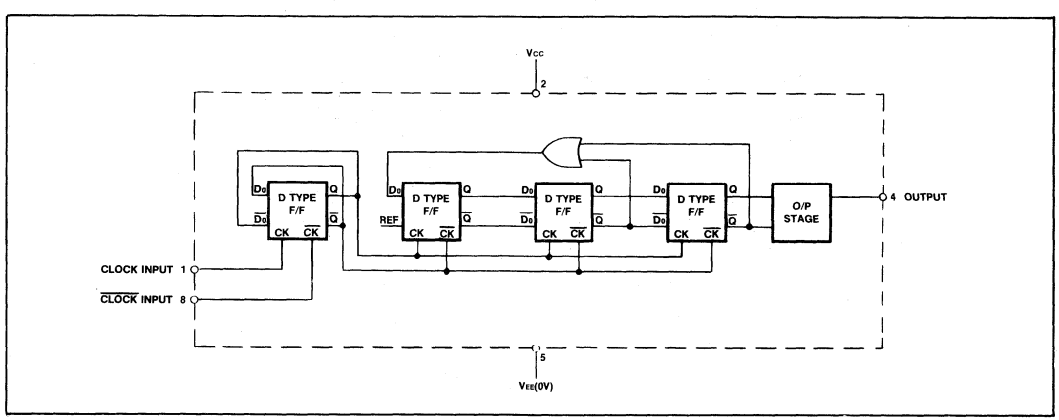


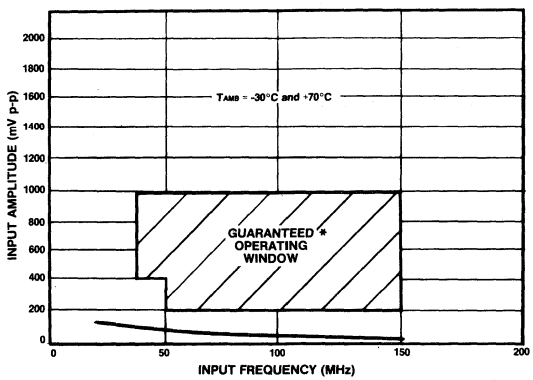
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input = 200-1000mV	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-1000mV	
Power supply current	I_{EE}		13	mA	V_{CC} = 5.25V	
Output high voltage	V_{OH}	9		V	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. All characteristics above are tested at 25°C only.
4. $C_{load} \leqslant 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics

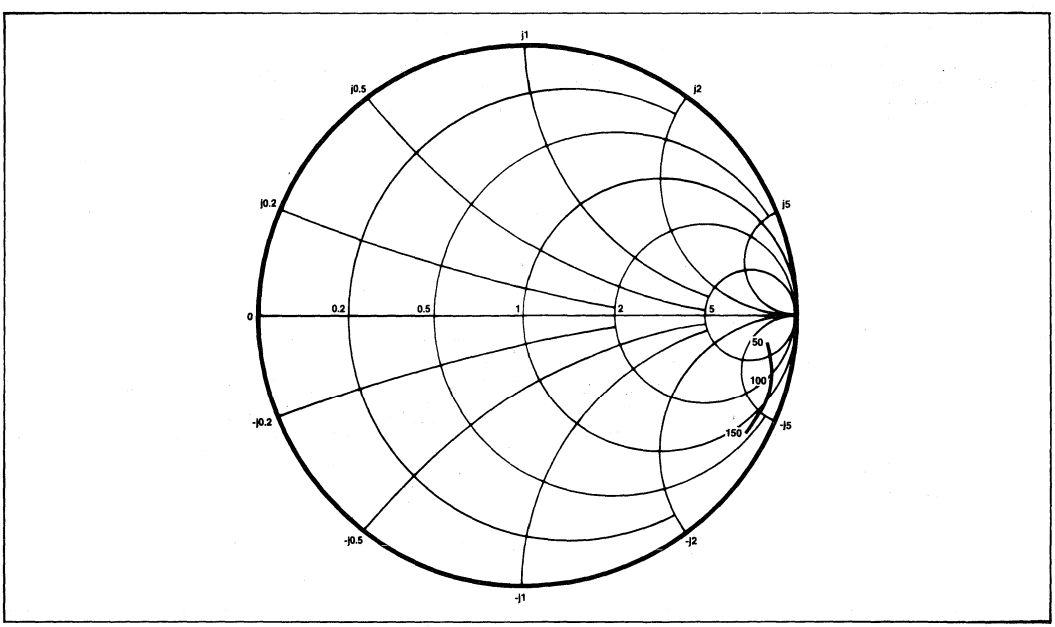


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to Vcc to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be returned to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig.4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is 10ns typically.

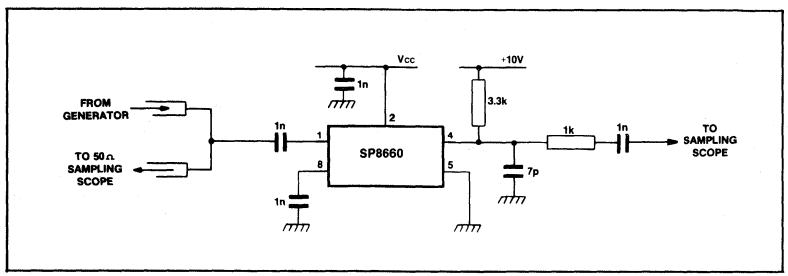


Fig.5 Test circuit

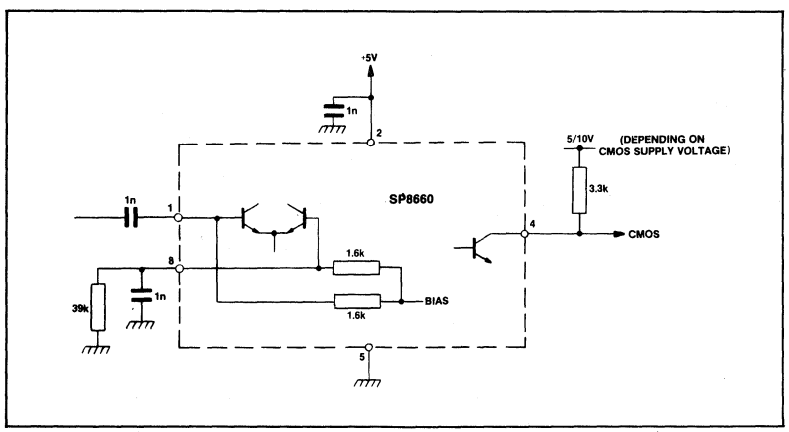


Fig.6 Typical application showing interfacing

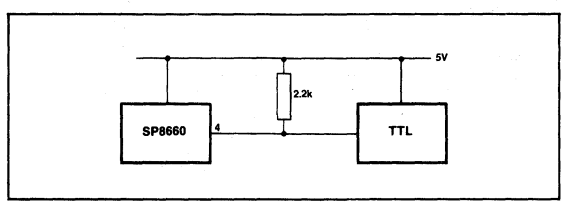


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

SP8660A & B

150MHz ÷ 10

The SP8660A/B is a low power emitter coupled logic counter with an open collector output capable of driving TTL or CMOS. The device is available in two temperature ranges: -55°C to +125°C (A grade) or -30°C to +70°C (B grade). It has internally biased inputs.

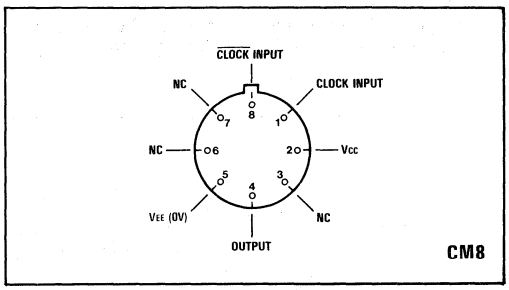


Fig.1 Pin connections - bottom view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range:
  - -55°C to +125°C (SP8660A)
  - -30°C to +70°C (SP8660B)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Output sink current	10mA
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8660 A CM
SP8660 B CM
SP8660 AB CM
SP8660 AC CM
SP8660 ABSS2 CM

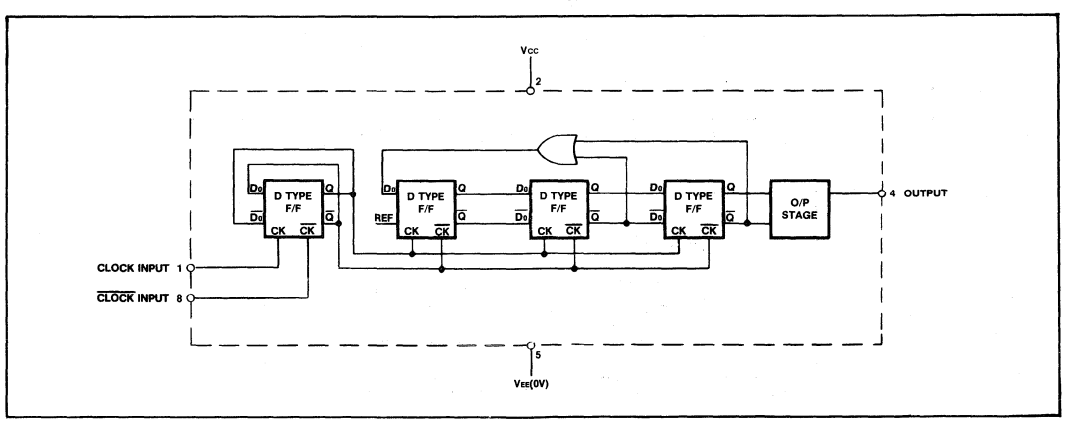


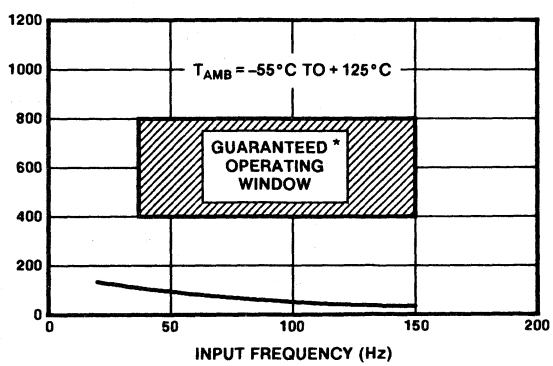
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input =400 - 800mV	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input =400 - 800mV	
Power supply current	I_{EE}		13	mA	V_{CC}= 5.25V	
Output high voltage	V_{OH}	7.5		V	V_{CC}= 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).
4. $C_{load} \leq 5pF$.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8860A and B

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to V_{CC} to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is 10ns typically.

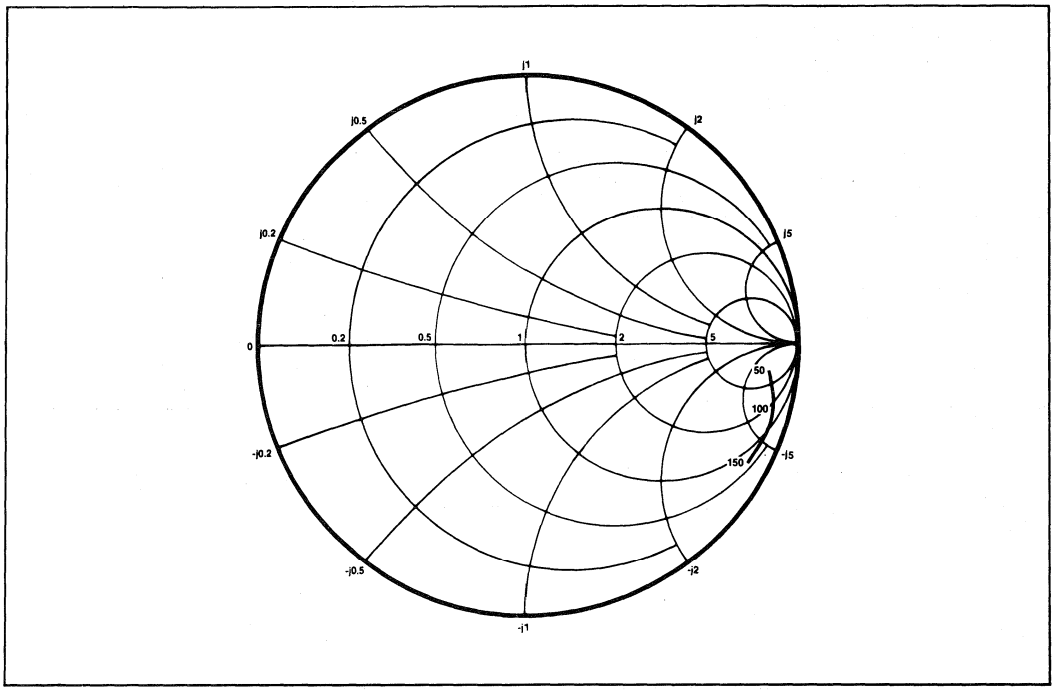


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

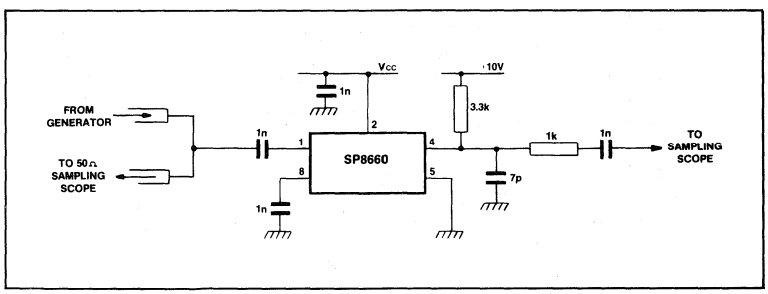


Fig.5 Test circuit

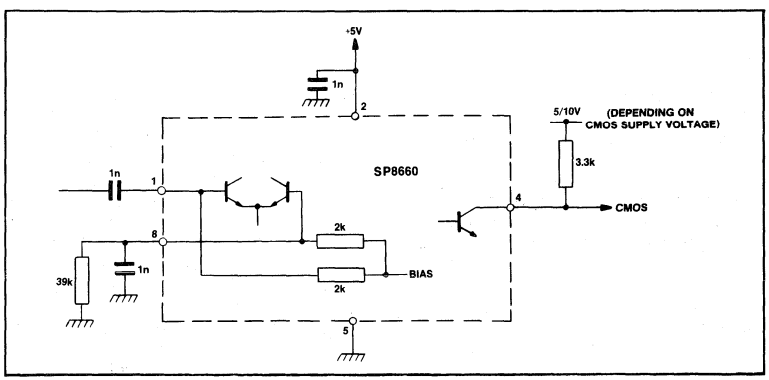


Fig.6 Typical application showing interfacing

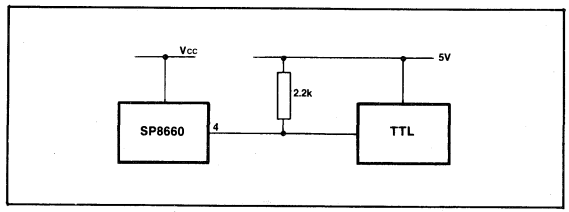


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

SP8665 1000MHz ÷ 10
SP8668 1500MHz ÷ 10

The SP8665/8 are asynchronous ECL counters which provide ECL compatible outputs. They feature an ECL compatible input inhibit which simplifies the design of frequency counters and other instrumentation.

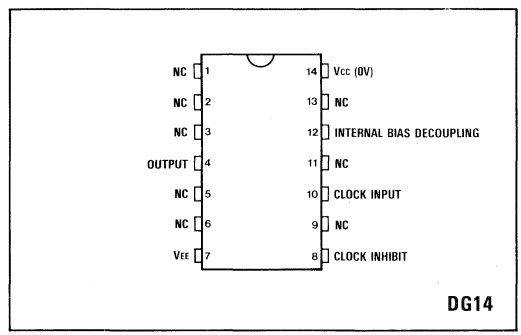


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input
- Clock Inhibit Input

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 500mW
- Temperature Range: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8665 B DG
SP8668 B DG

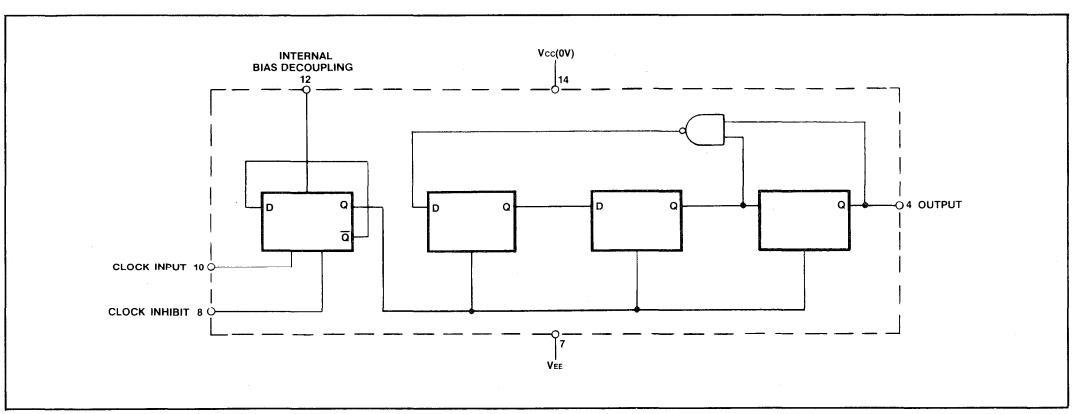


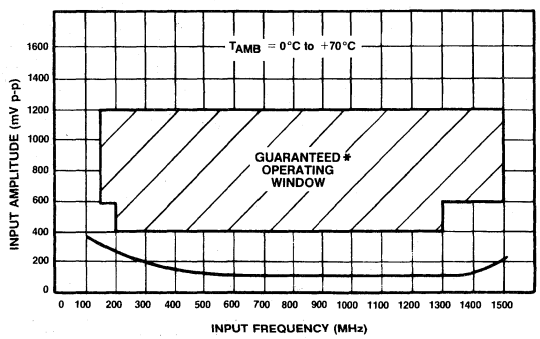
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V V_{EE} = -6.8V ± 0.3V
T_{amb} (B grade) = 0°C to +70°C

Characteristic	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency(sine wave I/P)	f_{max}	1.0		GHz	SP8665B	Input = 400-1200mV p-p	Note 5
		1.5		GHz	SP8668B	Input = 600-1200mV p-p	Note 5
Minimum frequency(sine wave I/P)	f_{min}		150	MHz	All	Input = 600-1200mV p-p	Note 6
Current consumption	I_{EE}		105	mA	All	V_{EE} = -6.8V	Note 6
Output low voltage	V_{OL}	-1.87	-1.5	V	All	V_{EE} = -6.8V (25° C)	
Output high voltage	V_{OH}	-0.87	-0.7	V	All	V_{EE} = -6.8V (25° C)	
Minimum output swing	V_{OUT}	500		mV	All		Note 5
Clock inhibit high threshold voltage	V_{INBH}	-0.96		V	All	V_{EE} = -6.8V (25° C)	
Clock inhibit low threshold voltage	V_{INBL}		-1.62	V	All	V_{EE} = -6.8V (25° C)	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The temperature coefficient of V_{OH} = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
4. The temperature coefficient of V_{INB} = +0.8mV/°C but this is not tested.
5. Tested at 25°C and 70°C only.
6. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic SP8668. The SP8665 operating window is similar except for the maximum operating frequency

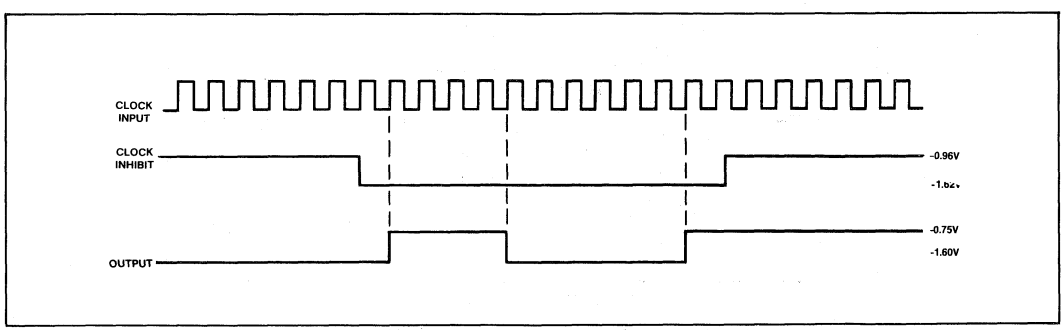


Fig.4 Timing diagram(N.B. output waveform is asymmetric)

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The clock inhibit input is compatible with standard ECL III/10K using a common 0V. A 6k pulldown resistor is included on the chip. The input should be left open to DC when not in use, but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity.
4. Input impedance is a function of frequency. See Fig. 5.
5. The emitter follower output includes an internal 3k pulldown resistor and is compatible with ECL II, but can be interfaced with ECL III/10K by the inclusion of two resistors. See Fig. 7.
6. Note that all components should be suitable for the frequency in use.
7. The circuit will operate to DC but the input slew rate must be 200V/µs or greater.

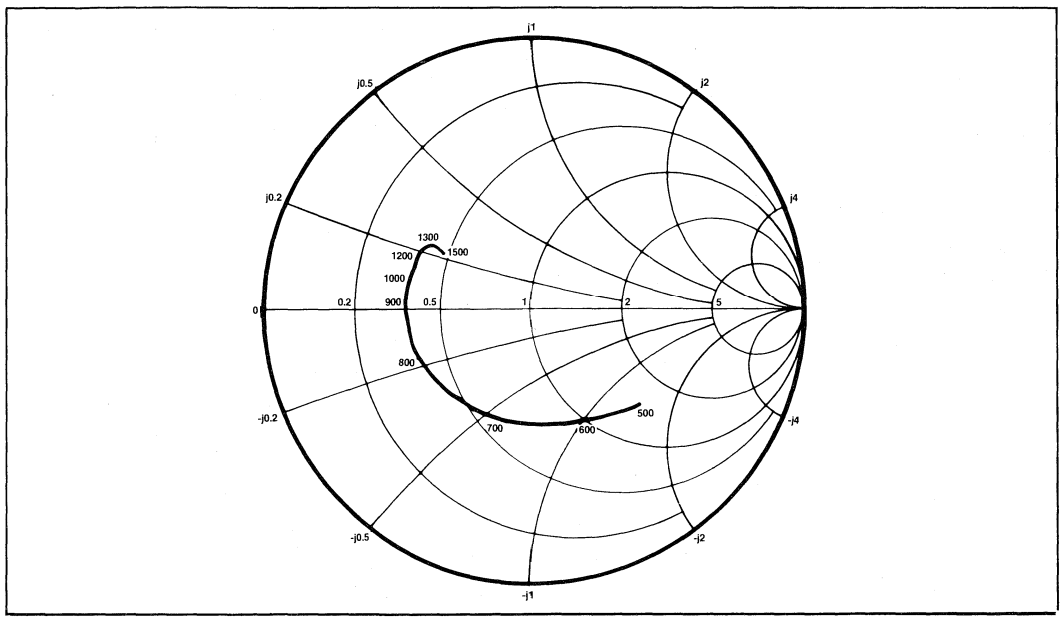


Fig.5 Typical input impedance. Test conditions: supply voltage -6.8V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

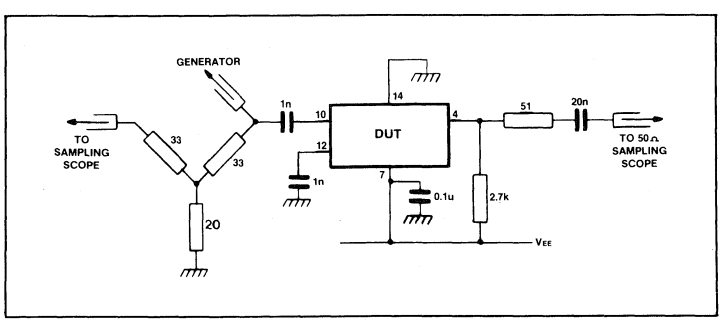


Fig.6 Test circuit

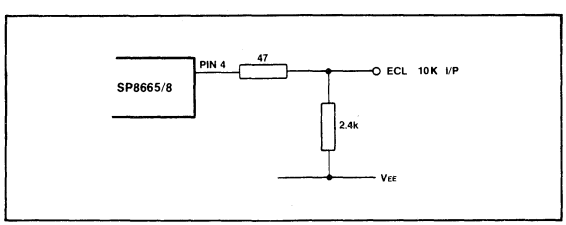


Fig.7 SP8665/8 to ECL 10K interface

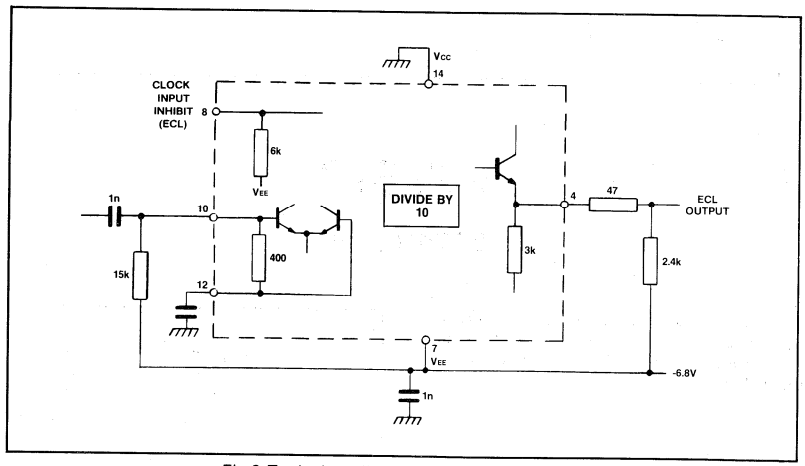


Fig.8 Typical application showing interfacing

SP8670

600MHz ÷ 8

The SP8670 is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs when external pulldown resistors are added. It requires an AC coupled input of 600mV p-p.

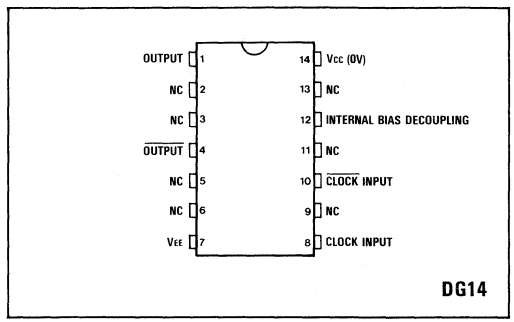


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 300mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	10mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8670 A DG
SP8670 B DG
SP8670 AB DG
SP8670 AC DG

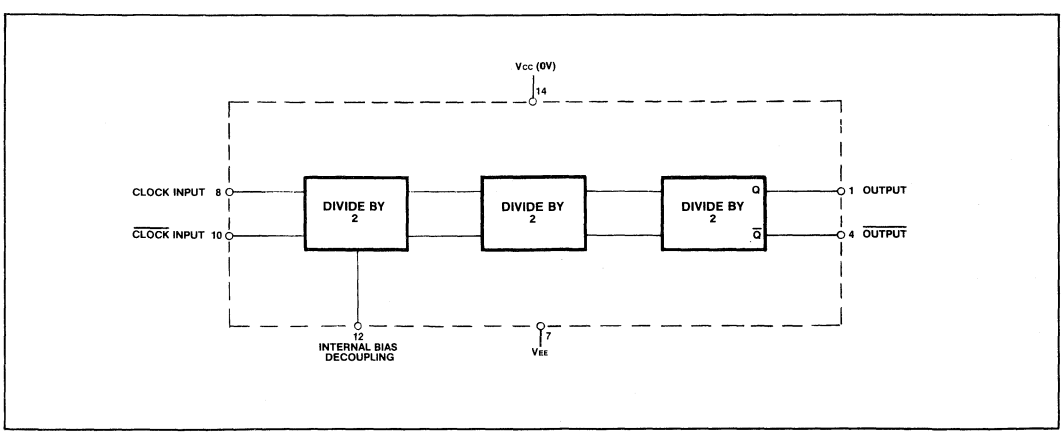


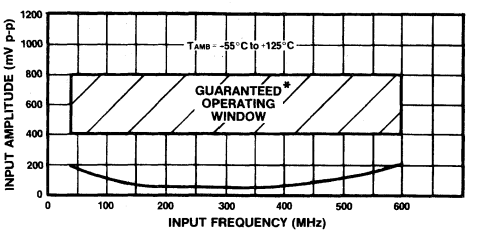
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		60	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
Minimum output swing	V_{OUT}	500		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristic of SP8670A

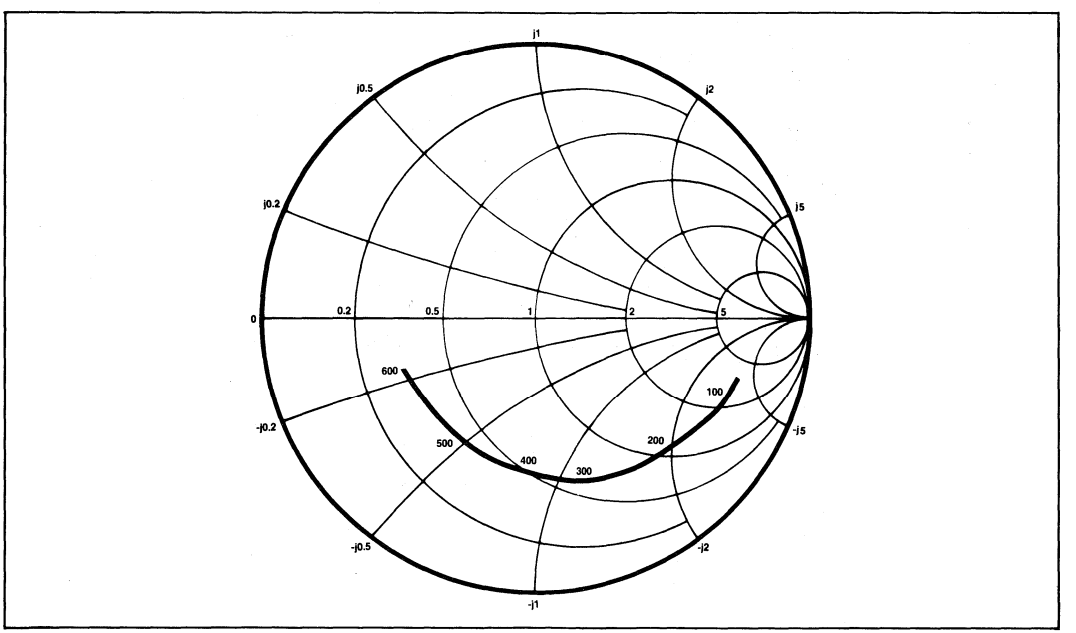


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 8 and 10) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from one of the inputs to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k at each output. The output can be interfaced to ECL 10K by addition of two resistors.
5. Input impedance is shown in Fig. 4.
6. All components should be suitable for the frequency in use.

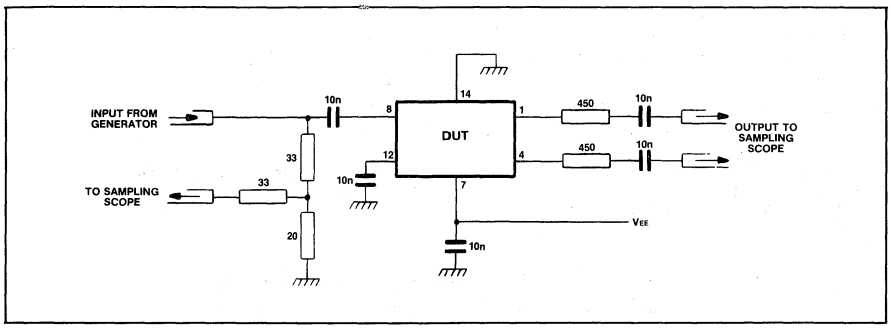


Fig.5 Test circuit

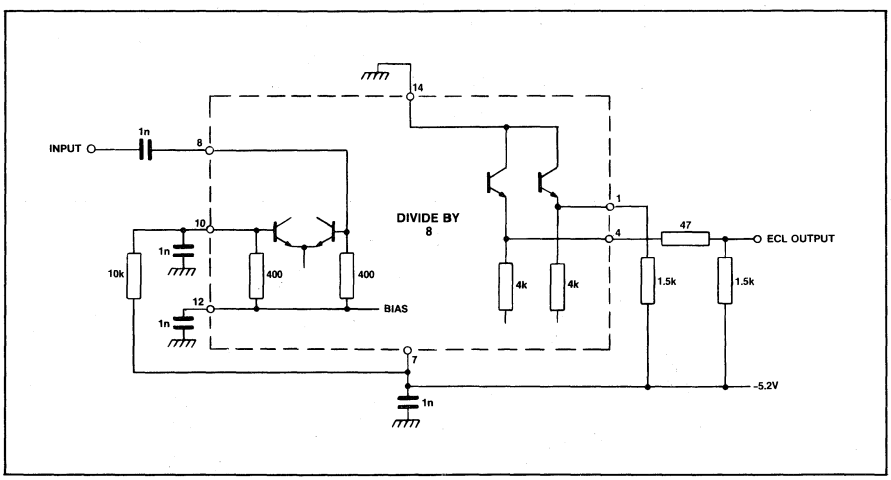


Fig.6 Typical application showing interfacing

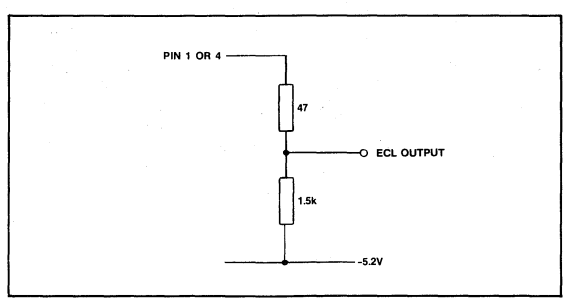


Fig.7 Interfacing to ECL 10K

SP8678

1500MHz ÷ 8

The SP8678 is an asynchronous ECL counter which provides ECL compatible outputs. It features an ECL compatible input inhibit which simplifies the design of frequency counters and other instrumentation.

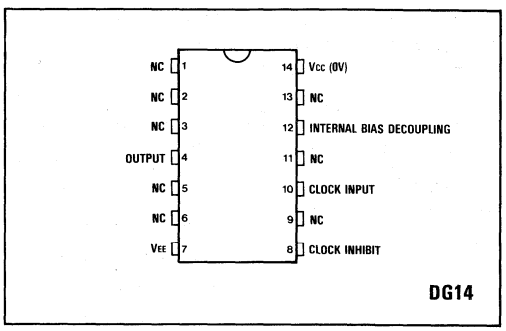


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input
- Clock Inhibit Input

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 475mW
- Temperature Range: **0°C to +70°C (B Grade)**
  –40°C to +85°C (M Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Output current	20mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8678 B DG
SP8678 M DG

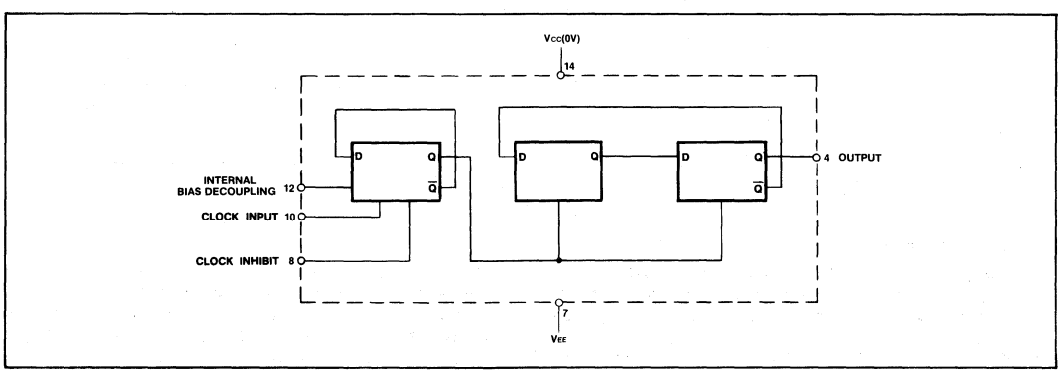


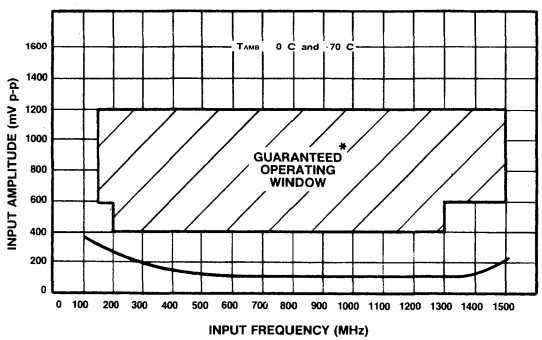
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = –6.8V ± 0.3V
T_{AMB} = 0°C to + 70°C (B Grade), –40°C to + 85°C (M Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	1.5		GHz	Input =600 - 1200mV p-p	Note 5
Minimum frequency (sinewave input)	f_{min}		150	MHz	Input =600 - 1200mV p-p	Note 6
Current consumption	I_{EE}		95	mA	V_{EE} = -6.8V	Note 6
Output low voltage	V_{OL}	-1.87	-1.5	V	V_{EE} = -6.8V(25° C)	
Output high voltage	V_{OH}	-0.87	-0.7	V	V_{EE} = -6.8V(25° C)	
Minimum output swing	V_{OUT}	500		mV		Note 5
Clock inhibit high threshold voltage	V_{INBH}	-0.96		V	V_{EE} = -6.8V(25° C)	
Clock inhibit low threshold voltage	V_{INBL}		-1.62	V	V_{EE} = -6.8V(25° C)	

NOTES
1. Unless otherwise stated, the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig. 6.
3. The temperature coefficient of V_{OH} = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
4. The temperature coefficient of V_{INB} = +0.8mV/°C but this is not tested.
5. Tested at 25°C and 70°C only.
6. Tested at 25°C only.



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics

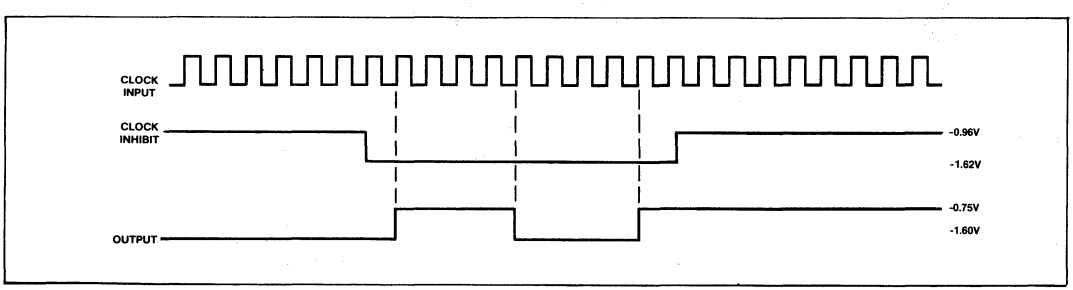


Fig.4 Timing diagram

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The clock inhibit input is compatible with standard ECL III/10K using a common 0V. A 6k pulldown resistor is included on the chip. The input should be left open to DC when not in use, but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity.
4. Input impedance is a function of frequency. See Fig. 5.
5. The emitter follower output includes an internal 3k pulldown resistor and is compatible with ECL II, but can be interfaced with ECL III/10K by the inclusion of two resistors. See Fig. 7.
6. Note that all components should be suitable for the frequency in use.
7. The circuit will operate to DC but the input slew rate must be 200V/µs or greater.

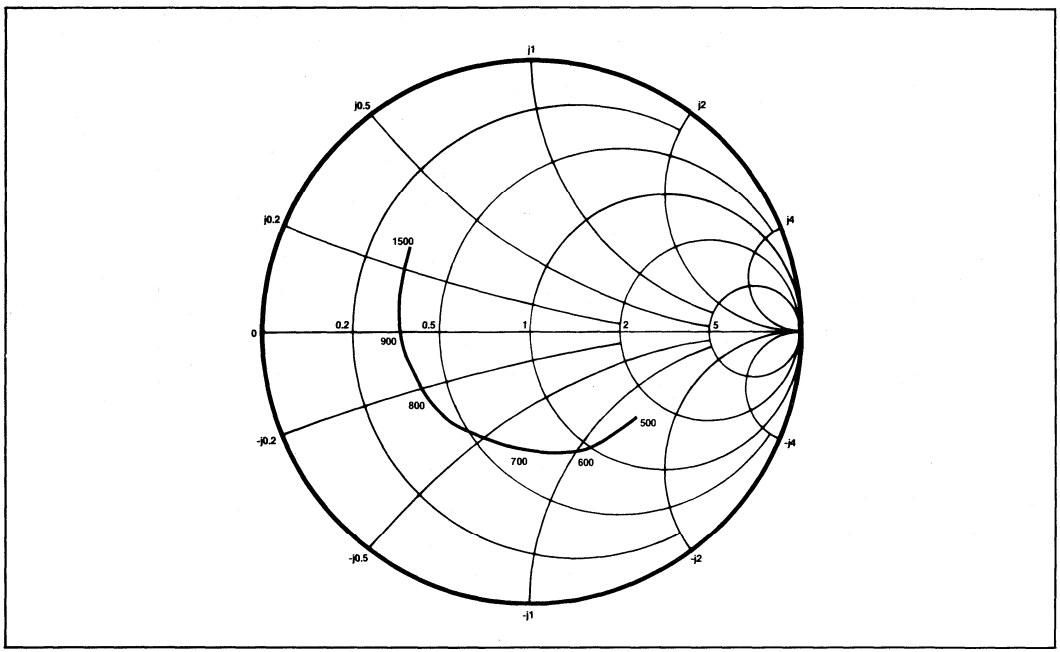


Fig.5 Typical input impedance. Test conditions: supply voltage -6.8V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

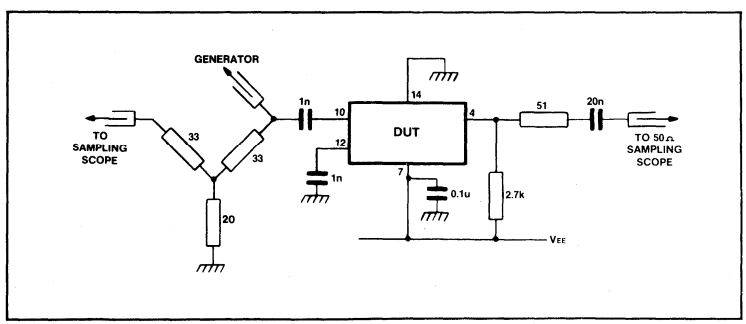


Fig.6 Test circuit

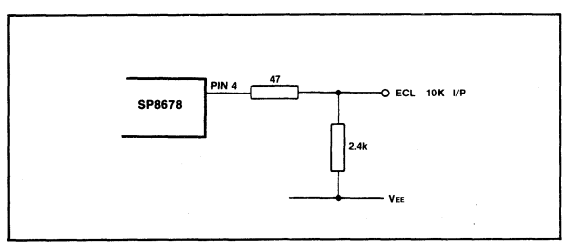


Fig.7 SP8678 to ECL 10K interface

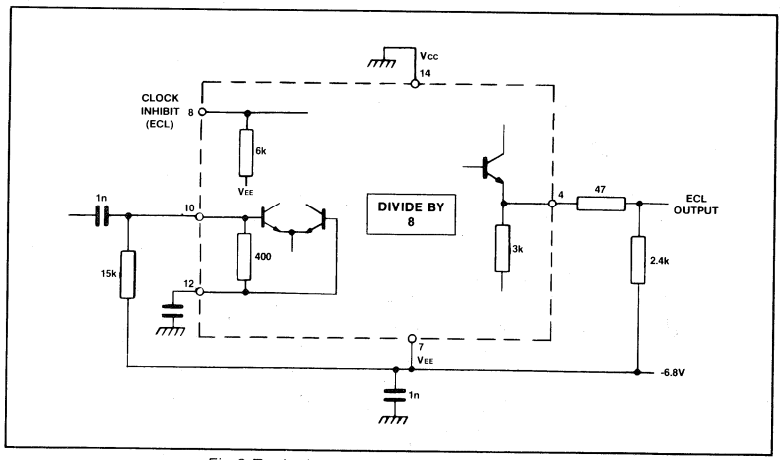


Fig.8 Typical application showing interfacing

SP8735

600MHz ÷ 8 (BINARY OUTPUTS)

The SP8735 is an ECL counter with binary outputs. In addition, carry outputs are provided in TTL and ECL. The AC coupled input requires 600mV p-p, and the outputs are open collectors. A TTL compatible reset is provided, making this device ideal for instrumentation applications.

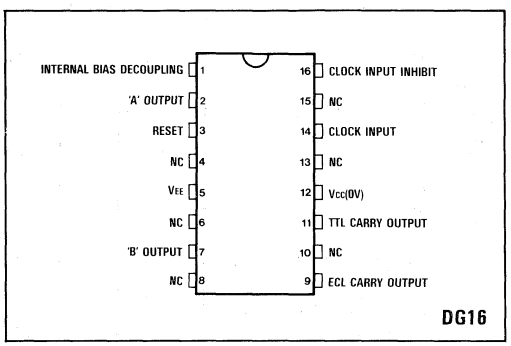


Fig.1 Pin connections - top view

FEATURES

- Binary Outputs to Open Collectors
- Reset Input TTL Compatible
- AC Coupled Input
- Clock Inhibit ECL Compatible
- TTL and ECL Compatible Carry Outputs

QUICK REFERENCE DATA

- Supply Voltage: 5.2V
- Power Consumption: 400mW
- Temperature Range: 0 to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-8V
Binary ourput voltage	V_{EE} +11V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8735 B DG

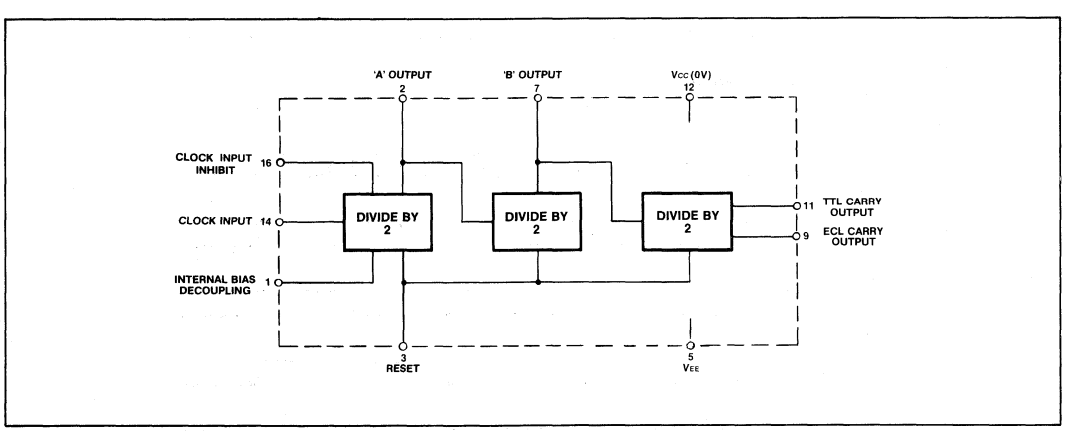


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	Note 5
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 7
Power supply current	I_{EE}		90	mA	V_{EE} = -5.2V	Note 6
Clock inhibit high voltage	V_{INH}	-0.96		V	V_{EE} = -5.2V (25°C)	
Clock inhibit low voltage	V_{INL}		-1.65	V	V_{EE} = -5.2V (25°C)	
TTL output high voltage (pin 2,7)	V_{OH}	2.4		V	10k Ω from TTL output to +5V	Note 6
TTL output low voltage (pin 2,7)	V_{OL}		0.4	V	10k from TTL output to +5V	Note 6
TTL carry high voltage (pin 11)	V_{OH}	2.4		V	5k Ω from TTL output to +5V	Note 6
TTL carry low voltage (pin 11)	V_{OL}		0.4	V	5k Ω from TTL output to +5V	Note 6
ECL carry high voltage (pin 9)	V_{OH}	-0.9	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL carry low voltage (pin 9)	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Edge speed for correct operation at maximum frequency	t_E		2.5	ns	10% to 90%	Note 7
Reset on time for correct operation	t_{ON}	100		ns		Note 7
Reset input high voltage	V_{INH}	2.4		V		Note 6
Reset input low voltage	V_{INL}		0.5	V		Note 6

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} (ECL) = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
3. The temperature coefficient of inhibited threshold voltage = +0.24mV/°C but this is not tested.
4. The test configuration for dynamic testing is shown in Fig.8.
5. Tested at 0°C and +70°C only.
6. Tested at +25°C only.
7. Guaranteed but not tested.

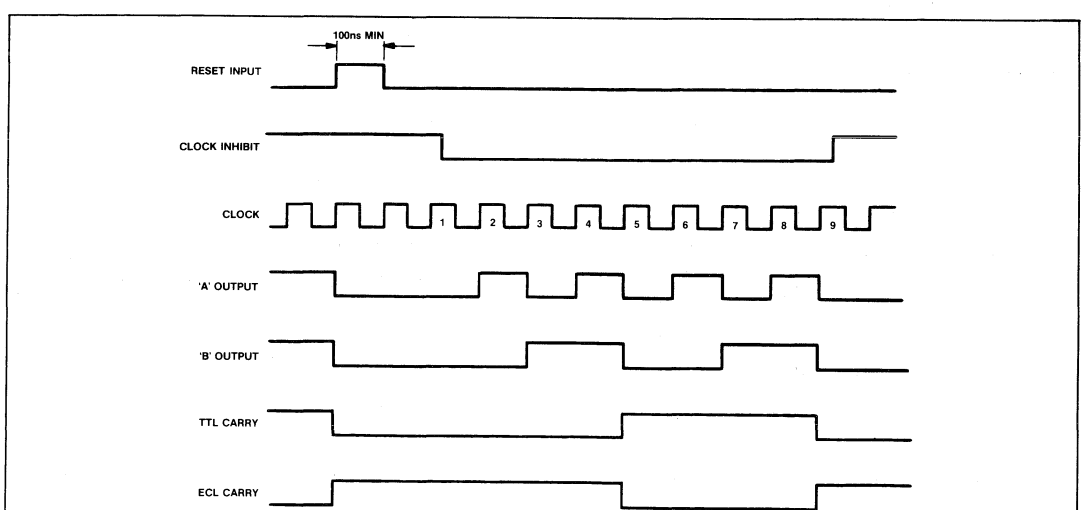


Fig.3 Timing diagram

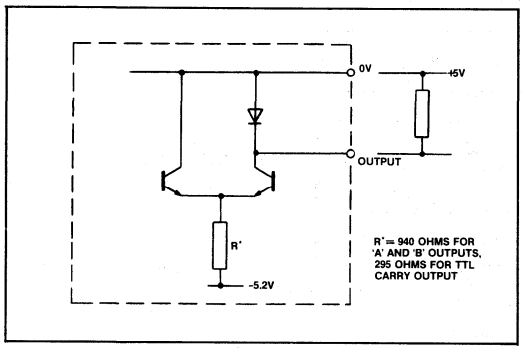


Fig.6 TTL output circuit

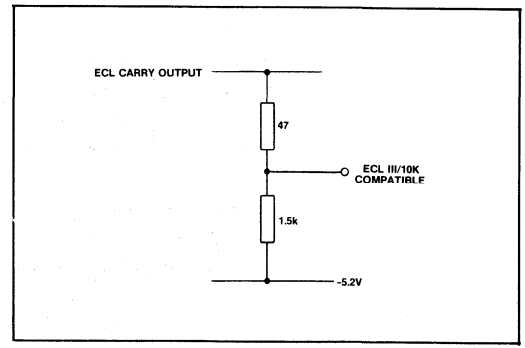


Fig.7 ECL II to ECL III/10K interface

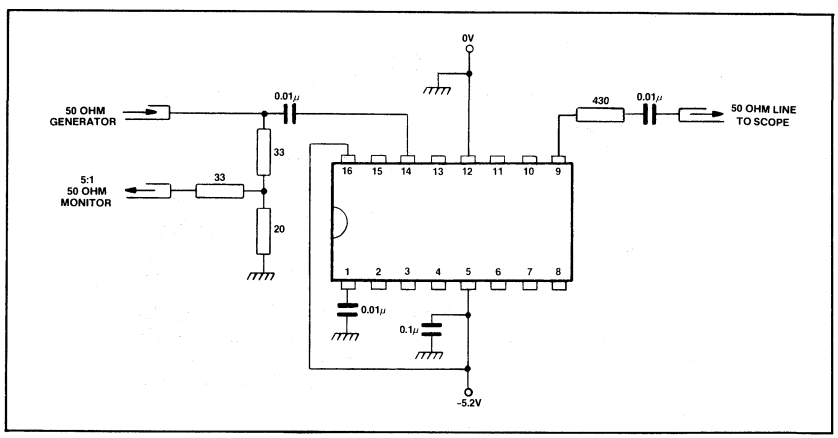


Fig.8 SP8735 high frequency test circuit

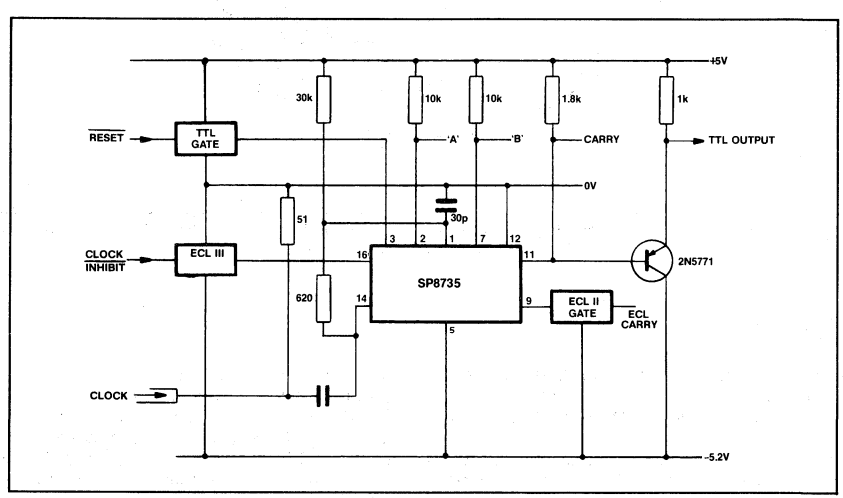
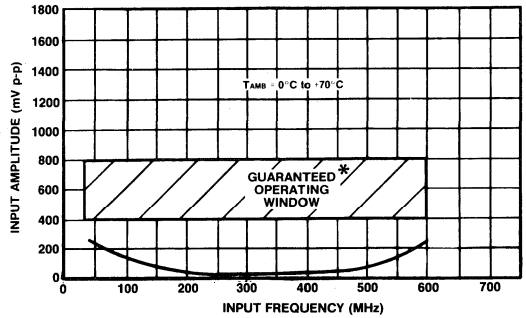


Fig.9 Typical application showing interfacing



*Tested as specified above.

Fig.4 Typical input characteristics SP8735

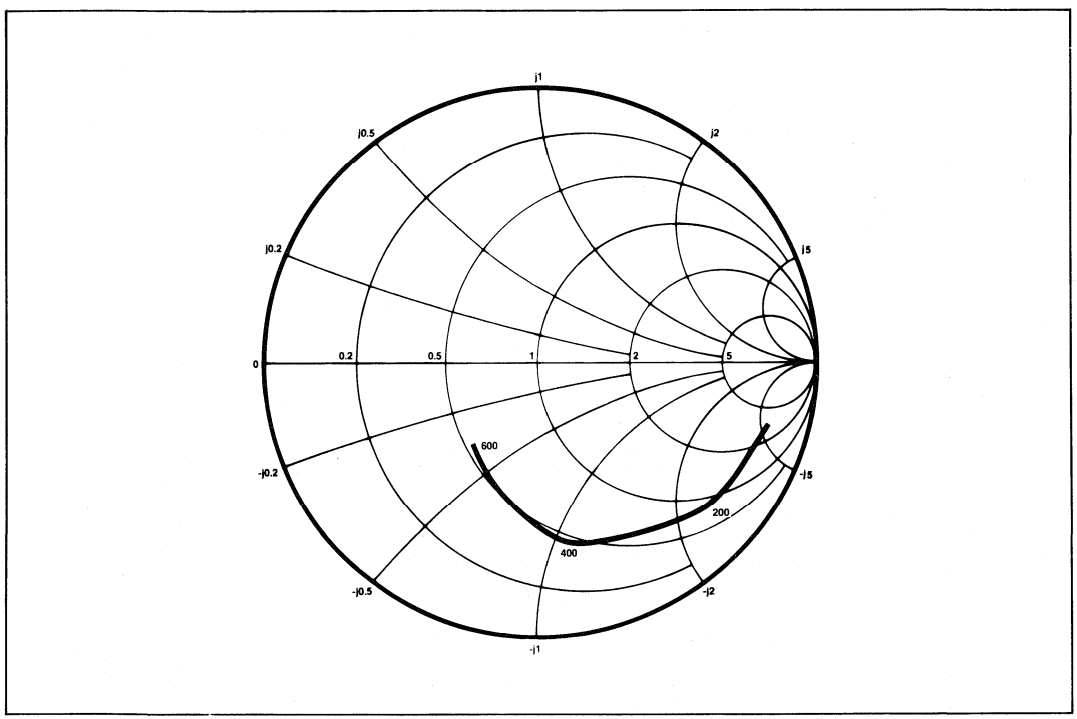


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 14) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 1 to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 68k resistor between the clock input and the negative supply (pin 5).
3. The device will operate down to DC but the input slew rate must be better than 100V/μs.
4. The ECL Carry output (pin 9) is ECL II compatible but can be interfaced ECL III/10K by the inclusion of two resistors. See Fig.7.
5. The clock inhibit is compatible with ECL III/10K throughout the temperature range.
6. The 'A', 'B' and TTL Carry outputs are current sources and require the addition of 10k (pins 2 and 7) and 5k (pin 11) to +5V for TTL compatibility. See Fig. 6. This gives a fan-out = 1. The fan-out can be increased by buffering the output with a PNP emitter follower, see Fig. 9.
7. It is important to note that a positive going transition on either the clock or clock inhibit will clock the device provided of course that each input is in the low state.
8. Input impedance is a function of frequency. See Fig. 5.

SP8755

1200MHz ÷ 64

The SP8755 is a divide by 64 prescaler which operates from a standard 5V TTL supply and will drive TTL directly. The SP8755A operates over the full military temperature range (-55°C to +125°C).

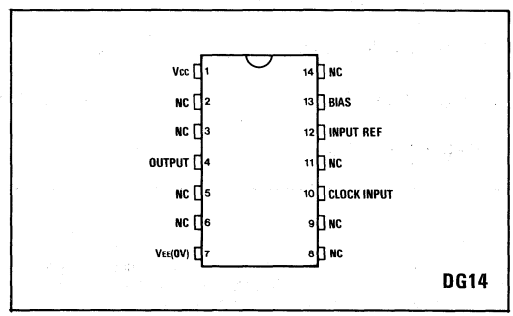


Fig.1 Pin connections - top view

FEATURES

- TTL Compatible Output
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 270mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Output current	±30mA
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

ORDERING INFORMATION

SP8755 A DG
SP8755 B DG
SP8755 AB DG
SP8755 AC DG

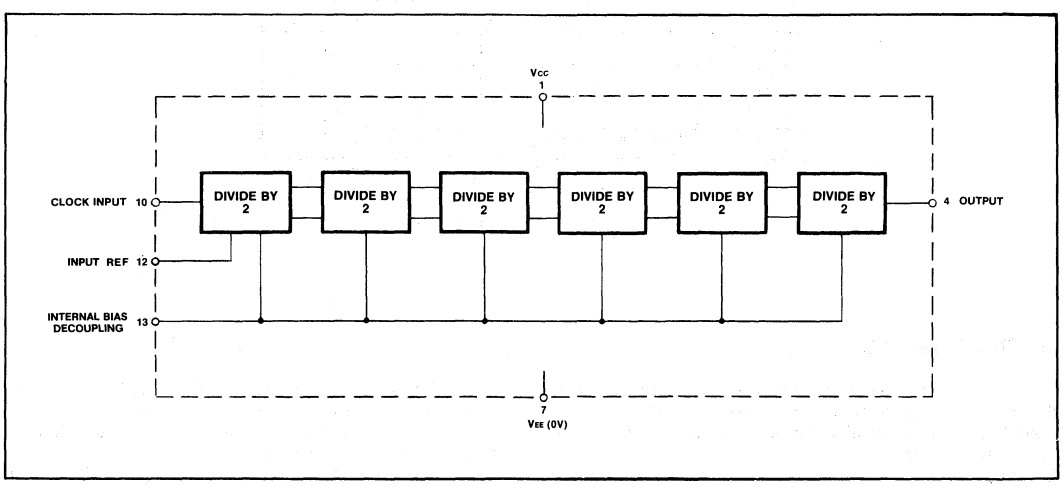


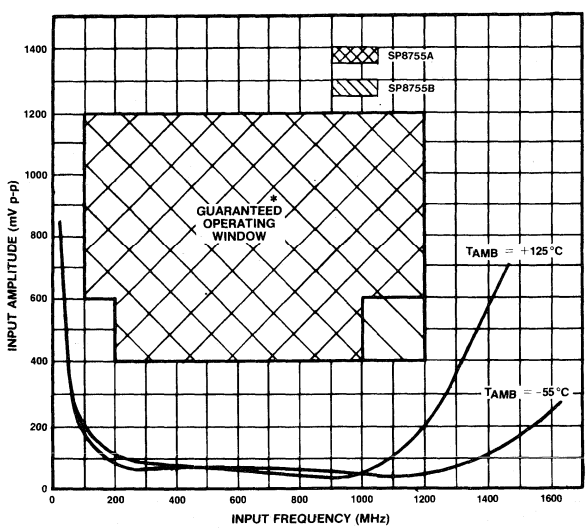
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	1.2		GHz	SP8755A	Input = 600-1200mV p-p
		1.2		GHz	SP8755B	Input = 400-1200mV p-p
Minimum frequency sinewave input	f_{min}		100	MHz	Both	Input = 600-1200mV p-p
Power supply current	I_{EE}		75	mA	Both	
Output high voltage	V_{OH}	2.5		V	Both	
Output low voltage	V_{OL}		0.45	V	Both	Sink current = 5mA

NOTES
1. Unless otherwise stated,the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).



*Tested as specified in table of Electrical Characteristics

Fig.3 Typical input characteristics SP8755A/B

OPERATING NOTES

1. The clock input is biased internally and is connected to the signal source via a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting an 18k resistor between input and V_{EE} (i.e. Pin 10 to Pin 7). This will reduce sensitivity by approximately 100mV.
3. The device will operate down to DC but input slew rate must be better than 100V/µs.
4. The output stage is a standard totem pole TTL and can therefore be interfaced directly to TTL.

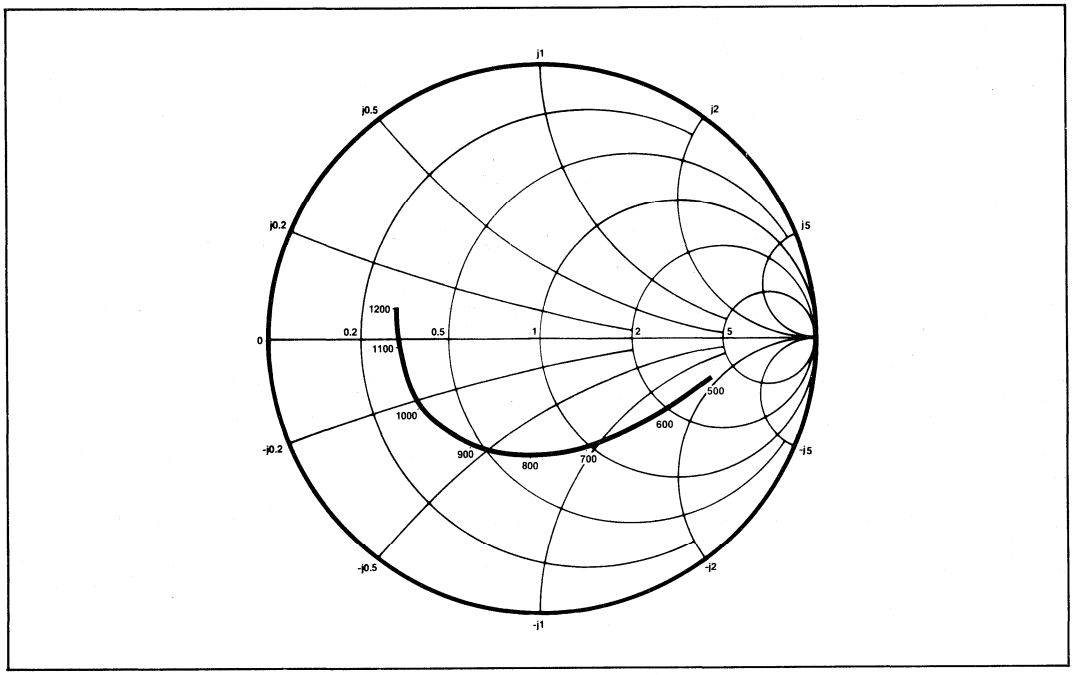


Fig.4 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25°C. Frequencies in MHz, impedances normalised to 50 ohms.

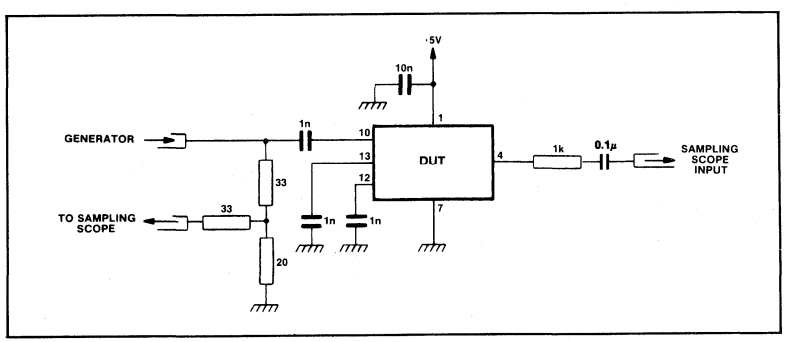


Fig.5 Test circuit

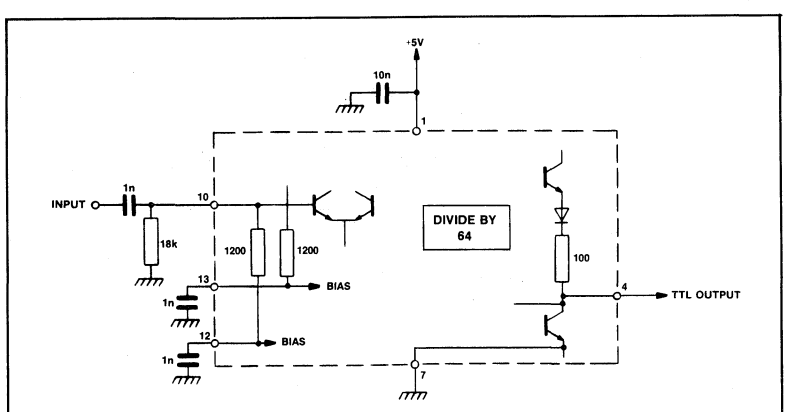


Fig.6 Typical applications circuit showing interfacing

SP8790

60MHz ÷ 4 (2-MODULUS EXTENDER)

The SP8790 is a divide-by-four counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratio. Suitable for low power frequency synthesis interfacing to CMOS or TTL.

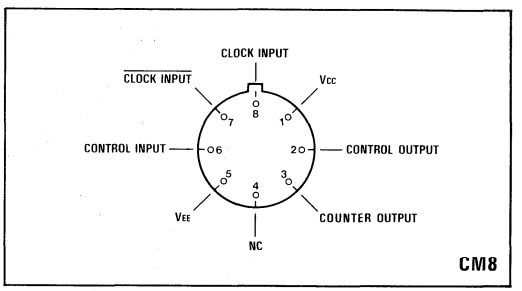


Fig.1 Pin connections

FEATURES

- Very Low Power
- Control Input and Counter Output will Interface Directly to TTL or CMOS
- Interfaces to SP8000 Programmable 2 Modulus Counters

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 40mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p
Output sink current	10mA

ORDERING INFORMATION

SP8790 A CM
SP8790 B CM
SP8790 AB CM
SP8790 AC CM

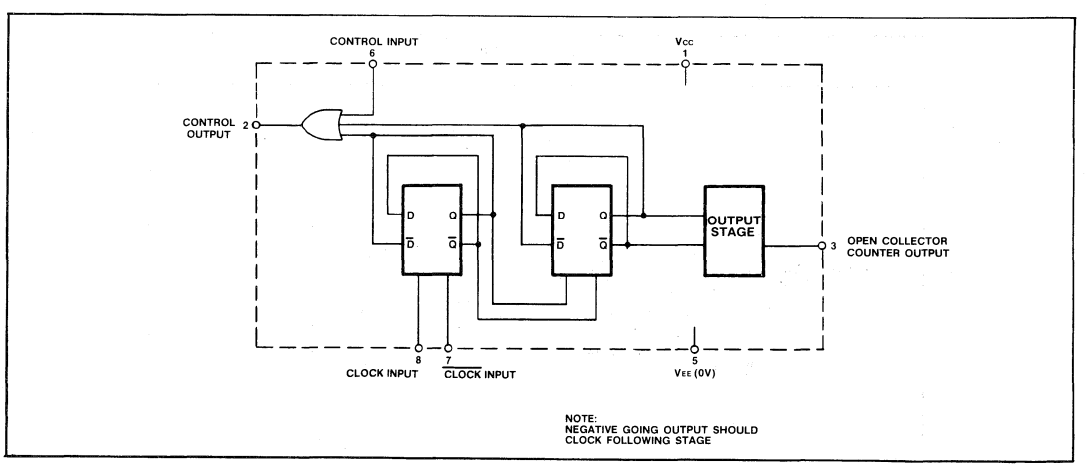


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} = 0V
Temperature: A grade: -55°C to +125°C
B grade: -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	60		MHz	Tested as a controller. See Fig.4	Note 3
Power supply current	I_{EE}		11	mA		Note 3
Control input high voltage	V_{INH}	3.5	10	V		Note 3
Control input low voltage	V_{INL}	0	1.5	V		Note 3
Output high voltage (pin 3)	V_{OH}	9		V	Pin 3 via 1.6k to +10V	Note 3
Output low voltage (pin 3)	V_{OL}		0.4	V	Pin 3 via 1.6k to +10V	Note 3
Output high voltage (pin 2)	V_{OH}	4.27	4.5	V	V_{CC} = 5.2V (25° C)	
Output low voltage (pin 2)	V_{OL}	3.28	3.7	V	V_{CC} = 5.2V (25° C)	
Clock to counter output -ve going delay	t_{pHL}		25	ns		Note 4
Clock to counter output +ve going delay	t_{pLH}		40	ns		Note 4
Clock to control output -ve going delay	t_{pLH}		15	ns	10kΩ pull-down on control O/P	Note 4
Clock to control output +ve going delay	t_{pHL}		26	ns	10kΩ pull-down on control O/P	Note 4
Control input to control output -ve going delay	t_{pLH}		12	ns	10kΩ pull-down on control O/P	Note 4
Control input to control output +ve going delay	t_{pHL}		16	ns	10kΩ pull-down on on control O/P	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.4.
3. Tested at low and high temperatures only.
4. Guaranteed but not tested.

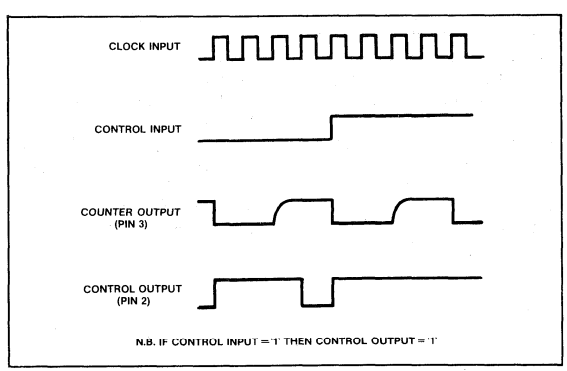


Fig.3 Timing diagram

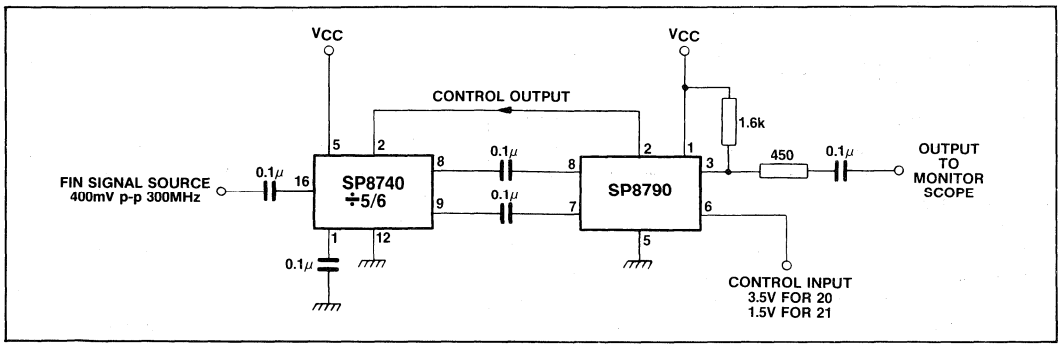


Fig.4 Test circuit

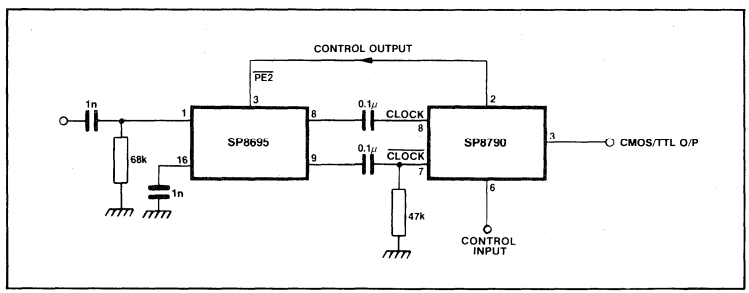


Fig.5 Typical interfacing to suppress self oscillation with no input signal

OPERATING NOTES

1. The device will normally be driven by capacitively coupling the inputs to outputs of a 2-modulus divider. See Figs. 4 and 5. The maximum frequency of the device when used as a controller is limited by the internal delays and will not operate above 60MHz. When used as a prescaler the device will operate in excess of 80MHz, the maximum frequency being limited by saturation of the counter output stage.
2. The device is normally driven from very fast edges of a 2-modulus divider and therefore there is no input slew rate problem.
3. The control input is TTL/CMOS compatible.
4. The counter output (pin 3) interfaces into CMOS/TTL by the addition of a pull-up resistor. For interconnecting to CMOS the output can be connected via a pull-up resistor to supply which should not exceed 12V.
5. When used as a controller the circuit will self-oscillate. This can be prevented by using one of the arrangements as shown in Fig. 5.
6. The control output, which includes an internal 16k pull-down resistor is ECL compatible and interfaced directly into, for example, SP8695. See Fig. 5.
7. The propagation delays stated are with a 10k pull-down resistor which is input pull-down of the SP8695. For interfacing into the SP8643/47 series which have 4.3k pull-downs, the propagation delays will be reduced.

SP8794

60MHz ÷ 8 (2-MODULUS EXTENDER)

The SP8794 is a divide-by-eight counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratio. Suitable for low power frequency synthesis interfacing to CMOS or TTL.

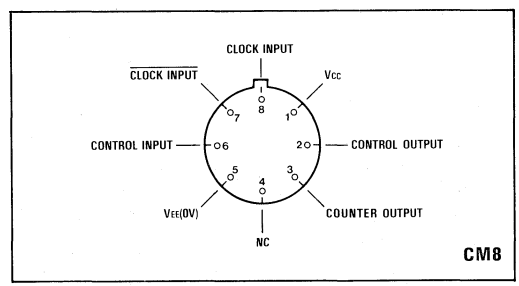


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Counter Output will Interface Directly to TTL or CMOS
- Interfaces to SP8000 Programmable 2-Modulus Counters

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 40mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Output collector output	12V
Storage temperature range	-55°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p
Output sink current	10mA

ORDERING INFORMATION

SP8794 A CM
SP8794 B CM
SP8794 AB CM
SP8794 AC CM

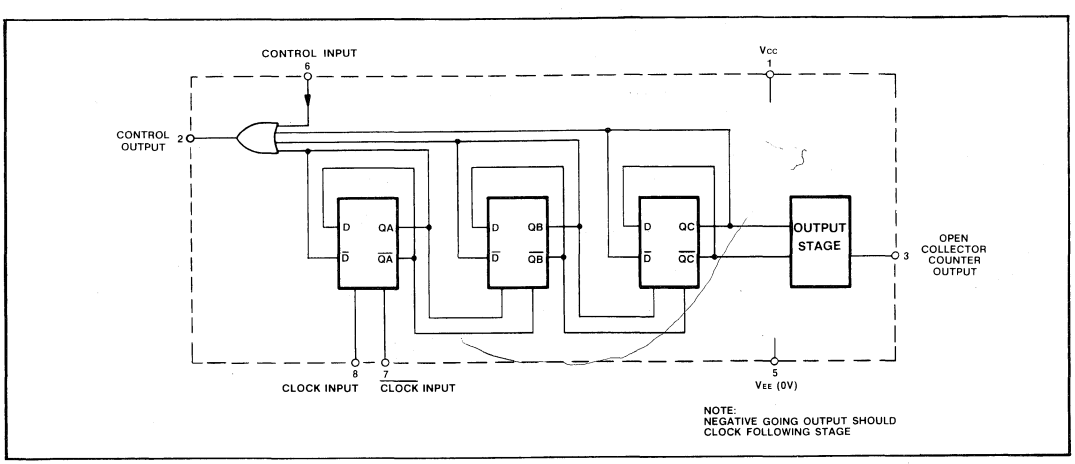


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} = 0V
Temperature: A grade: -55°C to +125°C
B grade: -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	60		MHz	Tested as a controller. See Fig. 4	Note 3
Power supply current	I_{EE}		11	mA		Note 3
Control input high voltage	V_{INH}	3.5	10	V		Note 3
Control input low voltage	V_{INL}	0	1.5	V		Note 3
Output high voltage (pin 3)	V_{OH}	9		V	Pin 3 via 1.6k to +10V	Note 3
Output low voltage (pin 3)	V_{OL}		0.4	V	Pin 3 via 1.6k to +10V	Note 3
Output high voltage (pin 2)	V_{OH}	4.27	4.5	V	V_{CC} = 5.2V(25° C)	
Output low voltage (pin 2)	V_{OL}	3.28	3.7	V	V_{CC} = 5.2V(25° C)	
Clock to counter output -ve going delay	t_{pHL}		27	ns		Note 4
Clock to counter output +ve going delay	t_{pLH}		48	ns		Note 4
Clock to control output -ve going delay	t_{pLH}		15	ns	10k pull-down on control O/P	Note 4
Clock to control output +ve going delay	t_{pHL}		26	ns	10k pull-down on control O/P	Note 4
Control input to control output -ve going delay	t_{pLH}		12	ns	10k pull-down on control O/P	Note 4
Control input to control output +ve going delay	t_{pHL}		16	ns	10k pull-down on on control O/P	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.4.
3. Tested at low and high temperatures only.
4. Guaranteed but not tested.

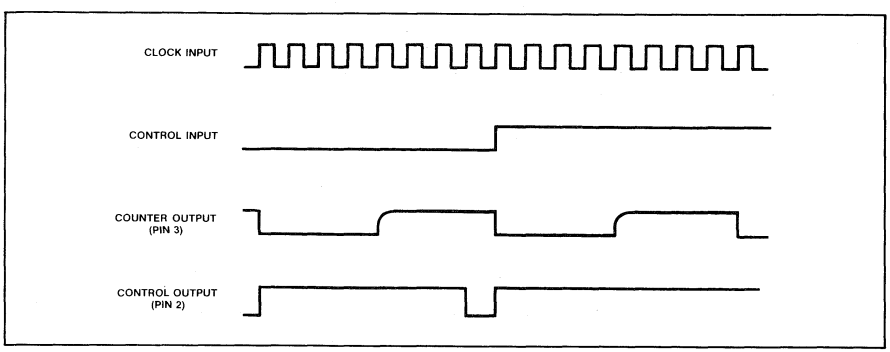


Fig.3 Timing diagram for SP8794

OPERATING NOTES

1. The device will normally be driven by capacitively coupling the clock inputs to the outputs of a 2-modulus divider. See Figs. 4 and 5. The maximum frequency of the device when used as a controller is limited by the internal delays and will not operate above 60MHz. When used as a prescaler the device will operate in excess of 120MHz, the maximum frequency being limited by saturation of the counter output stage.
2. The device is normally driven from the very fast edges of a 2-modulus divider and therefore there is no input slew rate problem.
3. The control input (pin 6) is TTL/CMOS compatible.
4. The counter output (pin 3) interfaces with CMOS/TTL by the addition of a pull-up resistor. For interconnecting to CMOS the output can be connected via a pull-up resistor to a supply which should not exceed 12V.
5. When used as a controller the circuit will self-oscillate in the absence of an input signal. This can be prevented by connecting a 47k resistor from pin 7 to ground, as shown in Fig. 5.
6. The control output which includes an internal 16k pull-down resistor, is ECL compatible and interfaced directly with, for example, the SP8695. See Fig. 5.
7. The propagation delays stated are with a 10k pull-down resistor which is the input pull-down of the SP8695. For interfacing with the SP8643/47 series, which have 4.3k input pull-downs, the propagation delays will be reduced.

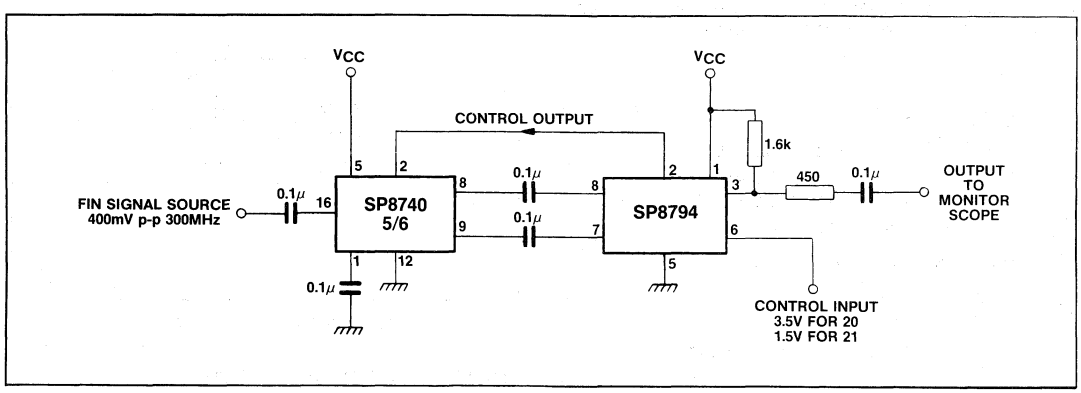


Fig.4 Test circuit

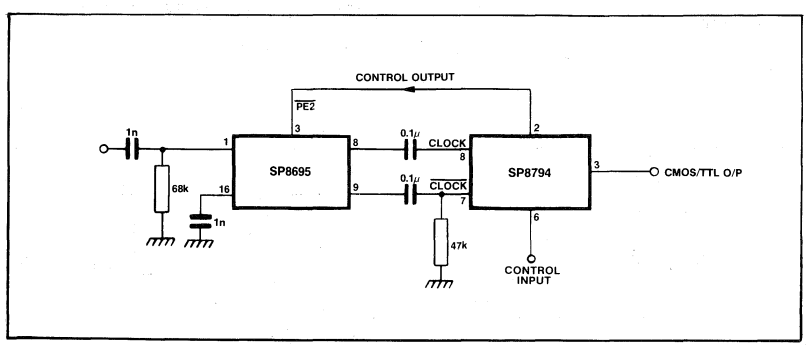


Fig.5 Typical interfacing to suppress self oscillation with no input signal

SP8802

3.3GHz ÷ 2 FIXED MODULUS DIVIDER

The SP8802A is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

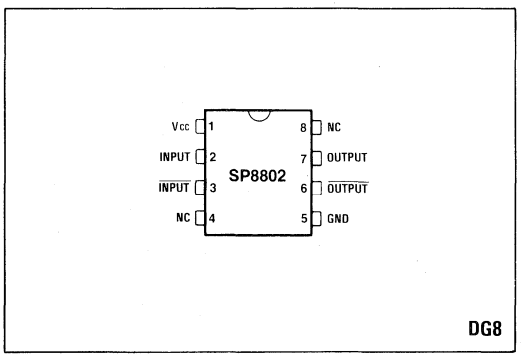


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Specified over the Full Military Temperature Range
- Low Power Dissipation 420mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8802 A DG
SP8802 AC DG

THERMAL CHARACTERISTICS

θ_{JA} = 150°C/W

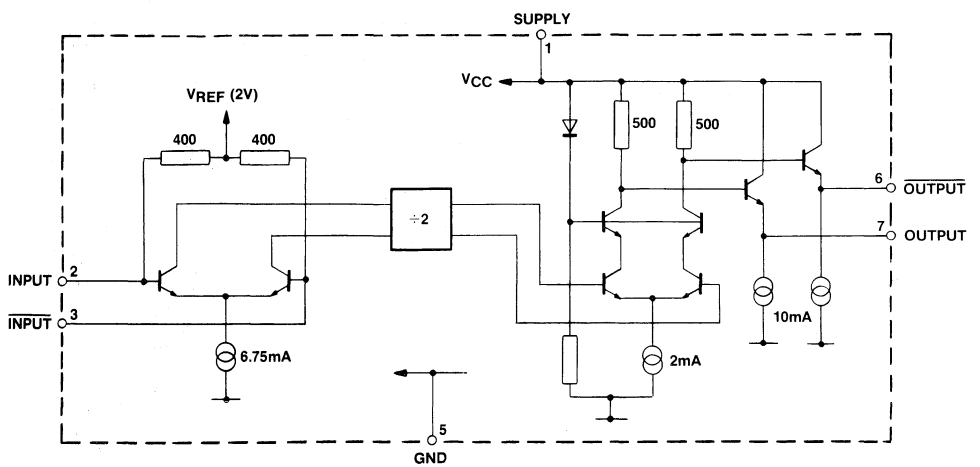


Fig.2 SP8802A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = −55°C to +125°C, V_{CC} = 4.75V to 5.25V (See Note)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		84	100	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.3GHz				400	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 1000MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 3GHz	6,7		0.25		V p-p	V_{CC} = 5V load as Fig.4

NOTE
Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{amb} > 100°C.

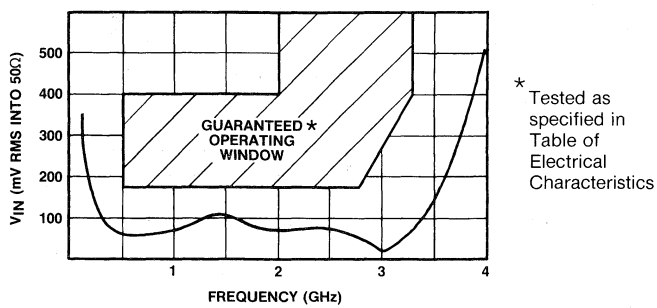


Fig.3 Typical input sensitivity

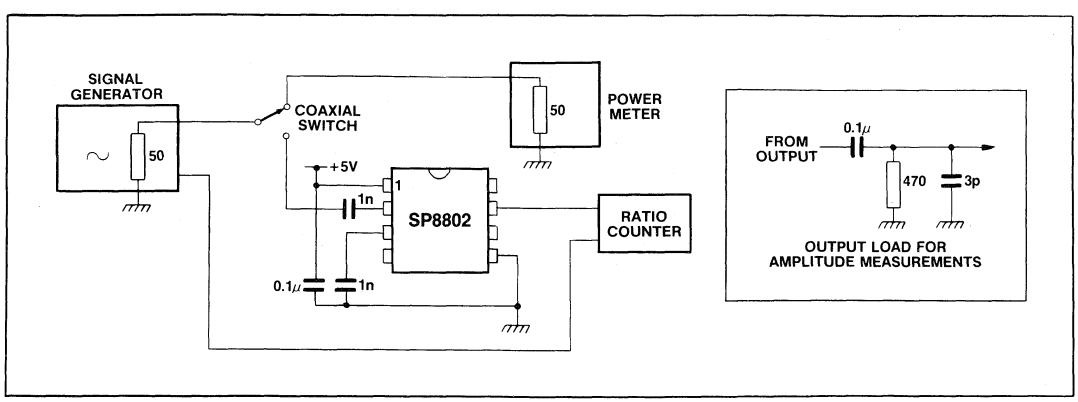


Fig.4 Test circuit

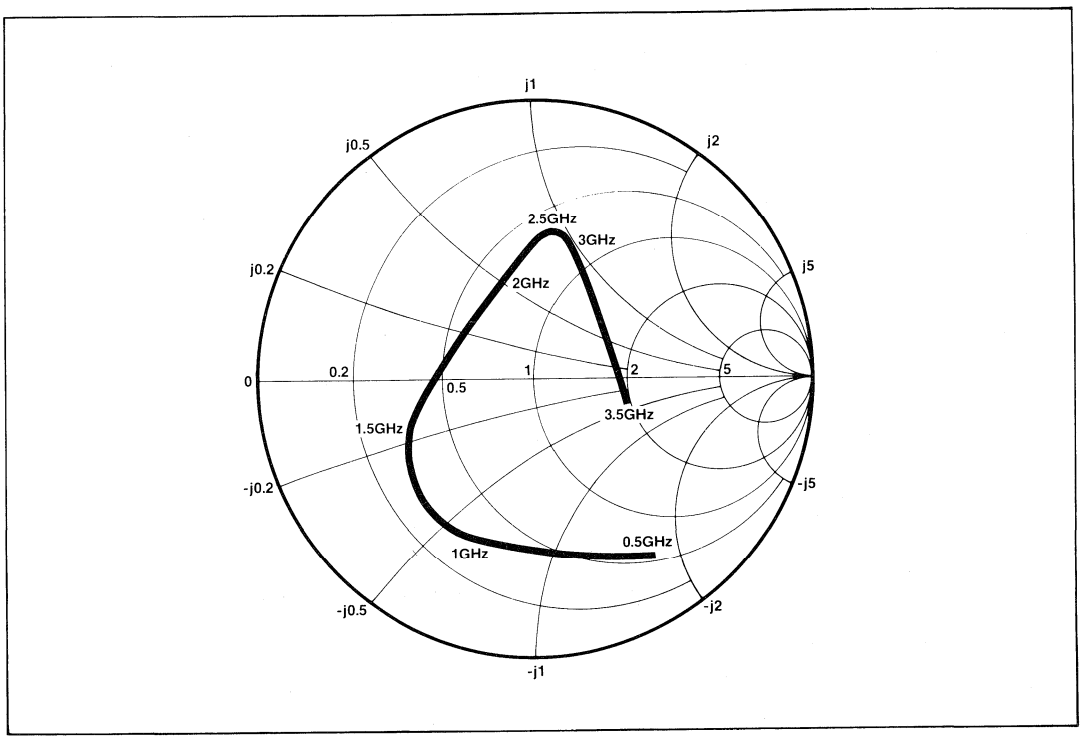


Fig.5 Typical input impedance

SP8804

3.3GHz ÷ 4 FIXED MODULUS DIVIDER

The SP8804A is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

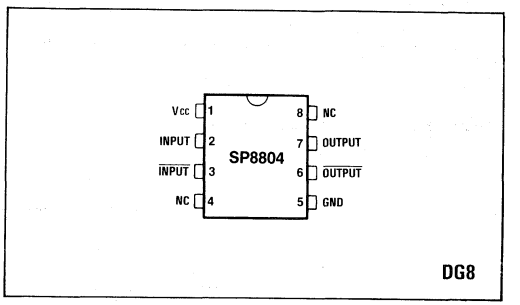


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Specified over the Full Military Temperature Range
- Low Power Dissipation 370mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8804 A DG
SP8804 AC DG

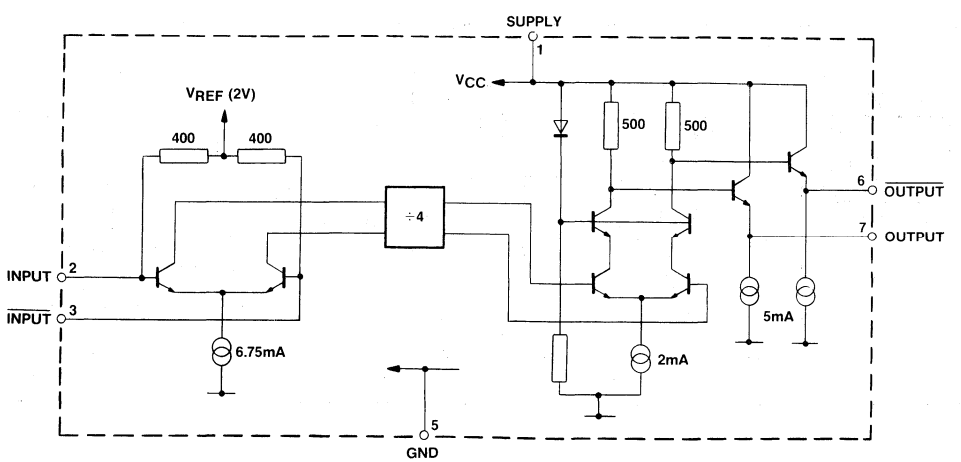


Fig.2 SP8804A block diagram

ELECTRICAL CHARACTERISTICS

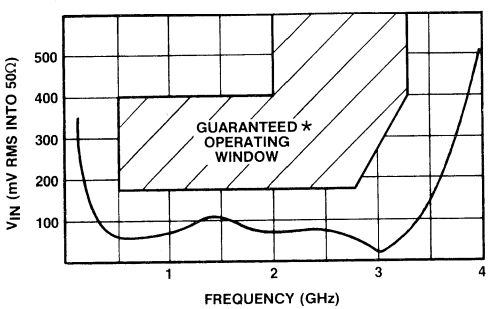
Test conditions (unless otherwise stated):
T_{amb} = -55°C to +125°C, V_{CC} = 4.75V to 5.25V (See Note)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		74	90	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.3GHz				100	mV	system, see Fig. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 1000MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 3GHz	6,7		0.35		V p-p	V_{CC} = 5V load as Fig.4

NOTE
Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{amb} >105°C.

THERMAL CHARACTERISTICS

θ_{JA} = 150°C/W



★ Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

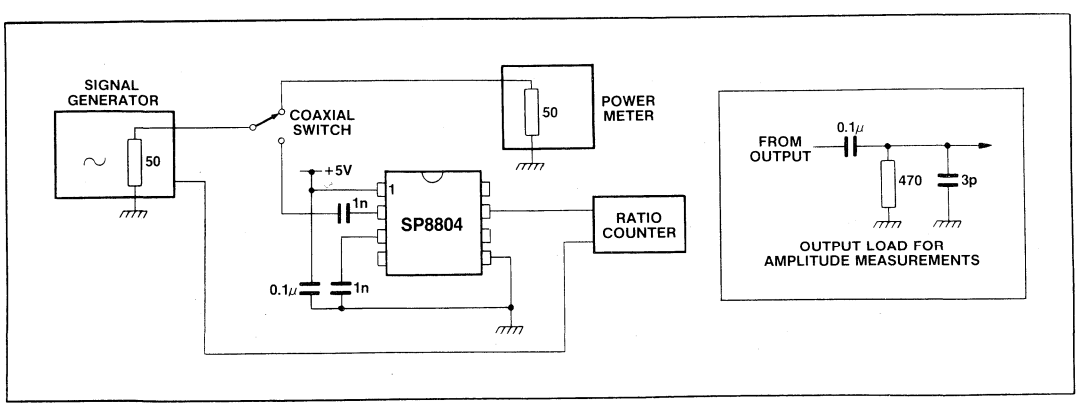


Fig.4 Test circuit

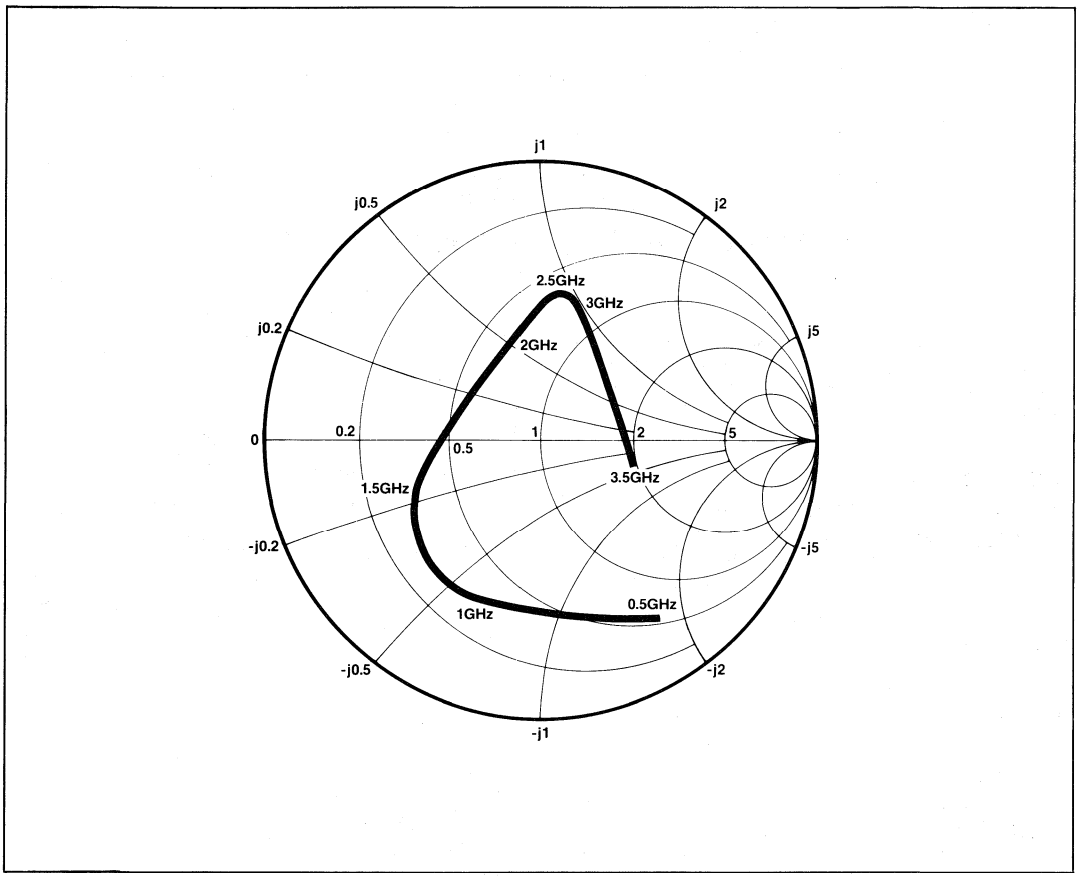


Fig.5 Typical input impedance

SP8808

3.3GHz ÷ 8 FIXED MODULUS DIVIDER

The SP8808A is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

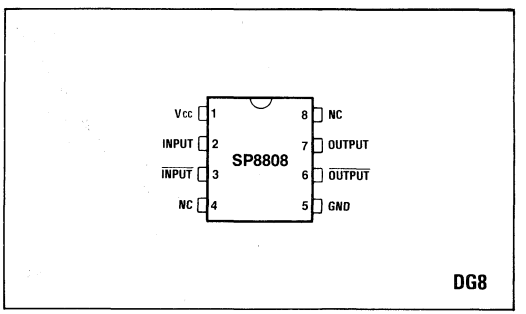


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Specified over the Full Military Temperature Range
- Low Power Dissipation 345mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8808 A DG
SP8808 AC DG

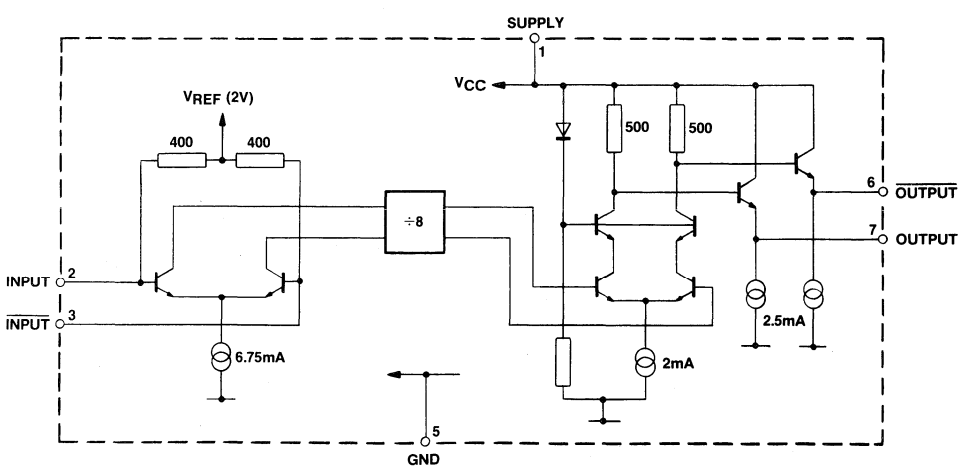


Fig.2 SP8808A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = -55°C to +125°C, V_{CC} = 4.75V to 5.25V (See Note)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		69	85	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.3GHz				400	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 1000MHz	6,7	0.8	1		V p-p	V_{CC} = 5V
Output voltage with f_{in} = 3GHz	6,7		0.4		V p-p	V_{CC} = 5V load as Fig.4

NOTE

Devices must be used with a suitable heat sink to maintain chip temperature below 175°C when operating at T_{amb} >110°C.

THERMAL CHARACTERISTICS

θ_{JA} = 150°C/W

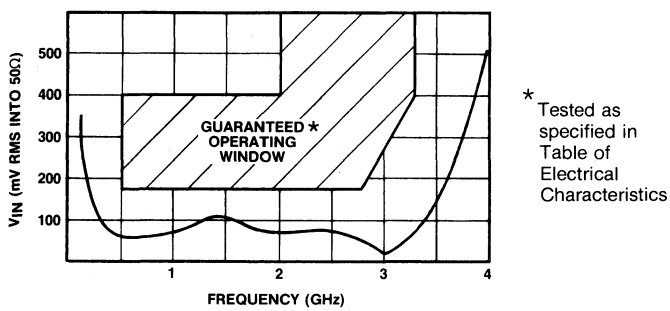


Fig.3 Typical input sensitivity

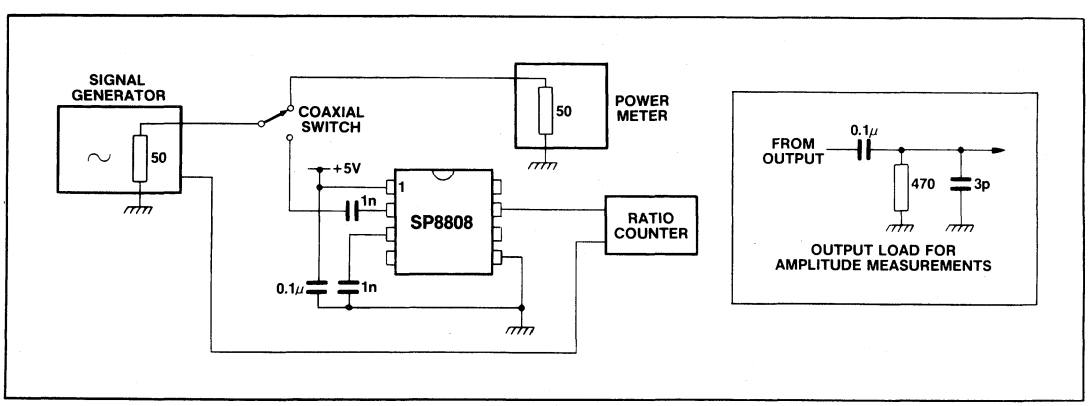


Fig.4 Test circuit

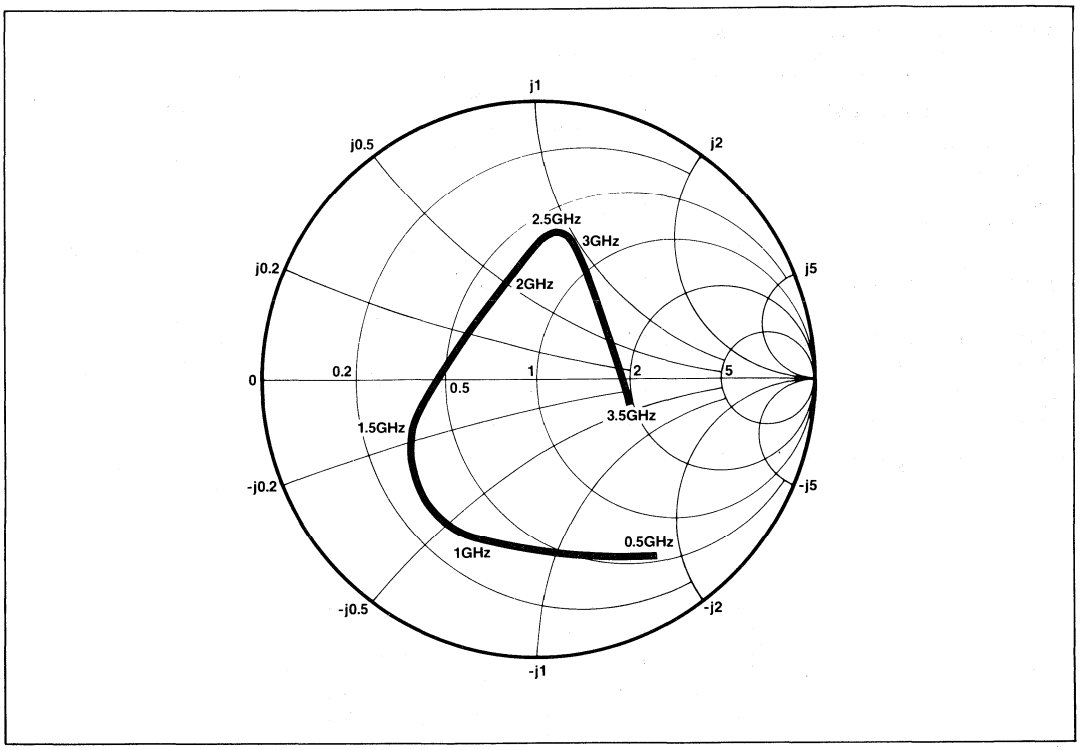


Fig.5 Typical input impedance

SP8812A1

1.6GHz ÷ 2 PRESCALER

(Supersedes December 1989 Edition)

The SP8812A1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.6GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 250mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -55°C to + 125°C

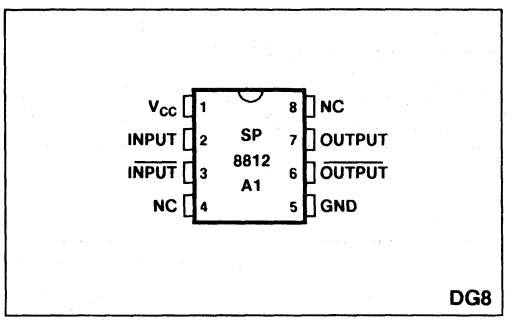


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8812 A1 DG

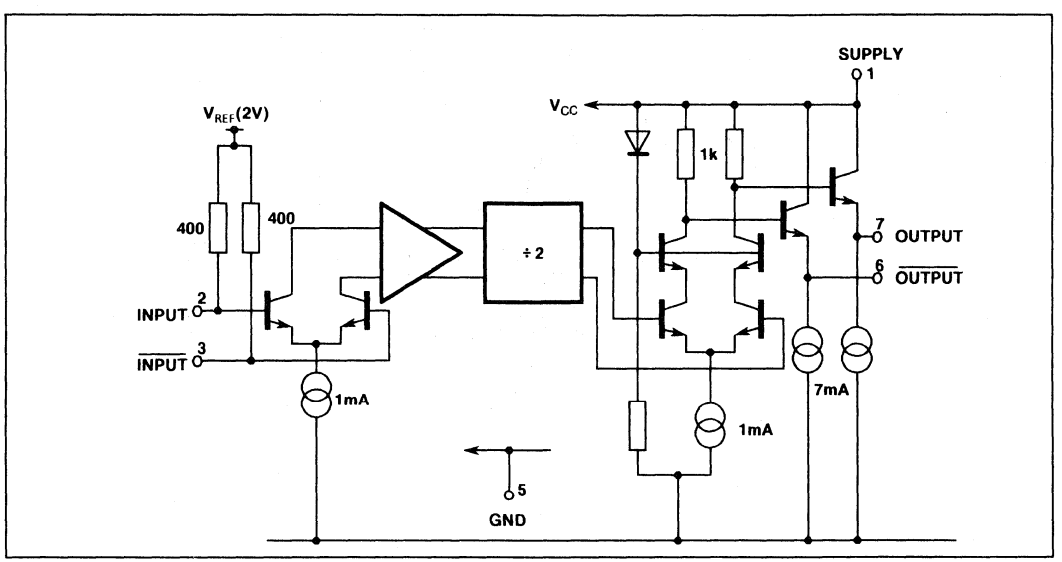


Fig 2 SP8812A1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to5.25V
Temperature:T_{amb} = –55°C to +125°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		50	65	mA	
Input Sensitivity, 500MHz to 1600MHz	2, 3			150	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50		Ω	
			2		pF	
Output voltage with f_{IN} = 500MHz	6, 7	0.5	1		Vp-p	
Output voltage with f_{IN} = 1600MHz	6, 7		0.13		Vp-p	

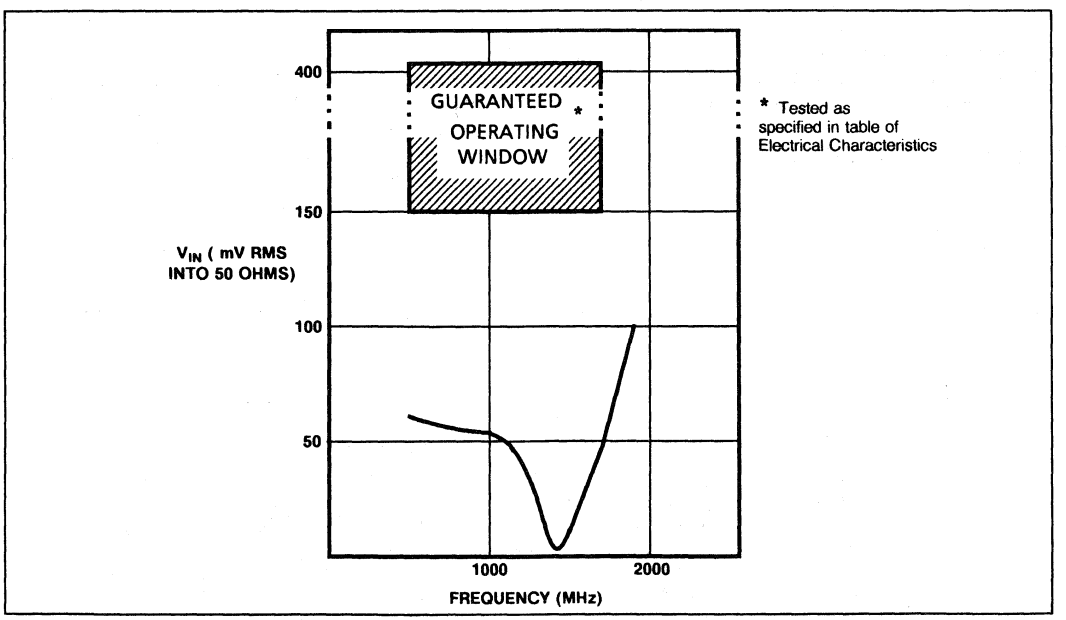


Fig.3 Typical input sensitivity

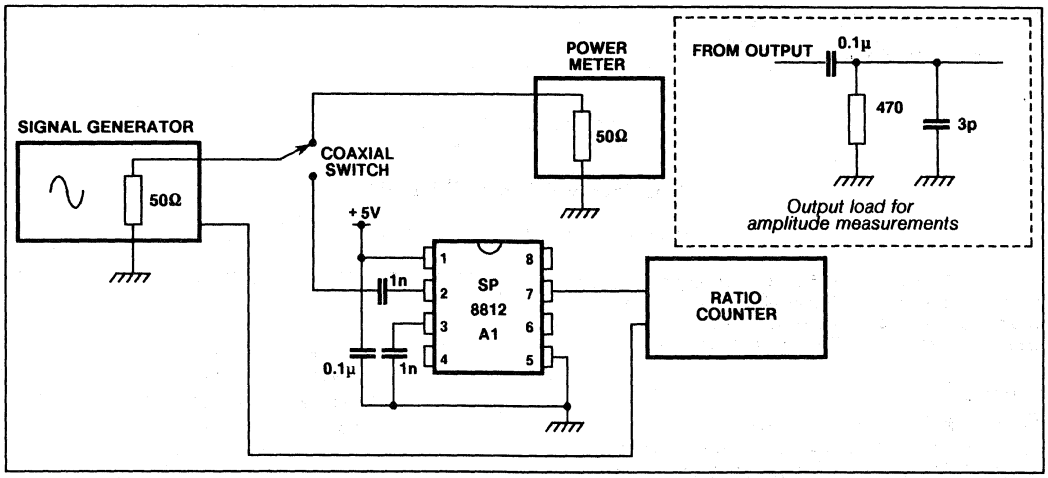


Fig.4 Test circuit

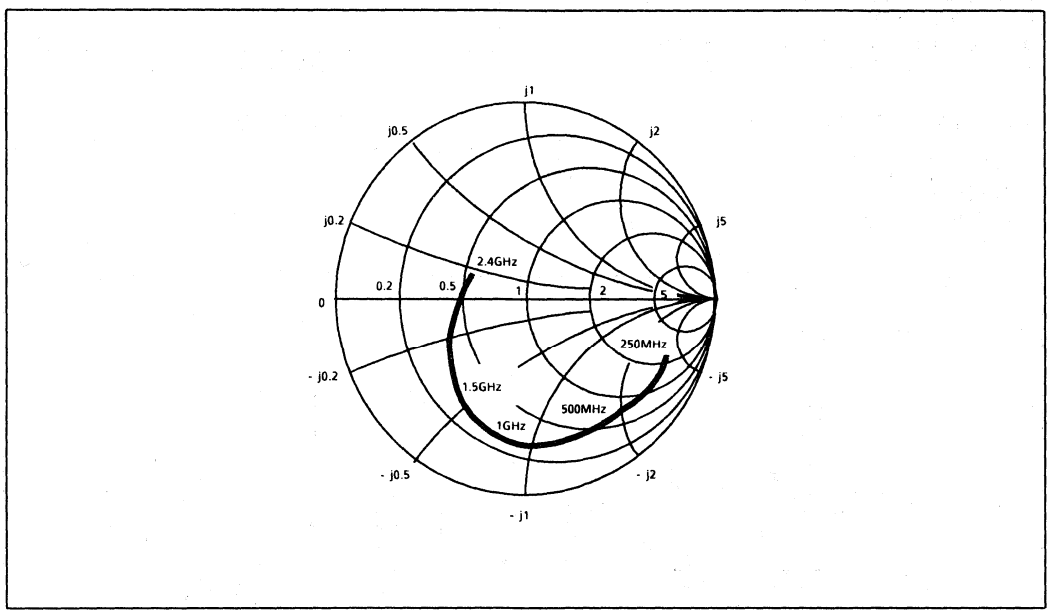


Fig.5 Typical input impedance, normalised to 50Ω

SP8812B1

2.0GHz ÷ 2 PRESCALER

(Supersedes December 1989 Edition)

The SP8812B1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2.0GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 250mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -40°C to + 85°C

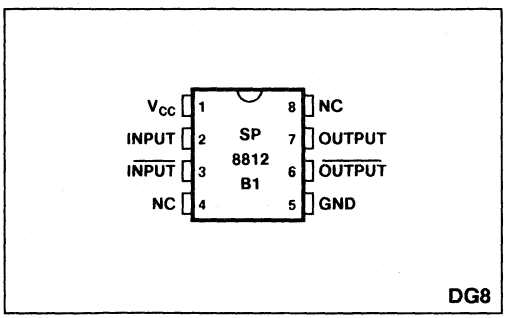


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8812 B1 DG

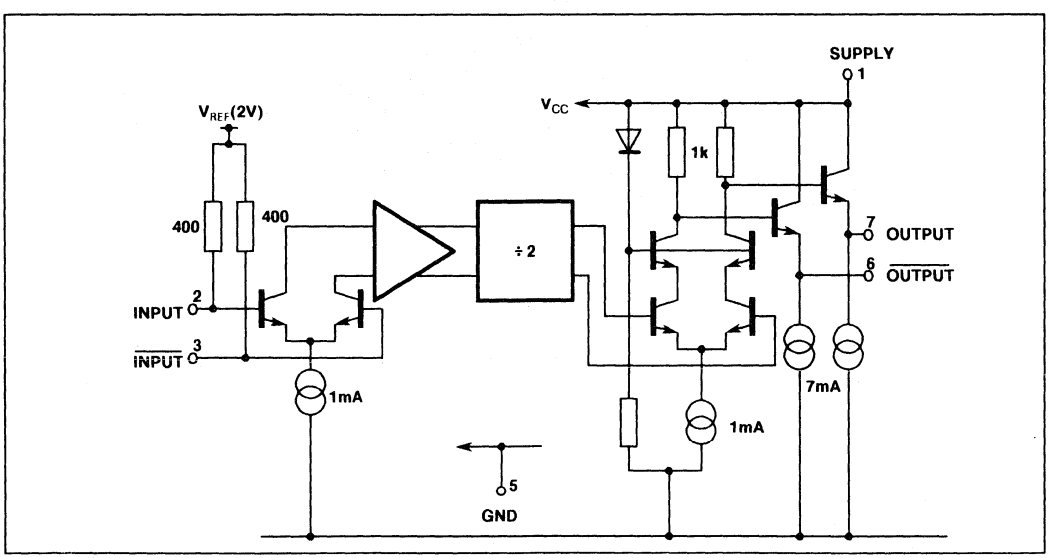


Fig 2 SP8812B1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		50	65	mA	
Input Sensitivity, 500MHz to 2000MHz	2, 3			150	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	
Output voltage with f_{IN} = 500MHz	6, 7	0.5	1		Vp-p	
Output voltage with f_{IN} = 2000MHz	6, 7		0.13		Vp-p	

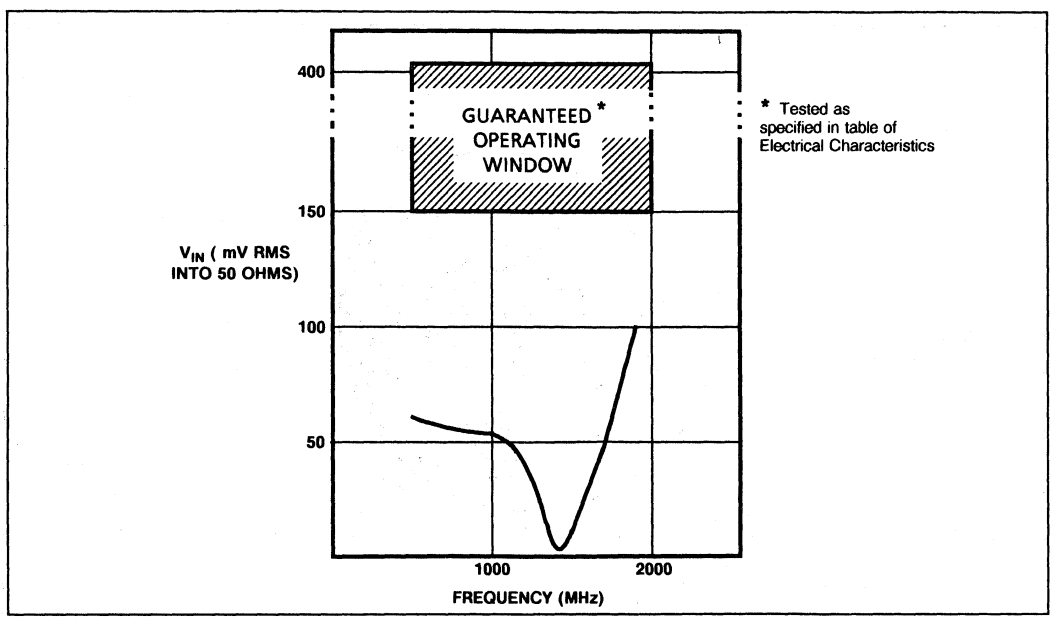


Fig.3 Typical input sensitivity

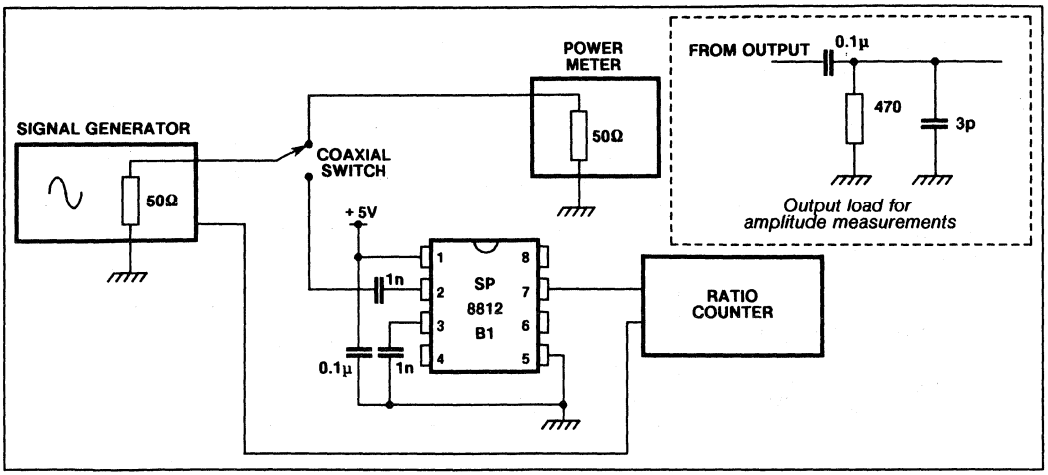


Fig.4 Test circuit

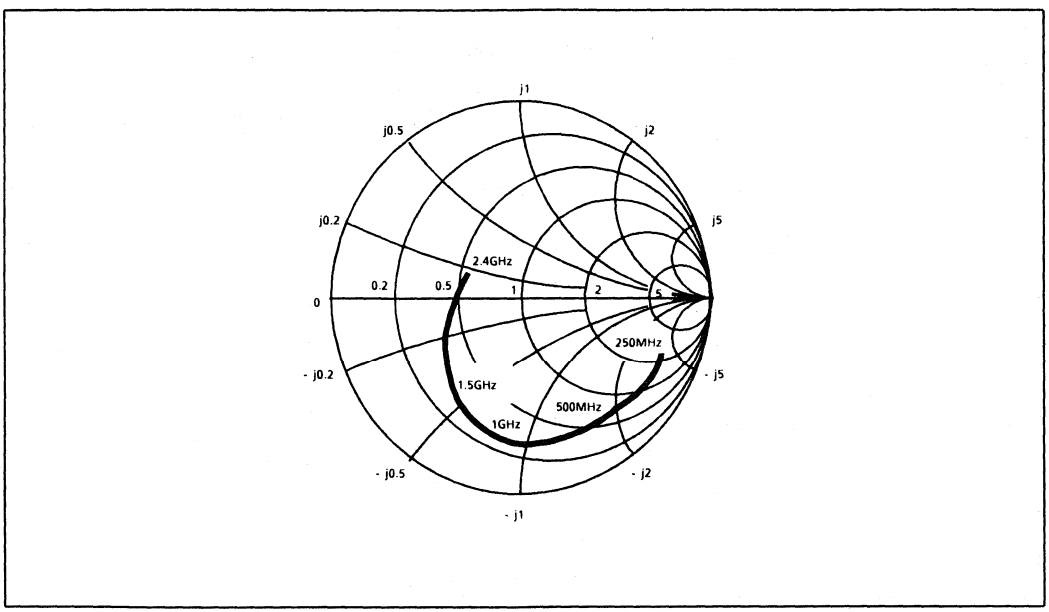


Fig.5 Typical input impedance, normalised to 50Ω

SP8814A1

1.6GHz ÷ 4 PRESCALER

(Supersedes December 1989 Edition)

The SP8814A1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.6GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 220mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -55°C to + 125°C

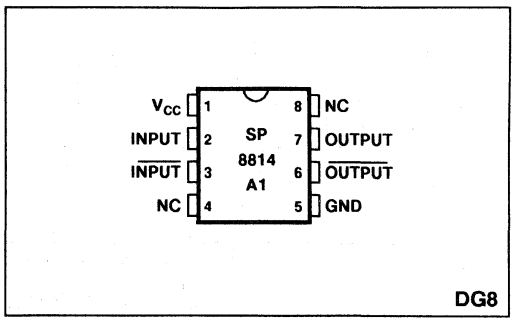


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8814 A1 DG

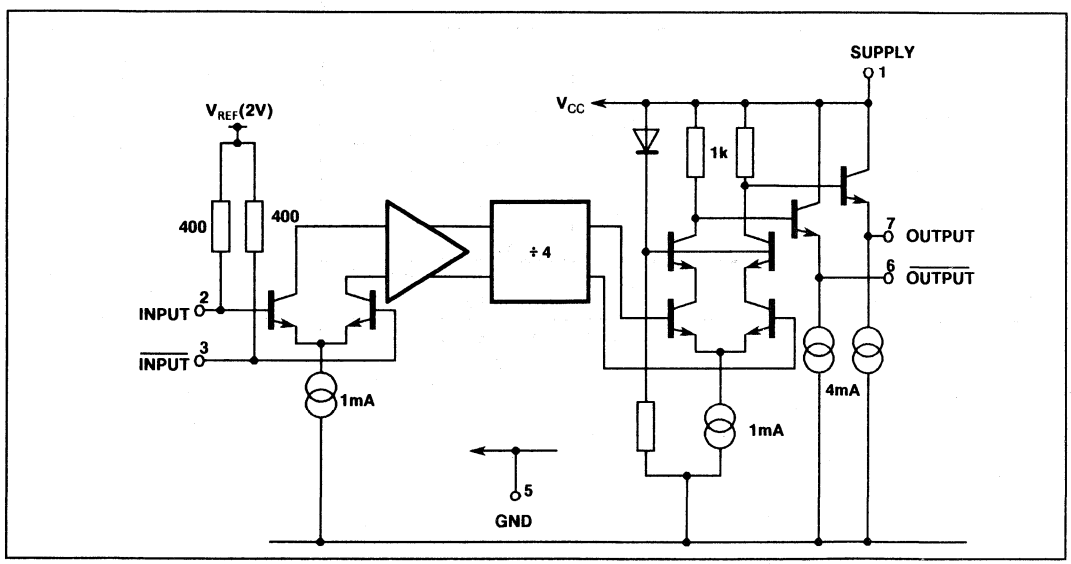


Fig 2 SP8814A1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –55°C to +125°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		44	52	mA	
Input Sensitivity, 500MHz to 1600MHz	2, 3			150	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	
Output voltage with f_{IN} = 500MHz	6, 7	0.5	1		Vp-p	
Output voltage with f_{IN} = 1600MHz	6, 7		0.13		Vp-p	

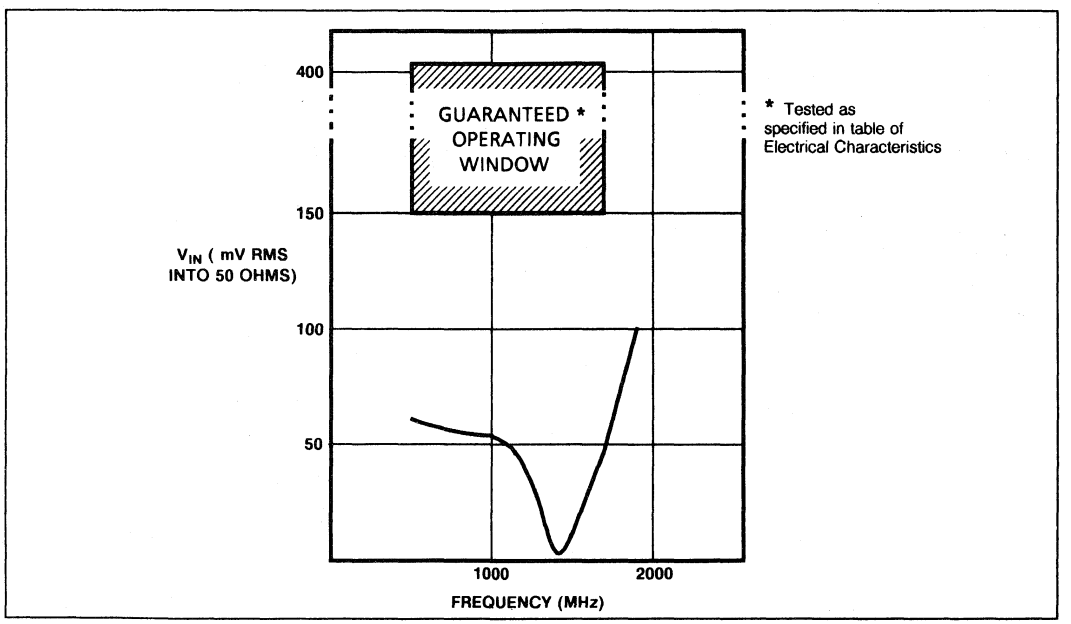


Fig.3 Typical input sensitivity

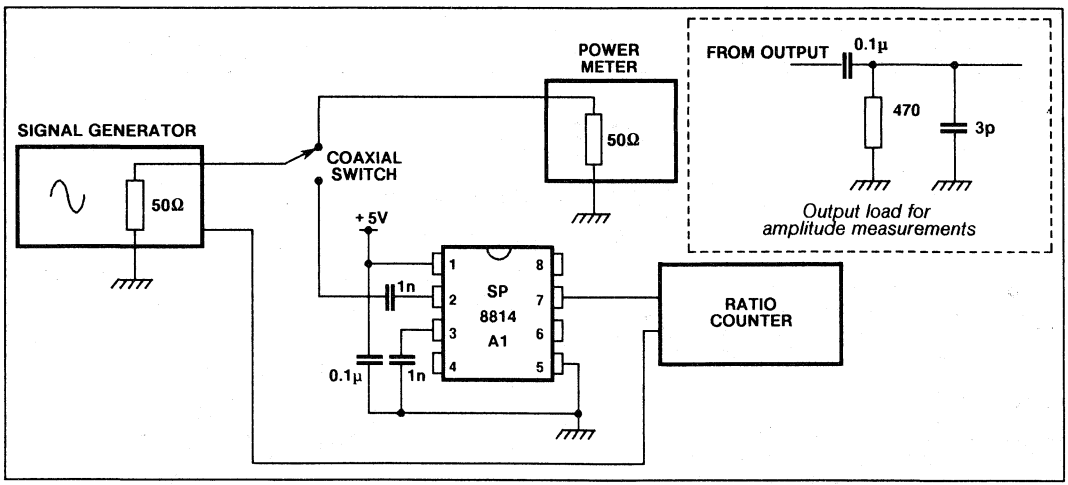


Fig.4 Test circuit

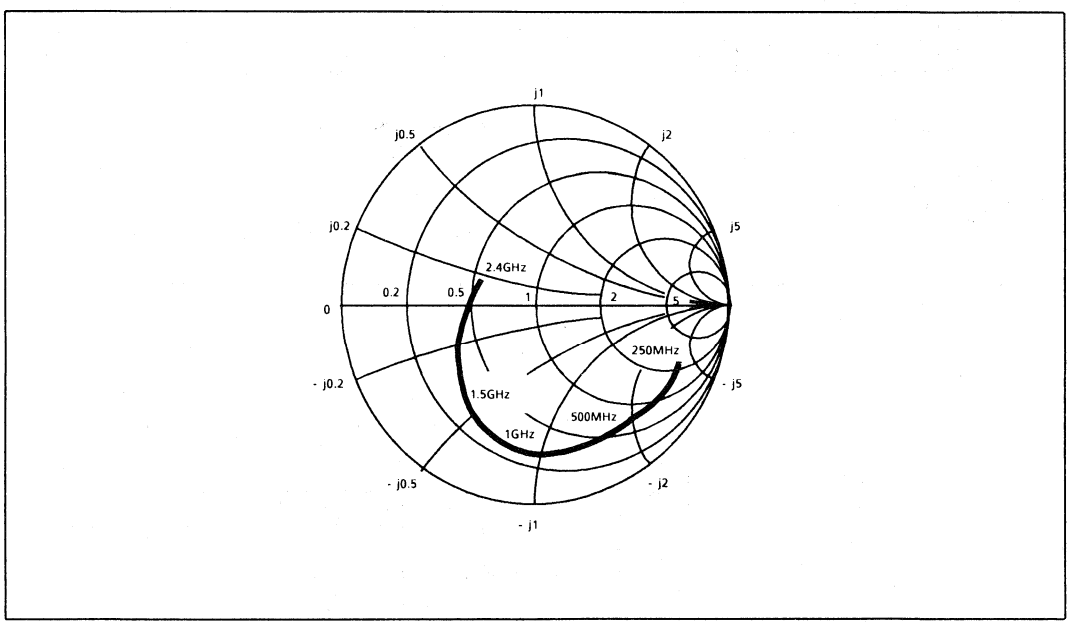


Fig.5 Typical input impedance, normalised to 50Ω

SP8814B1

2.0GHz ÷ 4 PRESCALER

(Supersedes December 1989 Edition)

The SP8814B1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2.0GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 220mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -40°C to + 85°C

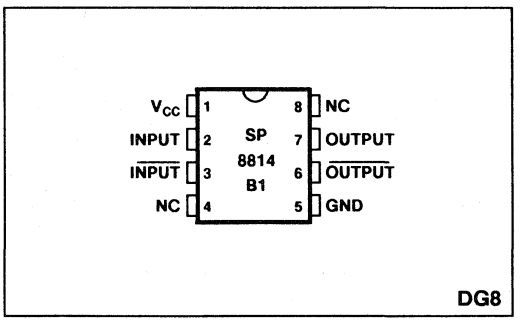


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8814 B1 DG

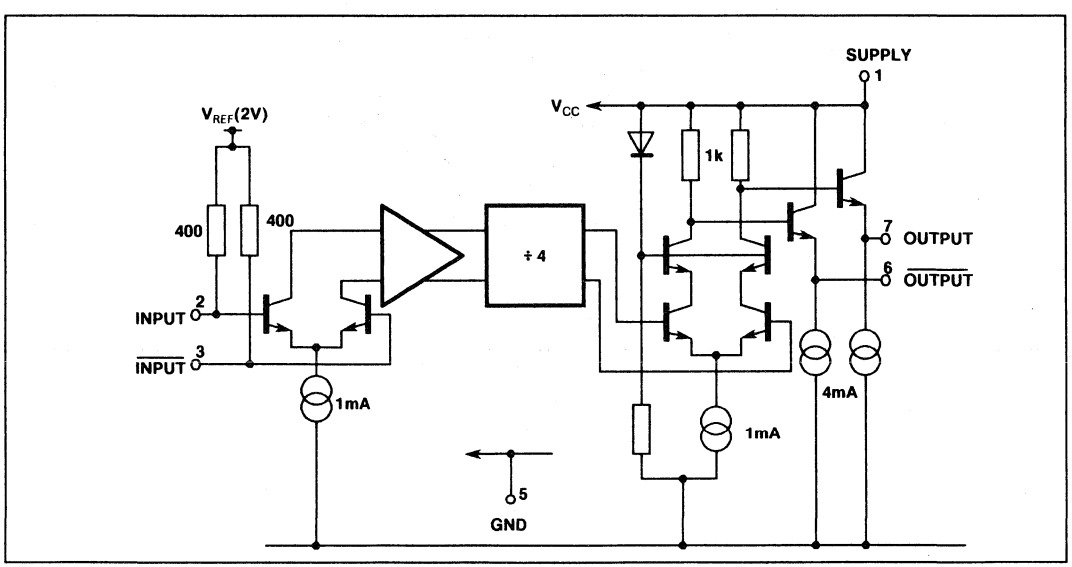


Fig 2 SP8814B1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		44	52	mA	
Input Sensitivity, 500MHz to 2000MHz	2, 3			150	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50		Ω	
			2		pF	
Output voltage with f_{IN} = 500MHz	6, 7	0.5	1		Vp-p	
Output voltage with f_{IN} = 2000MHz	6, 7		0.13		Vp-p	

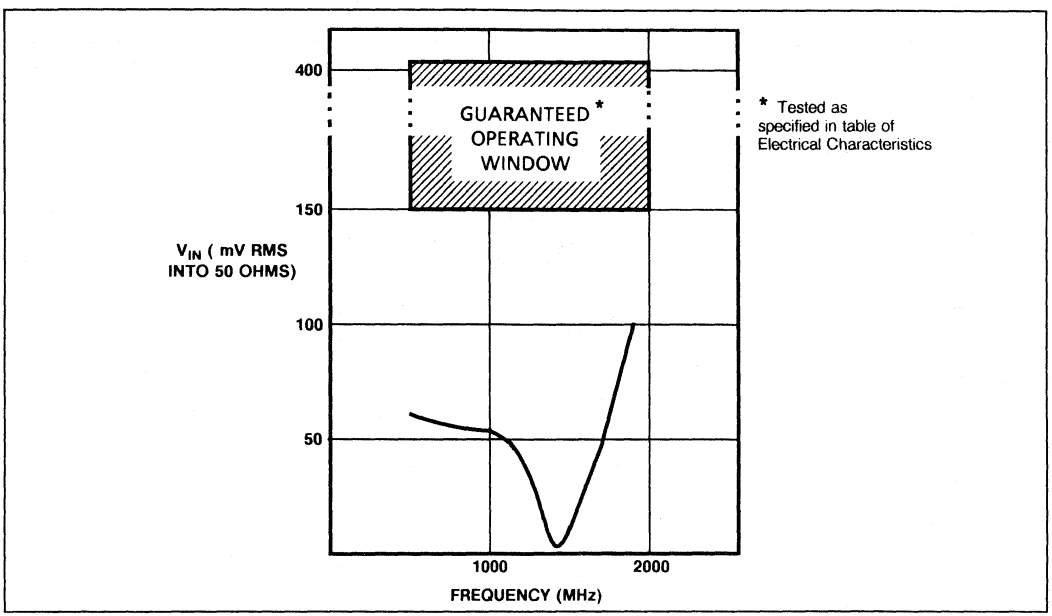


Fig.3 Typical input sensitivity

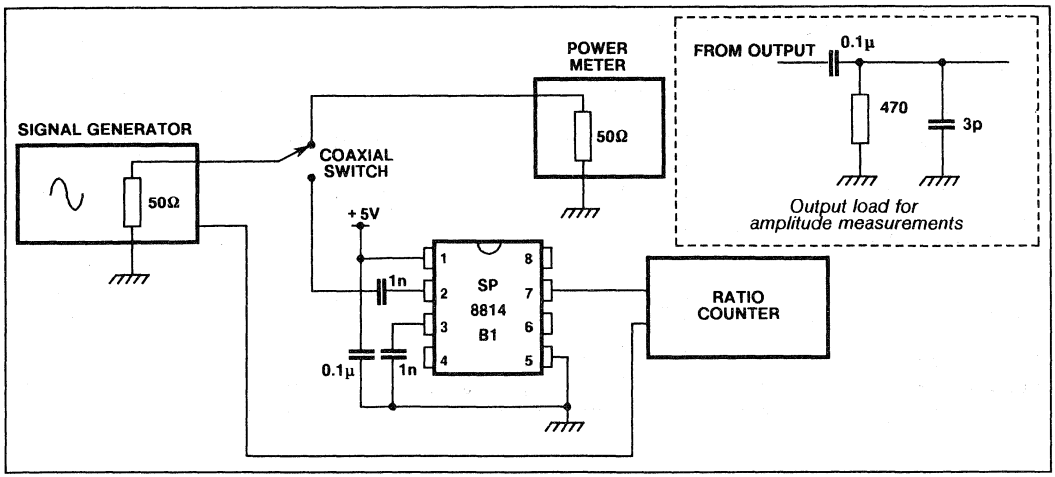


Fig.4 Test circuit

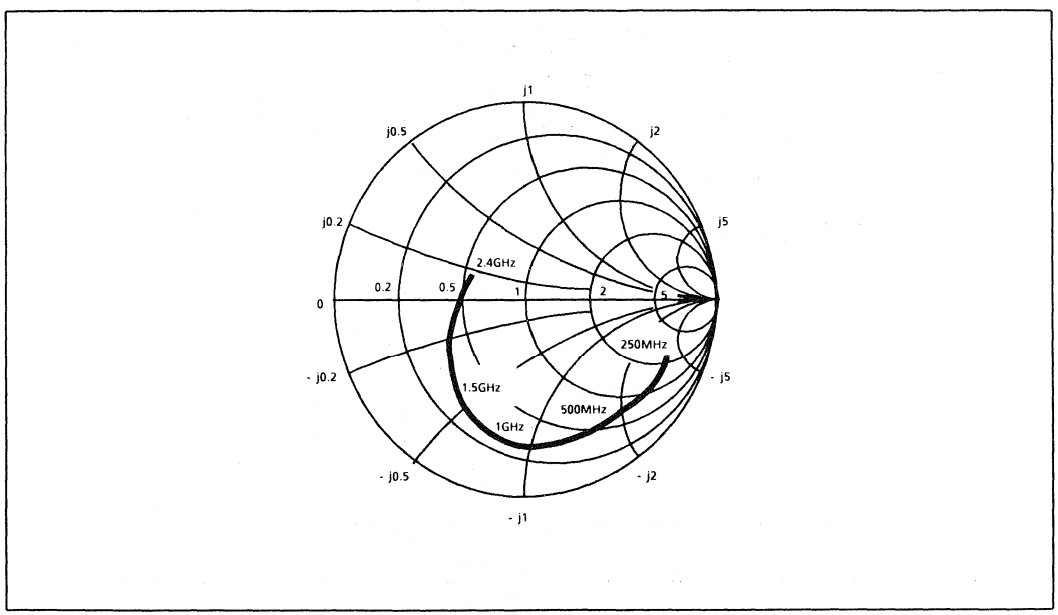


Fig.5 Typical input impedance, normalised to 50Ω

SP8818A1

1.6GHz ÷ 8 PRESCALER

(Supersedes December 1989 Edition)

The SP8818A1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.6GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 200mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -55°C to + 125°C

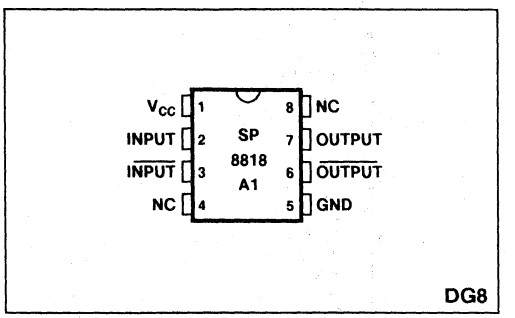


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8818 A1 DG

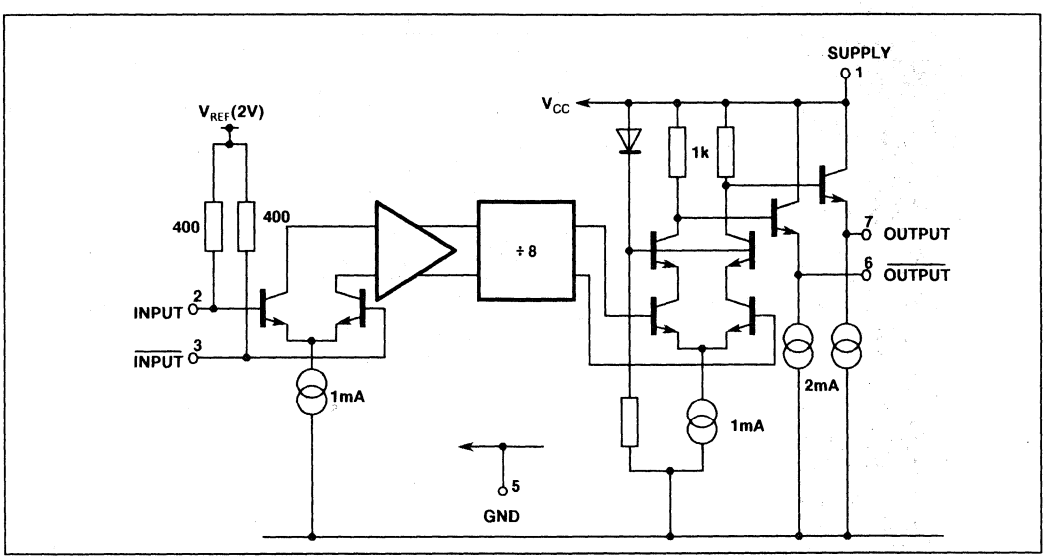


Fig 2 SP8818A1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –55°C to +125°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		40	48	mA	
Input Sensitivity, 500MHz to 1600MHz	2, 3			150	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50		Ω	
			2		pF	
Output voltage with f_{IN} = 500MHz	6, 7	0.5	1		Vp-p	
Output voltage with f_{IN} = 1600MHz	6, 7		0.13		Vp-p	

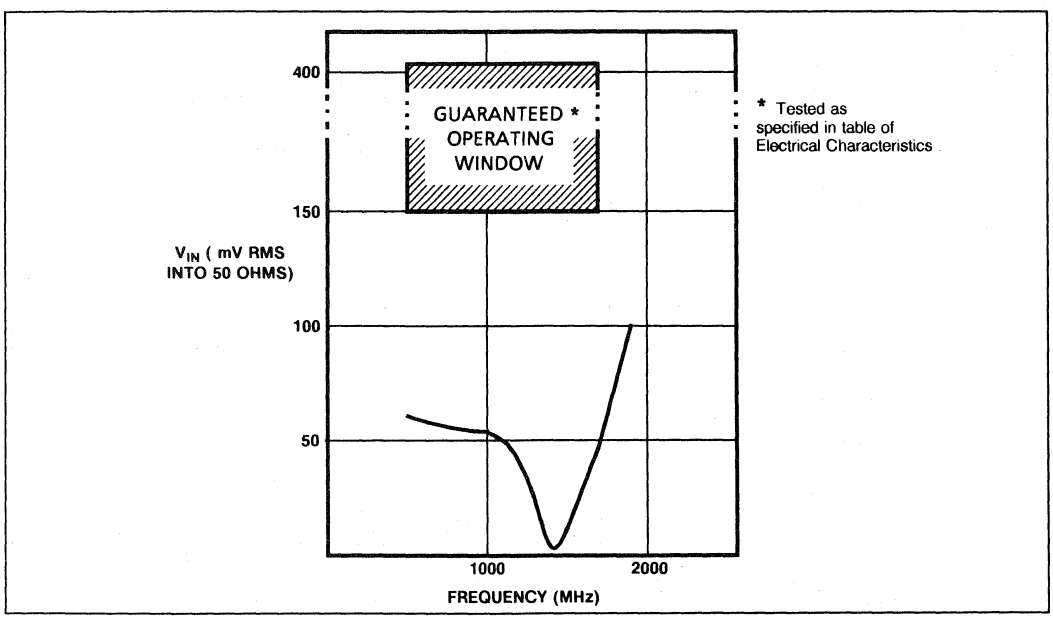


Fig.3 Typical input sensitivity

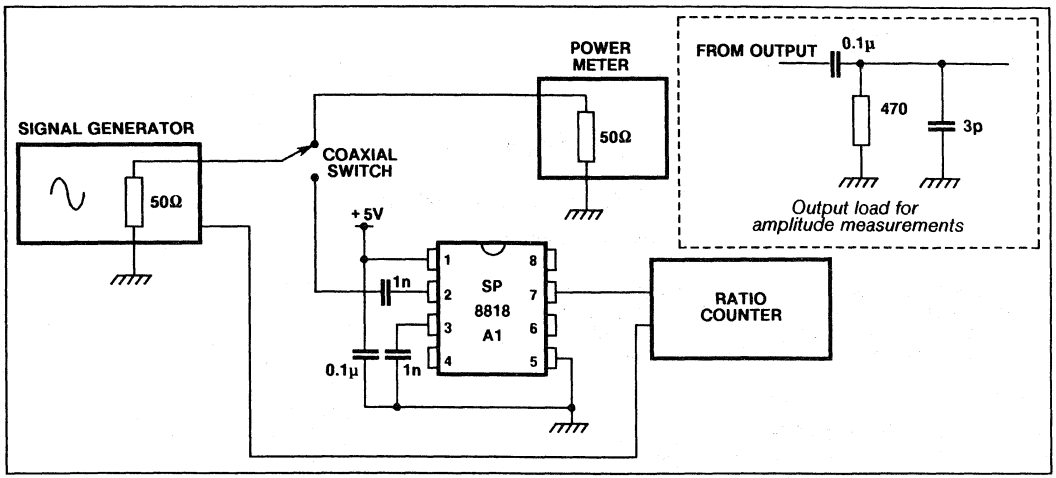


Fig.4 Test circuit

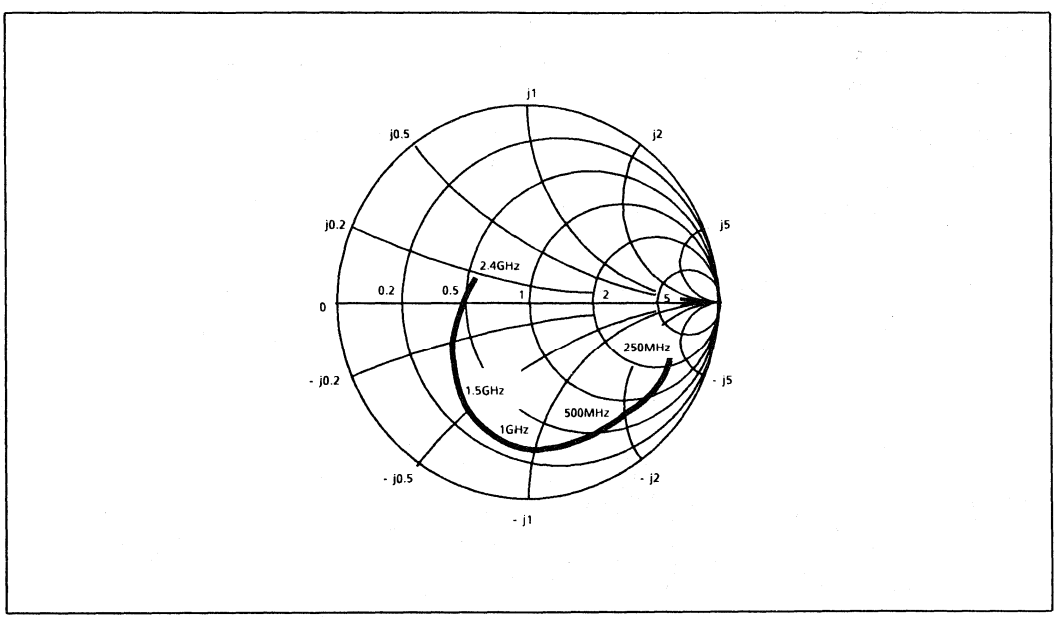


Fig.5 Typical input impedance, normalised to 50Ω

SP8818B1

2.0GHz ÷ 8 PRESCALER

(Supersedes December 1989 Edition)

The SP8818B1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2.0GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 200mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -40°C to + 85°C

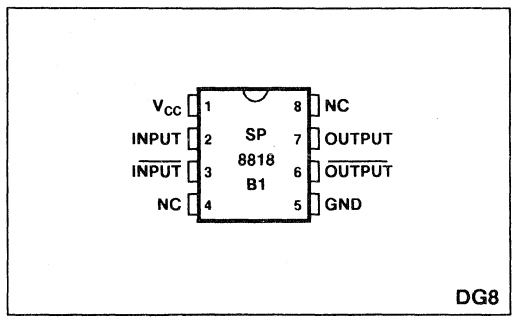


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8818 B1 DG

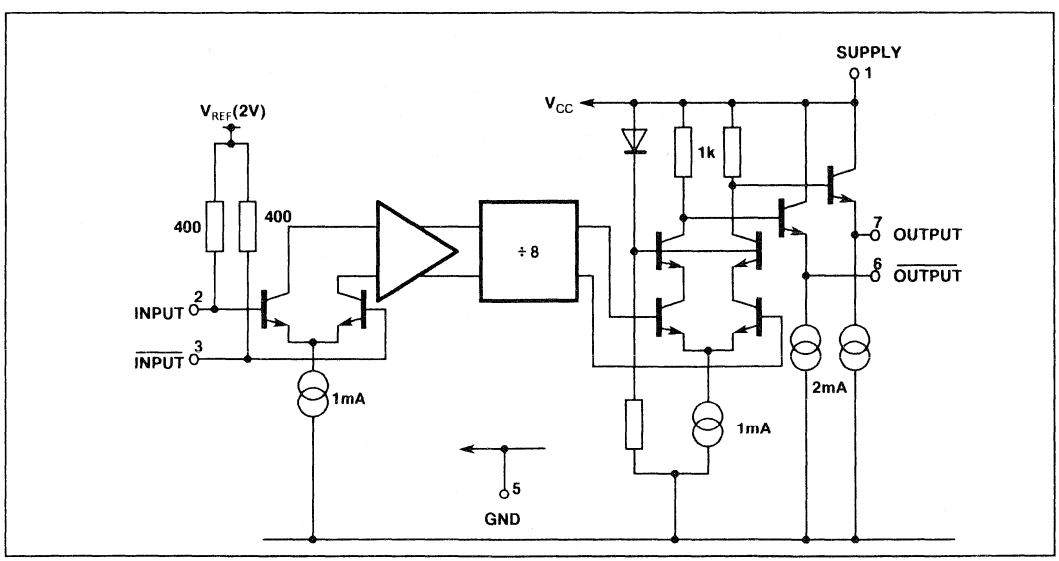


Fig 2 SP8818B1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		40	48	mA	
Input Sensitivity, 500MHz to 2000MHz	2, 3			150	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50		Ω	
			2		pF	
Output voltage with f_{IN} = 500MHz	6, 7	0.5	1		Vp-p	
Output voltage with f_{IN} = 2000MHz	6, 7		0.13		Vp-p	

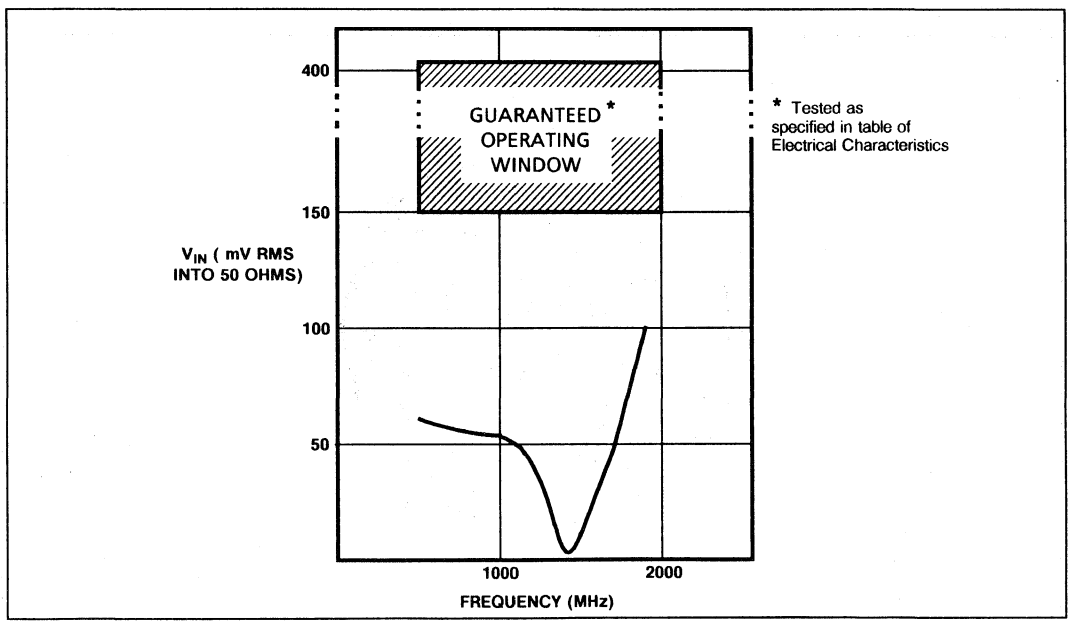


Fig.3 Typical input sensitivity

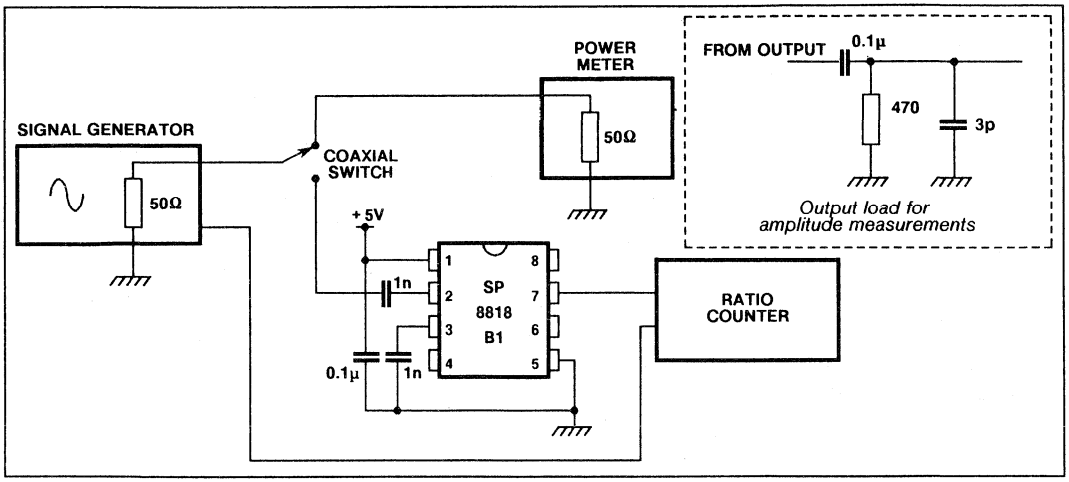


Fig.4 Test circuit

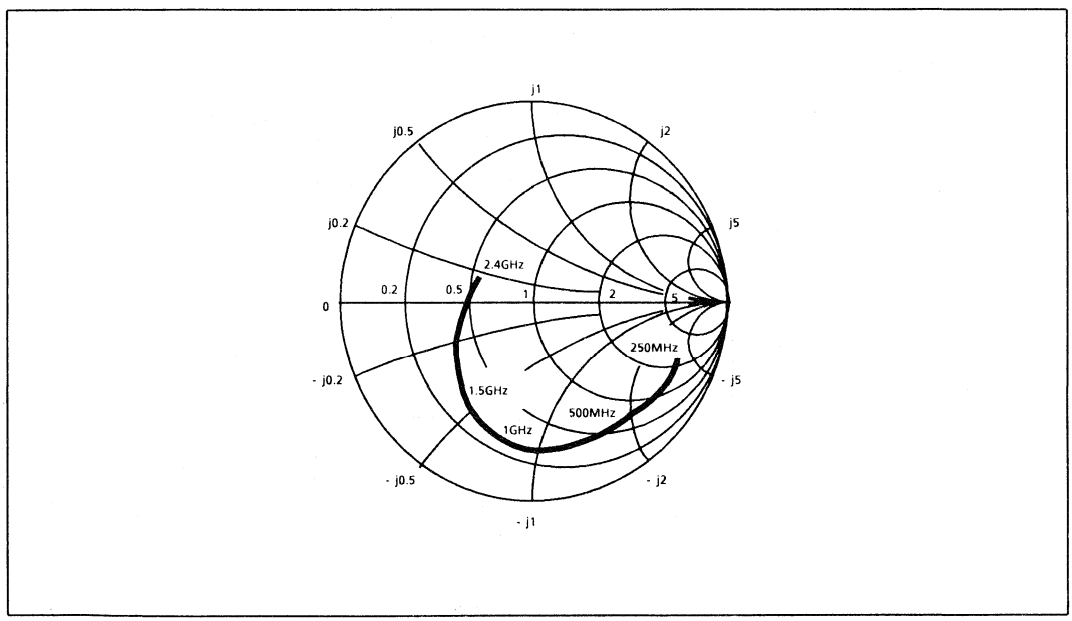


Fig.5 Typical input impedance, normalised to 50Ω

SP8822A1

1.3GHz ÷ 2 PRESCALER

(Supersedes December 1989 Edition)

The SP8822A1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.3GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 215mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -55°C to + 125°C

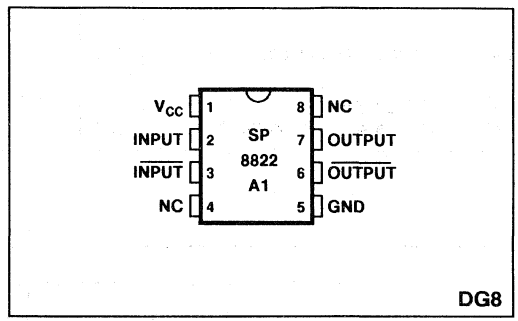


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8822 A1 DG

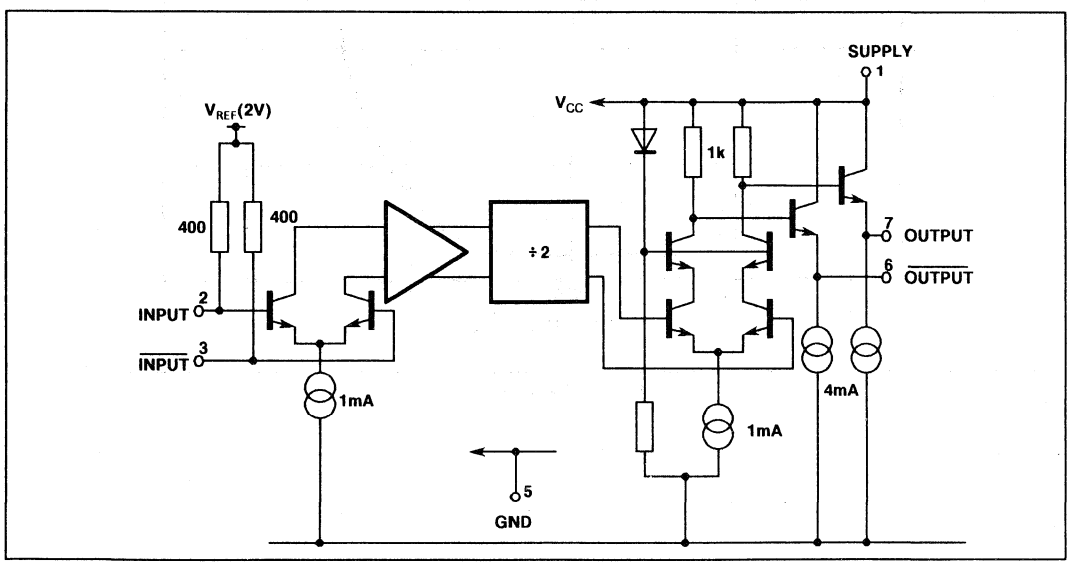


Fig 2 SP8822A1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –55°C to +125°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		43	53	mA	
Input Sensitivity, 200MHz to 1300MHz	2, 3			120	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	See Fig. 5
Output voltage with f_{IN} = 200MHz	6, 7	0.6	1		Vp-p	
Output voltage with f_{IN} = 1300MHz	6, 7		0.2		Vp-p	

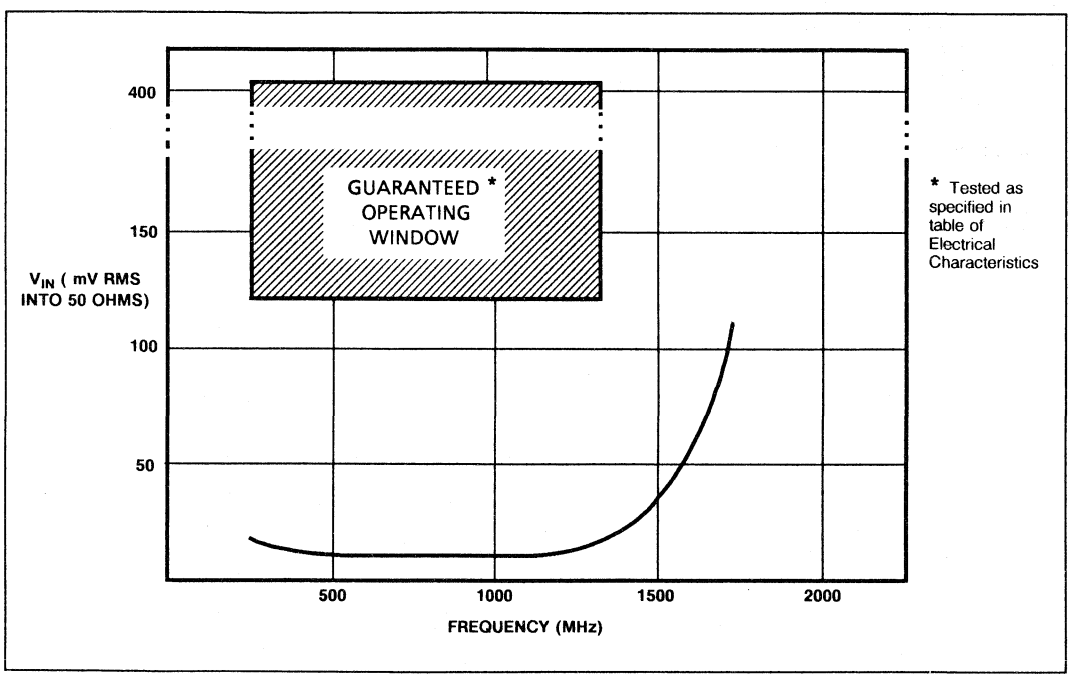


Fig.3 Typical input sensitivity

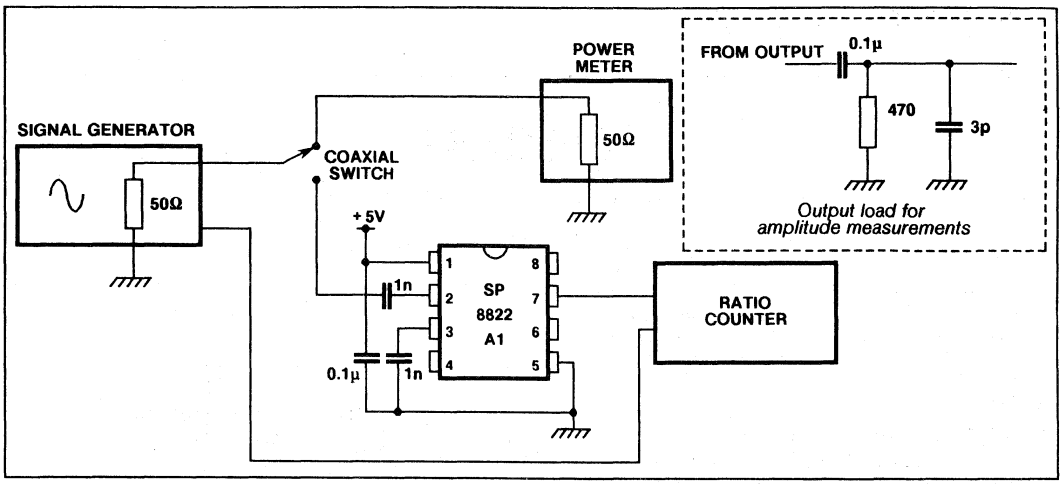


Fig.4 Test circuit

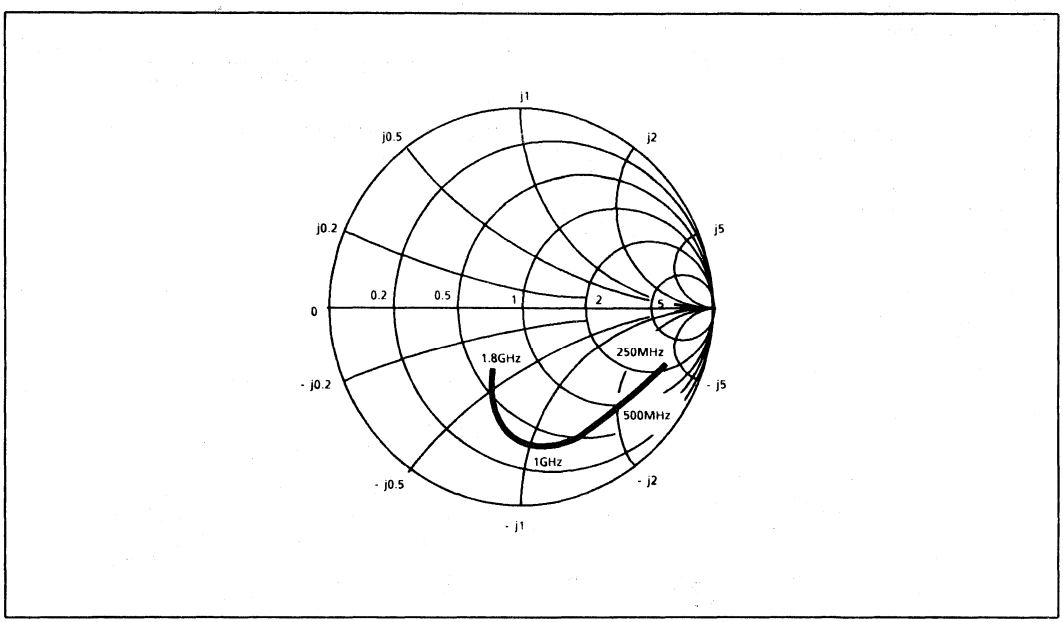


Fig.5 Typical input impedance, normalised to 50Ω

SP8822B1

1.6GHz ÷ 2 PRESCALER

(Supersedes December 1989 Edition)

The SP8822B1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.6GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 215mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -40°C to +85°C

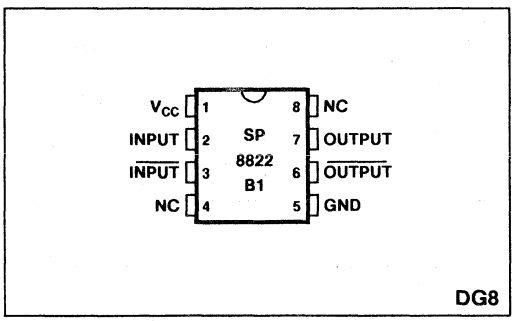


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8822 B1 DG

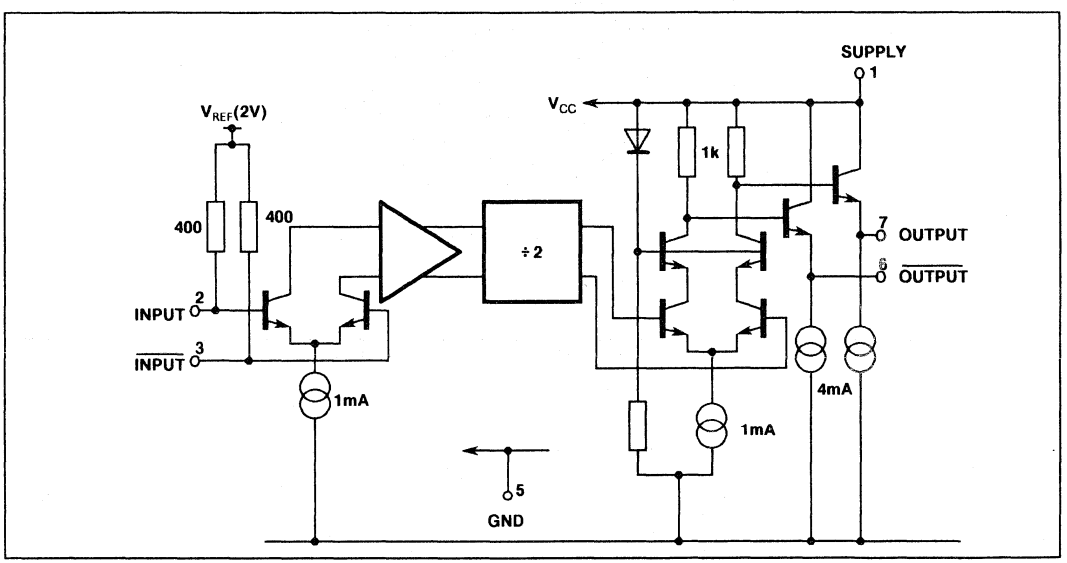


Fig 2 SP8822B1 Block Diagram

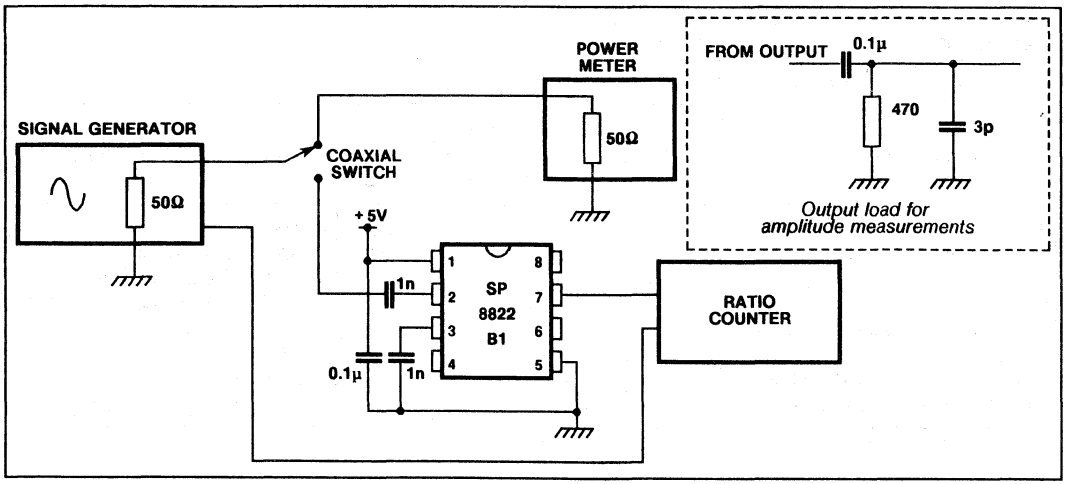


Fig.4 Test circuit

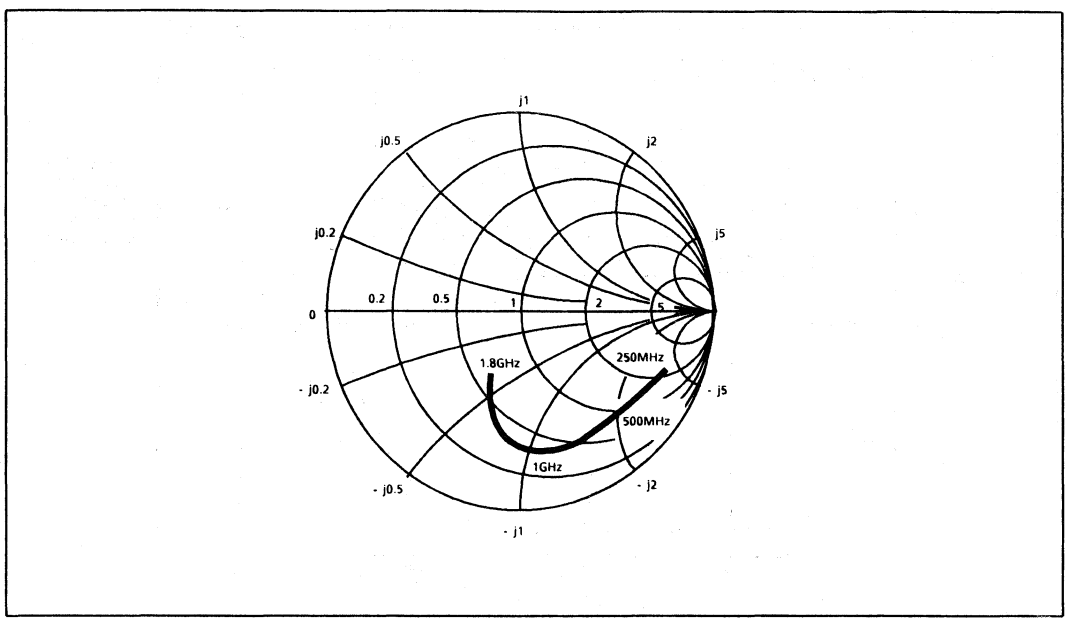


Fig.5 Typical input impedance, normalised to 50Ω

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		43	53	mA	
Input Sensitivity, 200MHz to 1600MHz	2, 3			120	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	See Fig. 5
Output voltage with f_{IN} = 200MHz	6, 7	0.8	1		Vp-p	
Output voltage with f_{IN} = 1600MHz	6, 7		0.13		Vp-p	

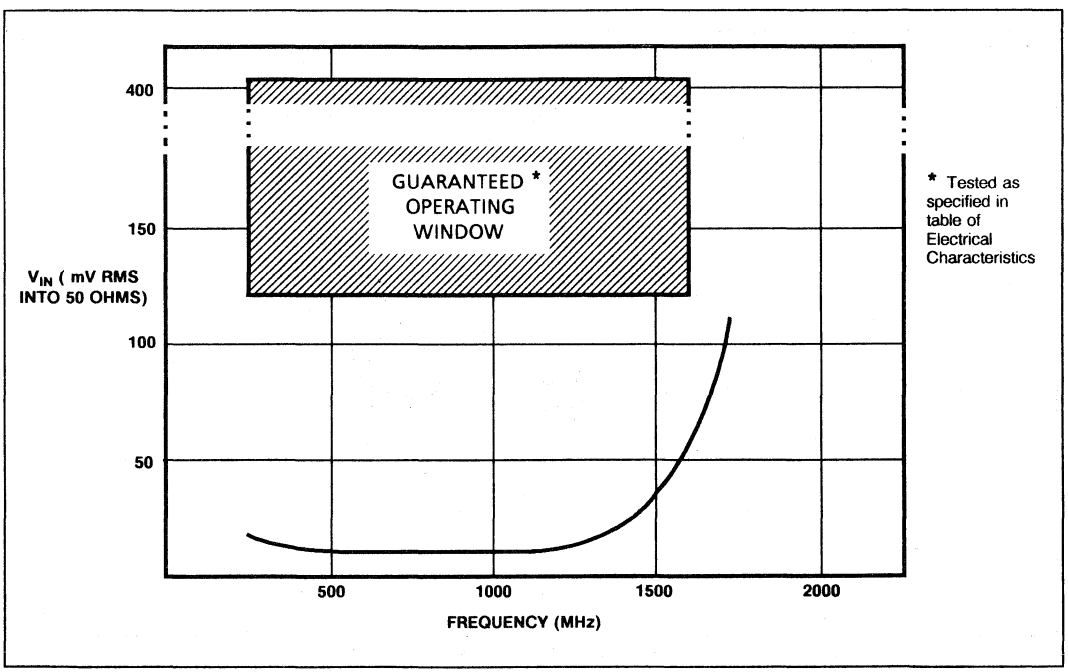


Fig.3 Typical input sensitivity

SP8824A1

1.3GHz ÷ 4 PRESCALER

(Supersedes December 1989 Edition)

The SP8824A1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.3GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 190mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -55°C to +125°C

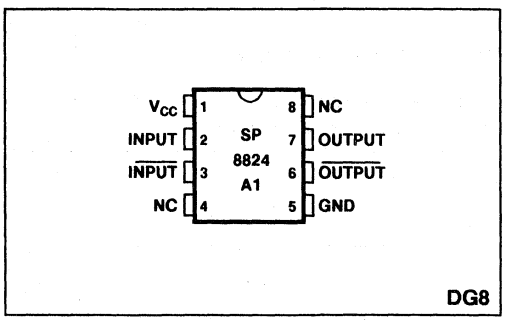


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8824 A1 DG

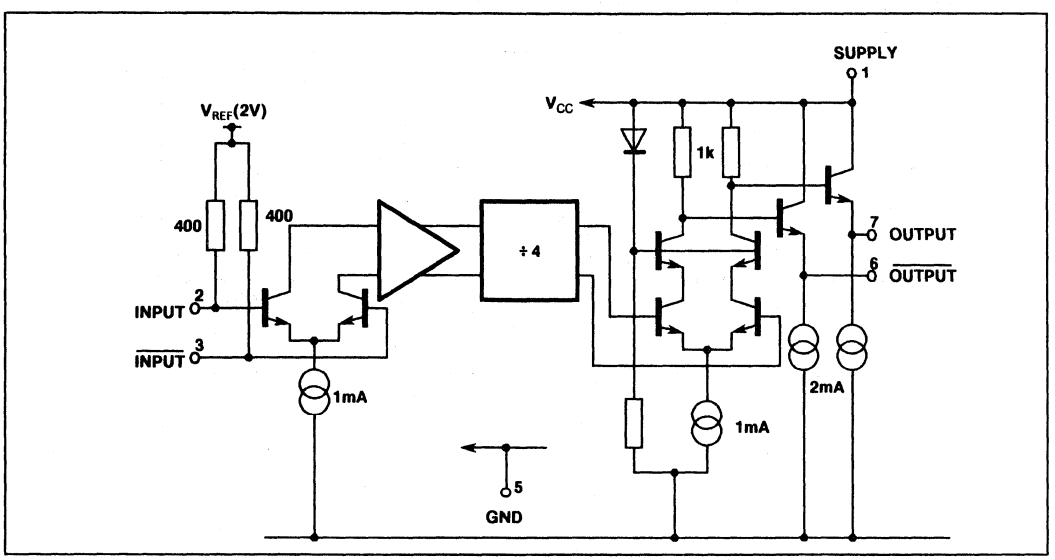


Fig 2 SP8824A1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –55°C to +125°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		38	48	mA	
Input Sensitivity, 200MHz to 1300MHz	2, 3			120	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	See Fig. 5
Output voltage with f_{IN} = 200MHz	6, 7	0.6	1		Vp-p	
Output voltage with f_{IN} = 1300MHz	6, 7		0.12		Vp-p	

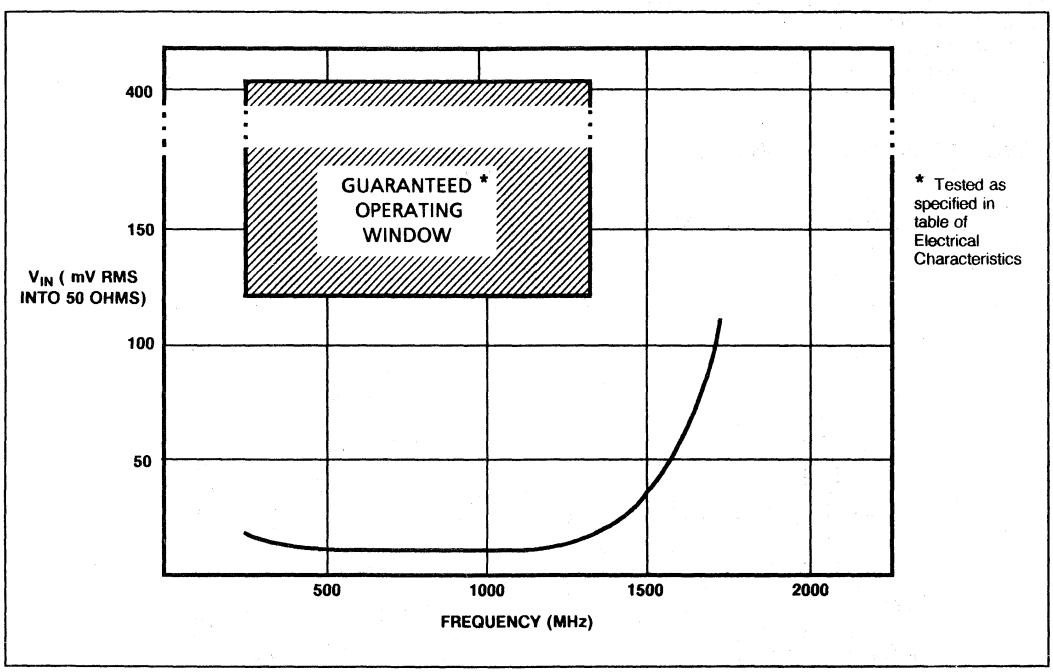


Fig.3 Typical input sensitivity

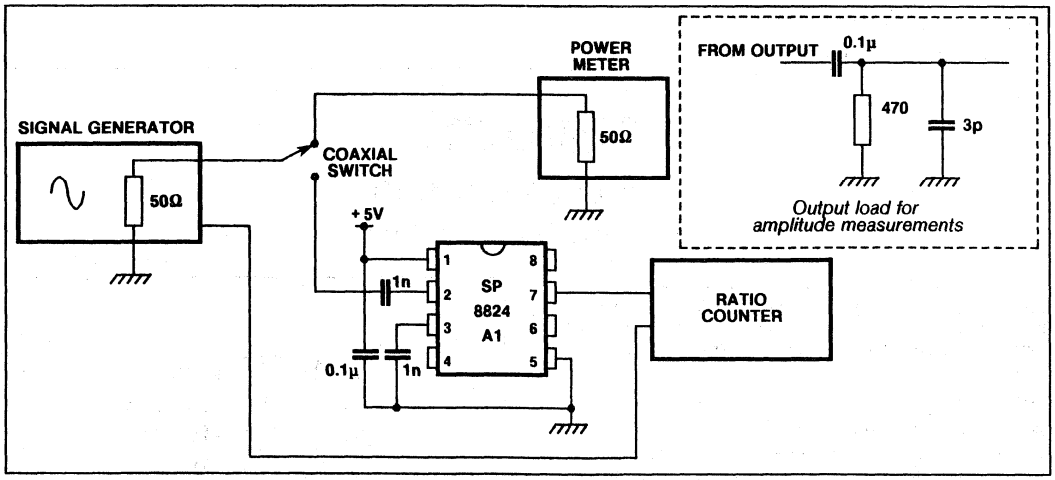


Fig.4 Test circuit

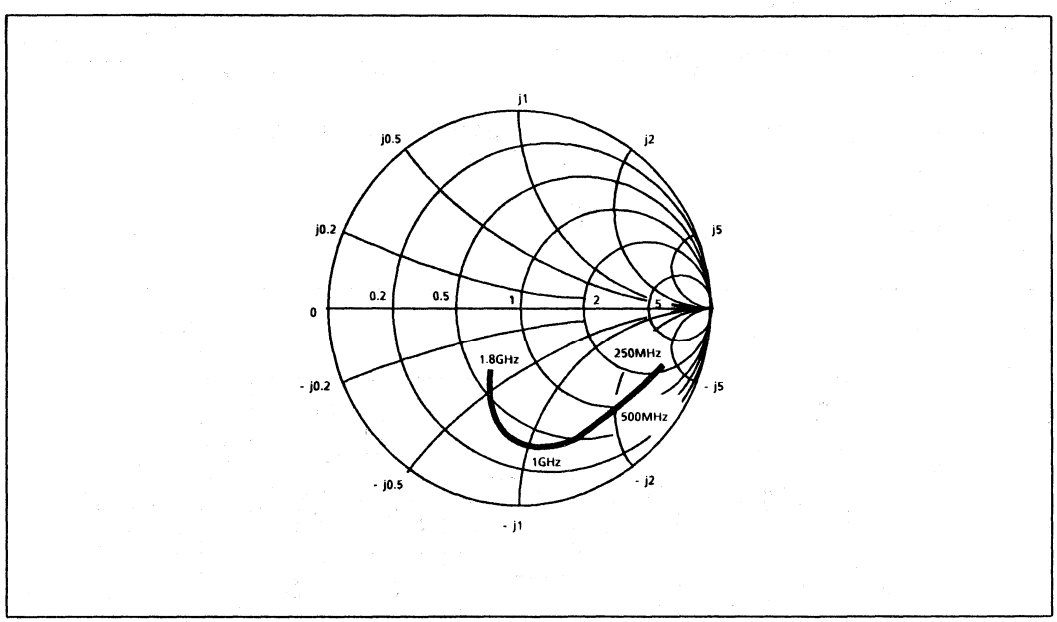


Fig.5 Typical input impedance, normalised to 50Ω

SP8824B1

1.6GHz ÷ 4 PRESCALER

(Supersedes December 1989 Edition)

The SP8824B1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.6GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 190mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -40°C to + 85°C

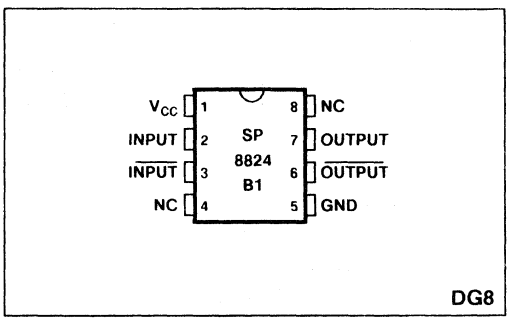


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8824 B1 DG

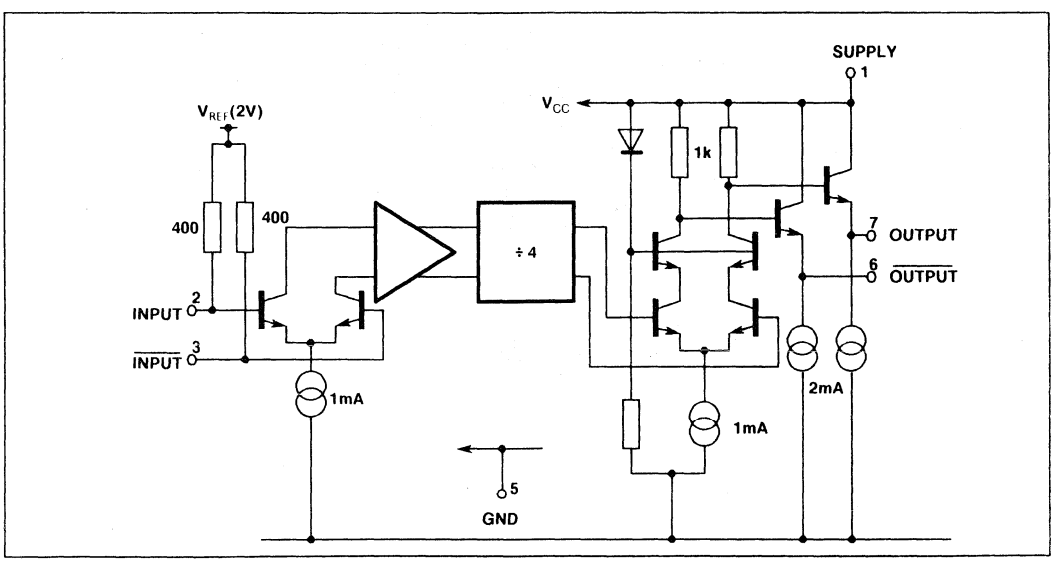


Fig 2 SP8824B1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		38	48	mA	
Input Sensitivity, 200MHz to 1600MHz	2, 3			120	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	See Fig. 5
Output voltage with f_{IN} = 200MHz	6, 7	0.6	1		Vp-p	
Output voltage with f_{IN} = 1600MHz	6, 7		0.15		Vp-p	

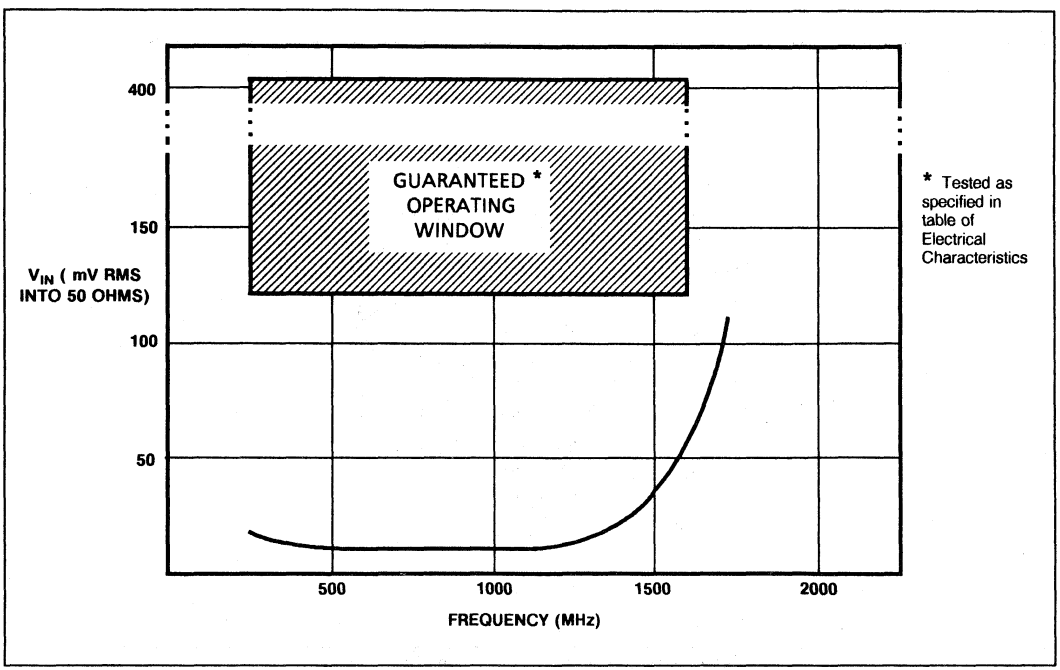


Fig.3 Typical input sensitivity

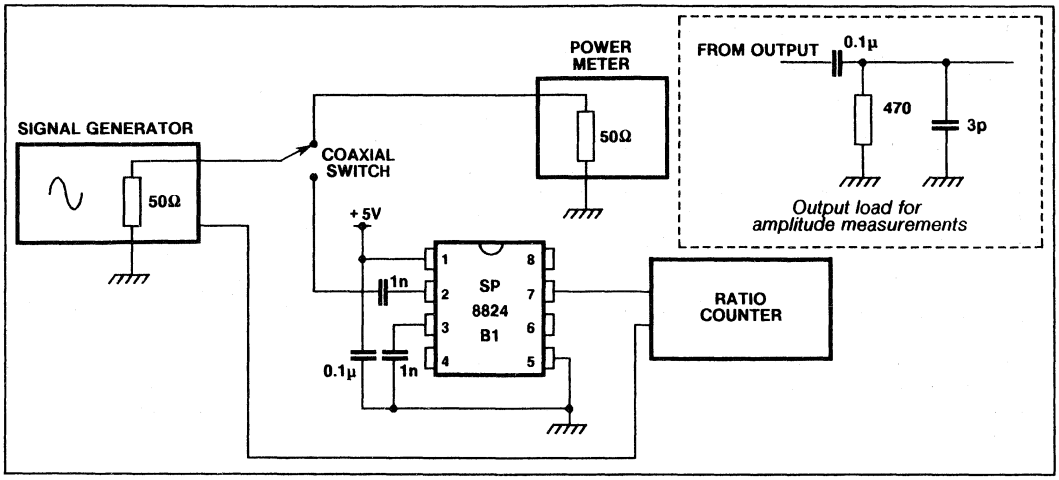


Fig.4 Test circuit

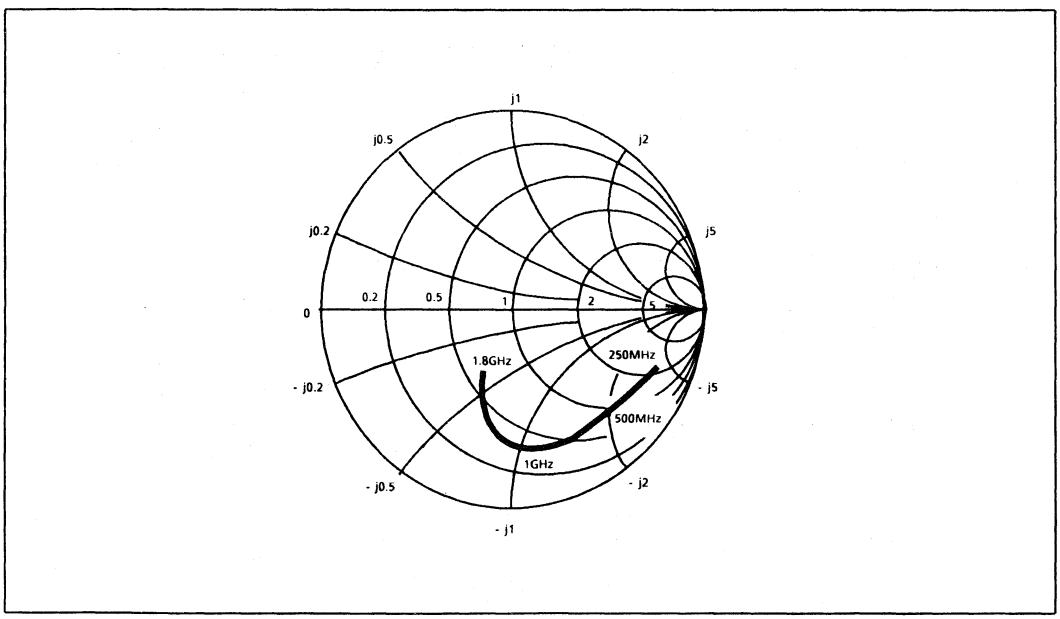


Fig.5 Typical input impedance, normalised to 50Ω

SP8828A1

1.3GHz ÷ 8 PRESCALER

(Supersedes December 1989 Edition)

The SP8828A1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.3GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 175mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -55°C to +125°C

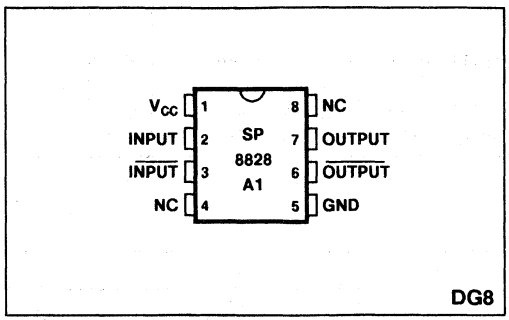


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8828 A1 DG

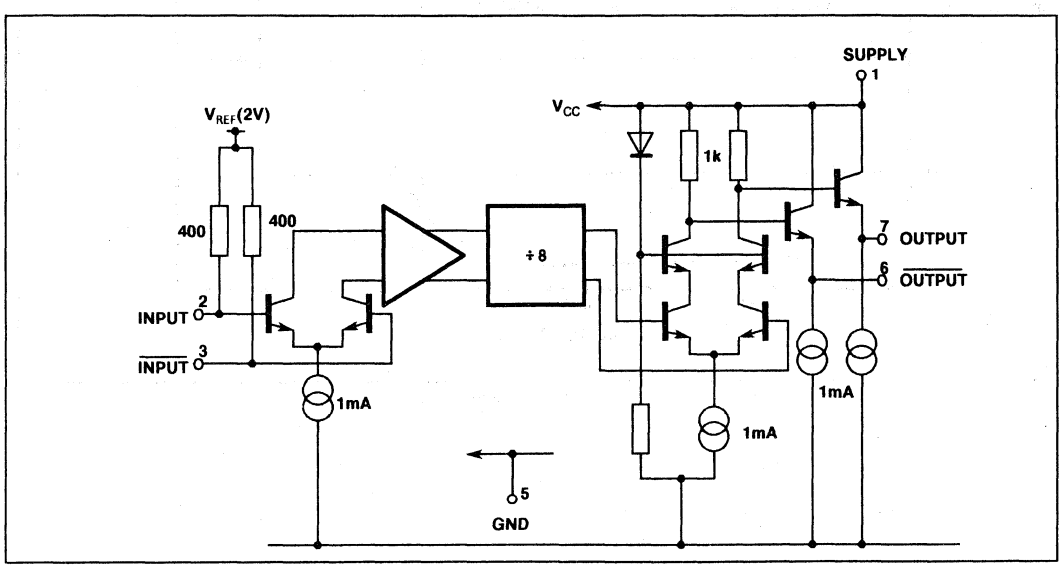


Fig 2 SP8828A1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –55°C to +125°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		35	45	mA	
Input Sensitivity, 200MHz to 1300MHz	2, 3			120	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50		Ω	See Fig. 5
			2		pF	
Output voltage with f_{IN} = 200MHz	6, 7	0.6	1		Vp-p	
Output voltage with f_{IN} = 1300MHz	6, 7		0.2		Vp-p	

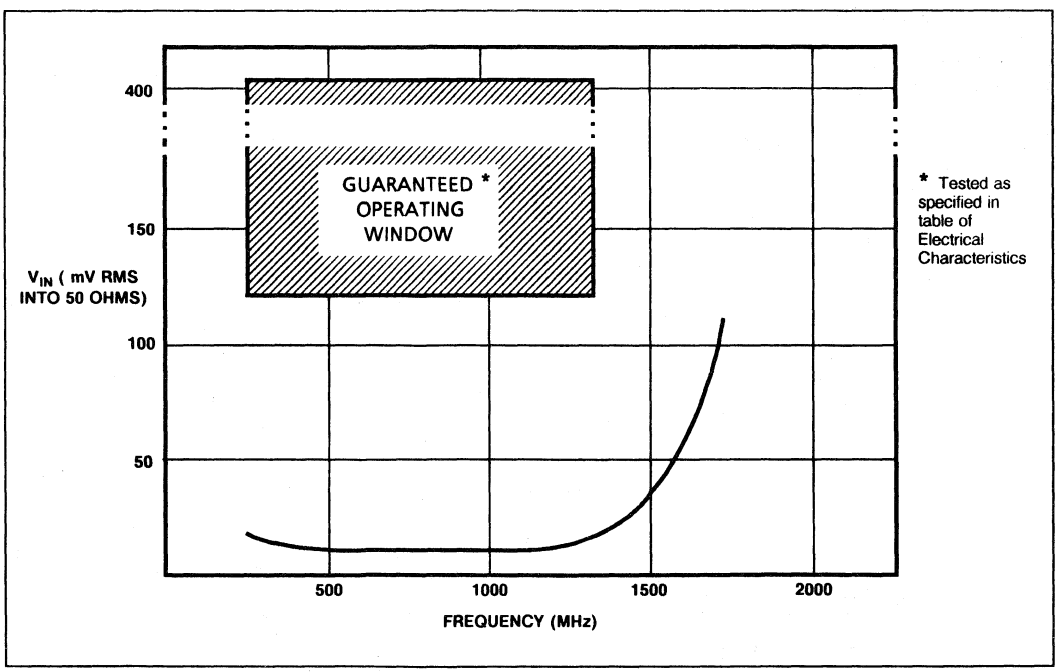


Fig.3 Typical input sensitivity

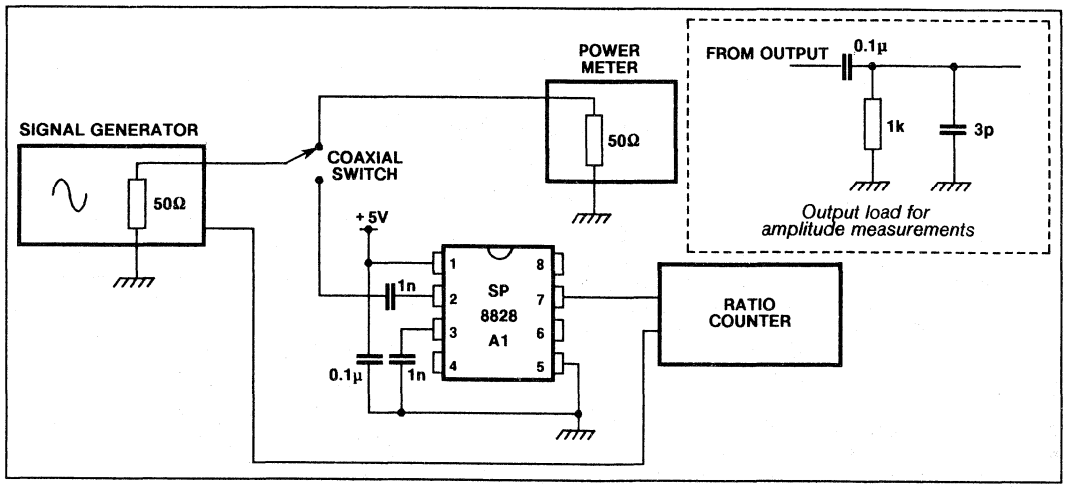


Fig.4 Test circuit

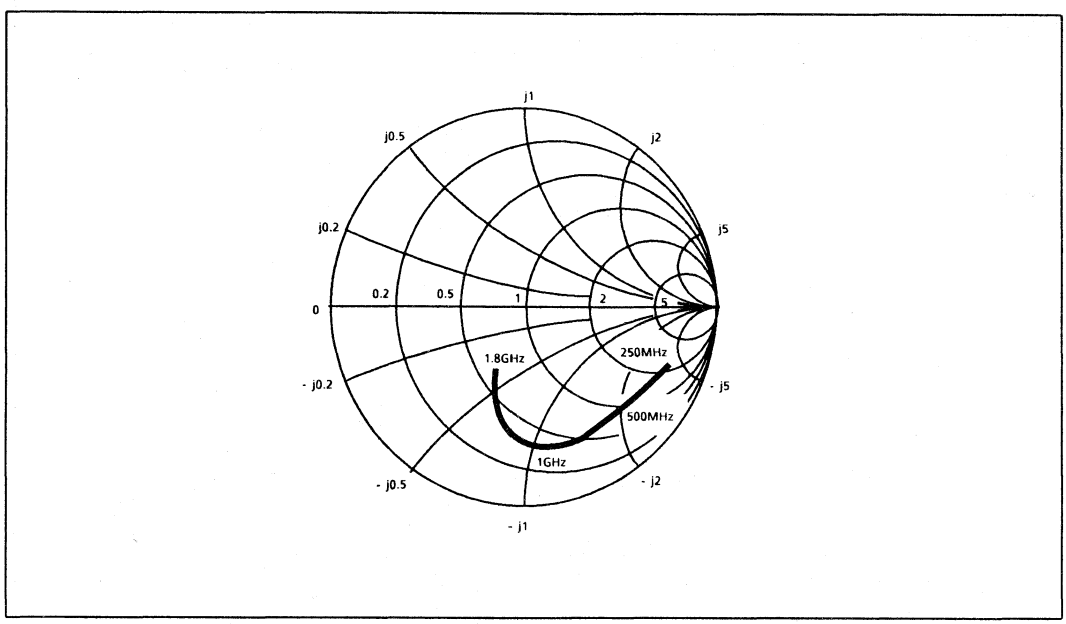


Fig.5 Typical input impedance, normalised to 50Ω

SP8828B1

1.6GHz ÷ 8 PRESCALER

(Supersedes December 1989 Edition)

The SP8828B1 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

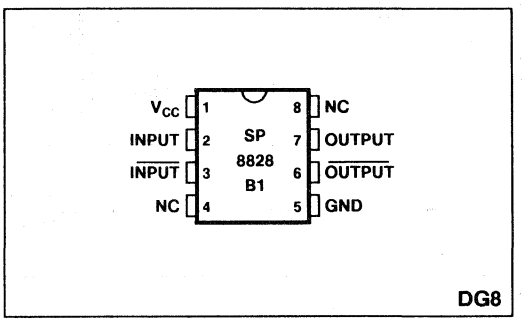


Fig 1 Pin Connections - top view

FEATURES

- High Speed Operation 1.6GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 175mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8828 B1 DG

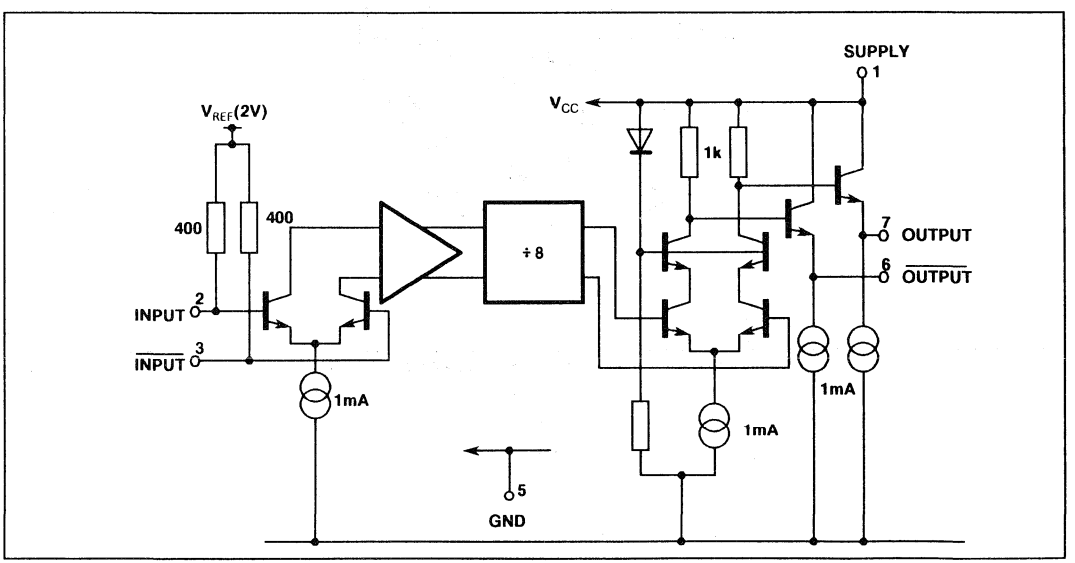


Fig 2 SP8828B1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: T_{amb} = –40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		35	45	mA	
Input Sensitivity, 200MHz to 1600MHz	2, 3			120	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	See Fig. 5
Output voltage with f_{IN} = 200MHz	6, 7	0.6	1		Vp-p	
Output voltage with f_{IN} = 1600MHz	6, 7		0.13		Vp-p	

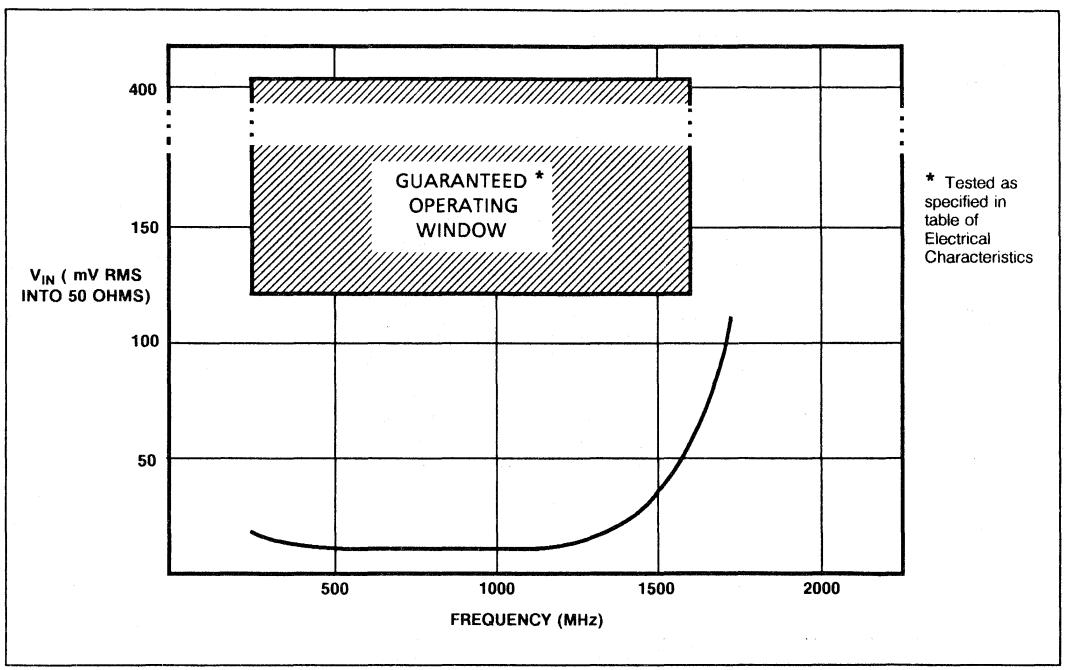


Fig.3 Typical input sensitivity

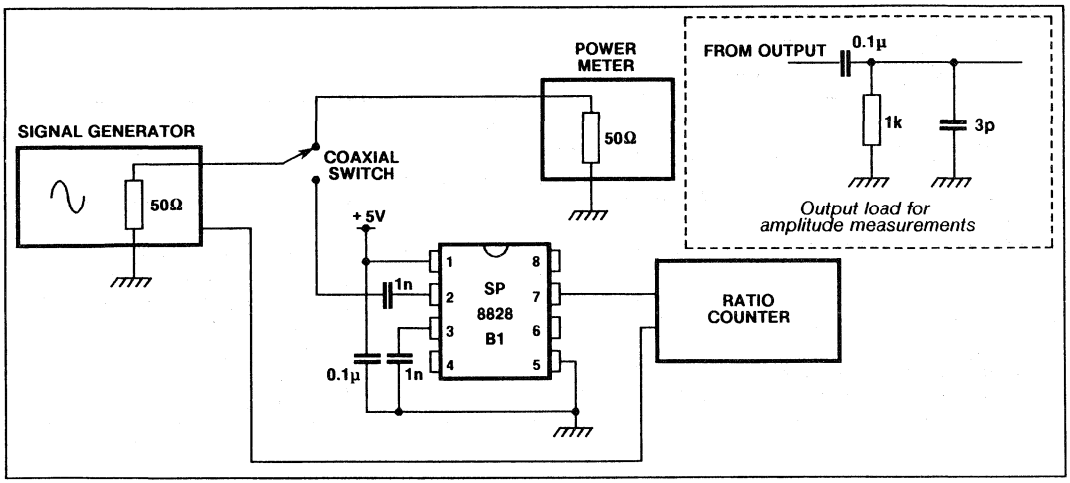


Fig.4 Test circuit

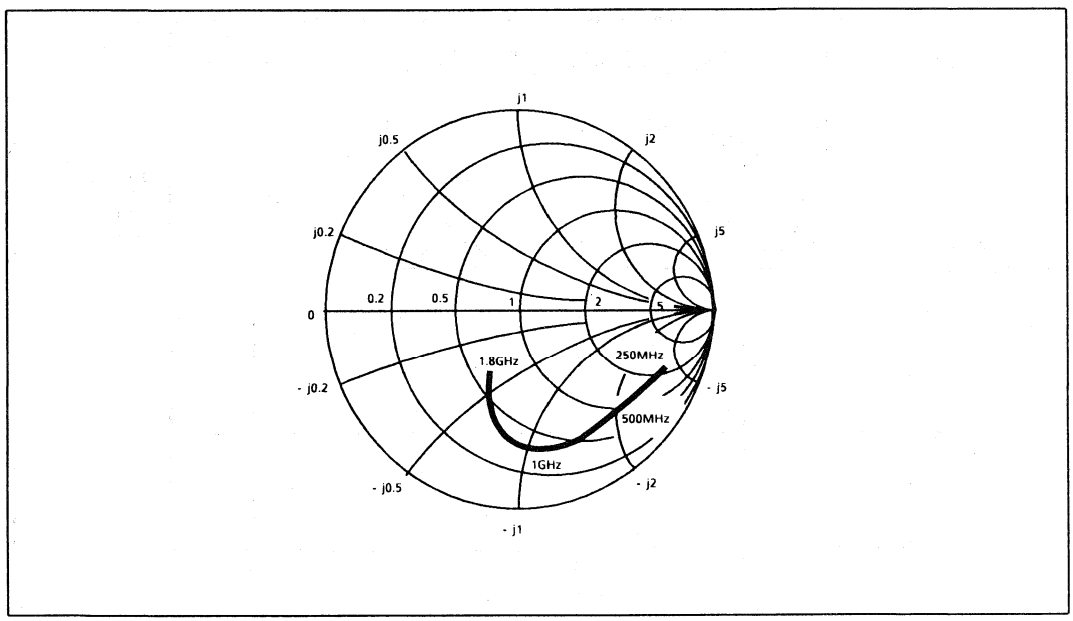


Fig.5 Typical input impedance, normalised to 50Ω

SP8830

1.5GHz ÷ 10 PRESCALER

(Supersedes December 1989 Edition)

The SP8830 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 1.5GHz
- Silicon Technology for Low Phase Noise (Typically Better than -140dBc/Hz at 10kHz)
- Very Low Power Dissipation 150mW (Typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range -55°C to + 125°C (A Grade)
  -40°C to + 85°C (B Grade)

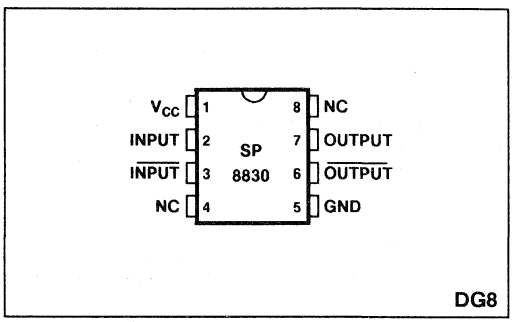


Fig 1 Pin Connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8830 A DG
SP8830 B DG
SP8830 AC DG

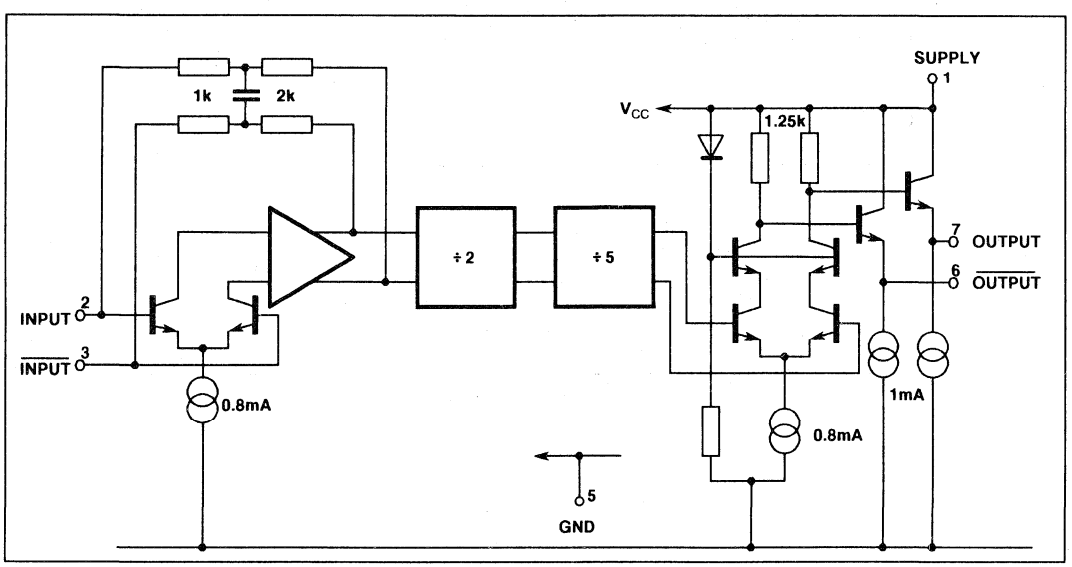


Fig 2 SP8830 Block Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage: V_{CC} = 4.75V to 5.25V
Temperature: A Grade T_{amb} = –55°C to +125°C, B Grade T_{amb} = –40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	1		40	50	mA	
Input Sensitivity, 100MHz to 1500MHz	2, 3			100	mV	RMS sinewave, measured in 50Ω system. See Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	See Fig. 5
Output voltage with f_{IN} = 100MHz	6, 7	0.7	1		Vp-p	
Output voltage with f_{IN} = 1500MHz	6, 7		0.4		Vp-p	

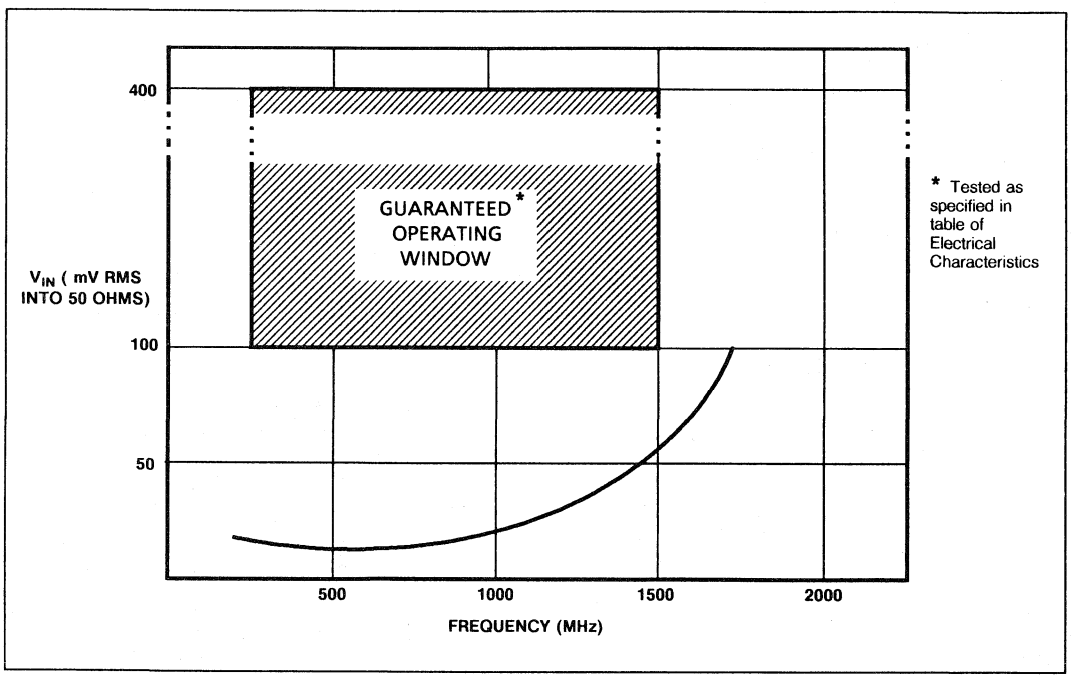


Fig.3 Typical input sensitivity

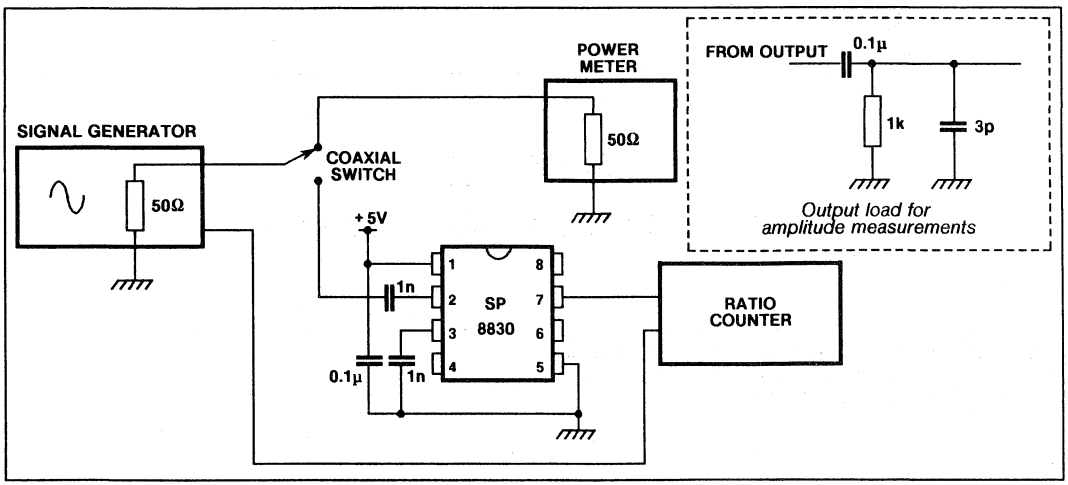


Fig.4 Test circuit

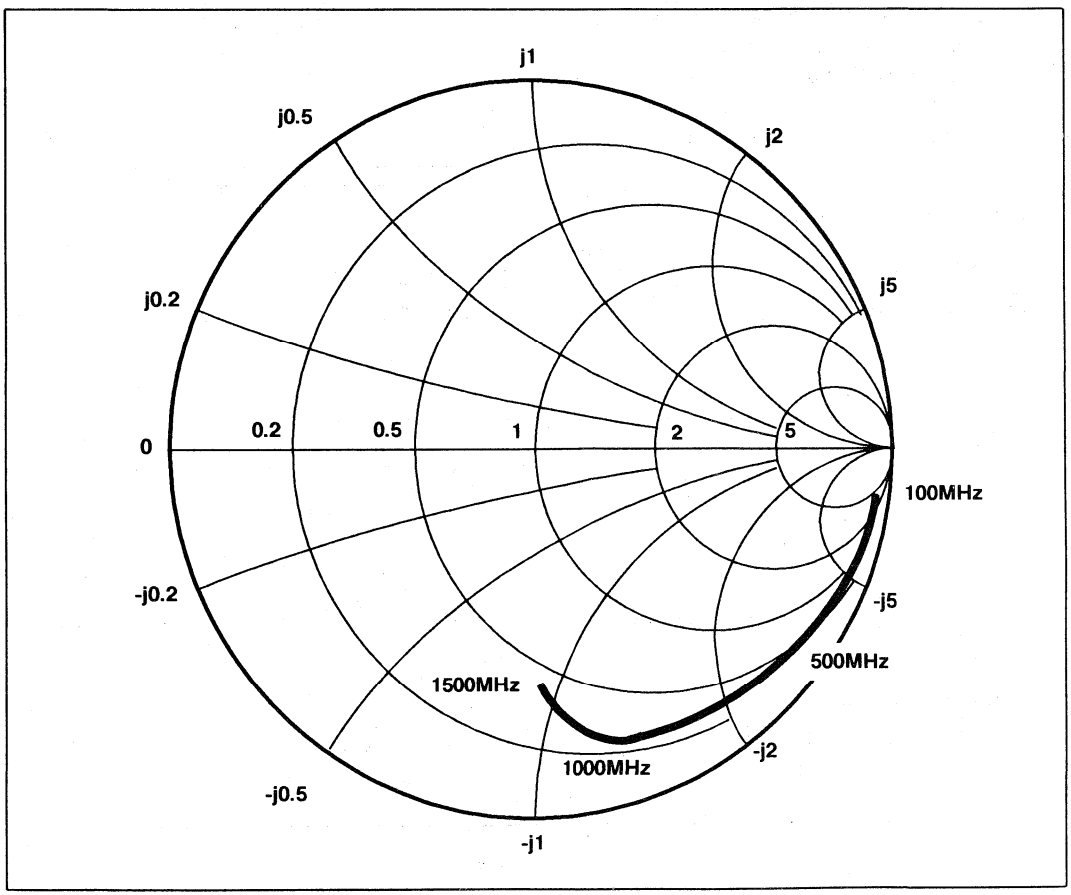


Fig.5 Typical input impedance, normalised to 50Ω

SP8832

3.5GHz ÷ 2 FIXED MODULUS DIVIDER

The SP8832B is one of a range of very high speed low power prescalers for professional applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

FEATURES

- Very High Speed Operation 3.5GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Low Power Dissipation 420mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

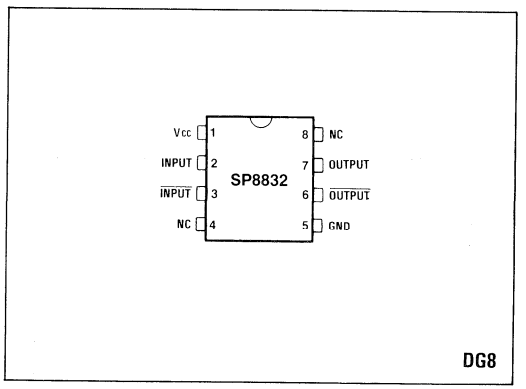


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8832 B DG

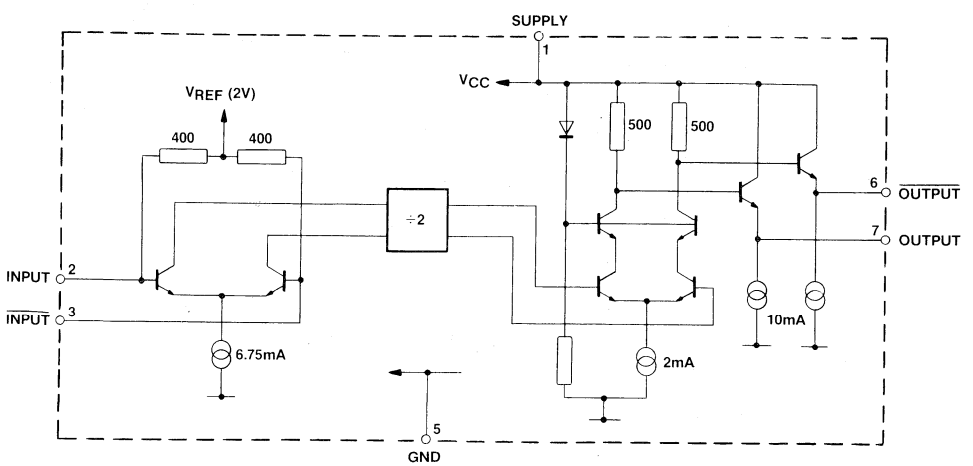
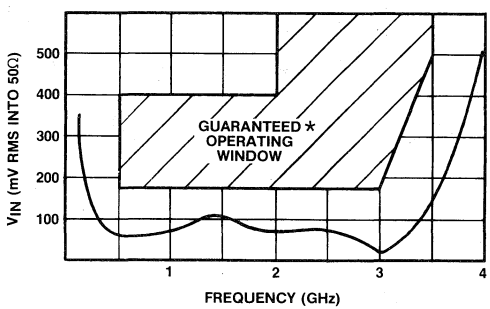


Fig.2 SP8832B block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		84	100	mA	
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.5GHz				500	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 500MHz	6,7	0.55	1		V p-p	
Output voltage with f_{in} = 3GHz	6,7		0.35		V p-p	Load as Fig.4



* Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

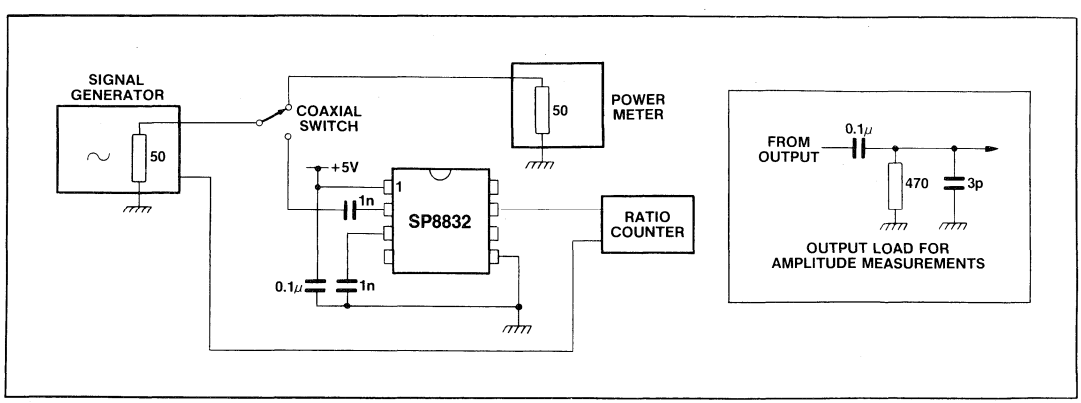


Fig.4 Test circuit

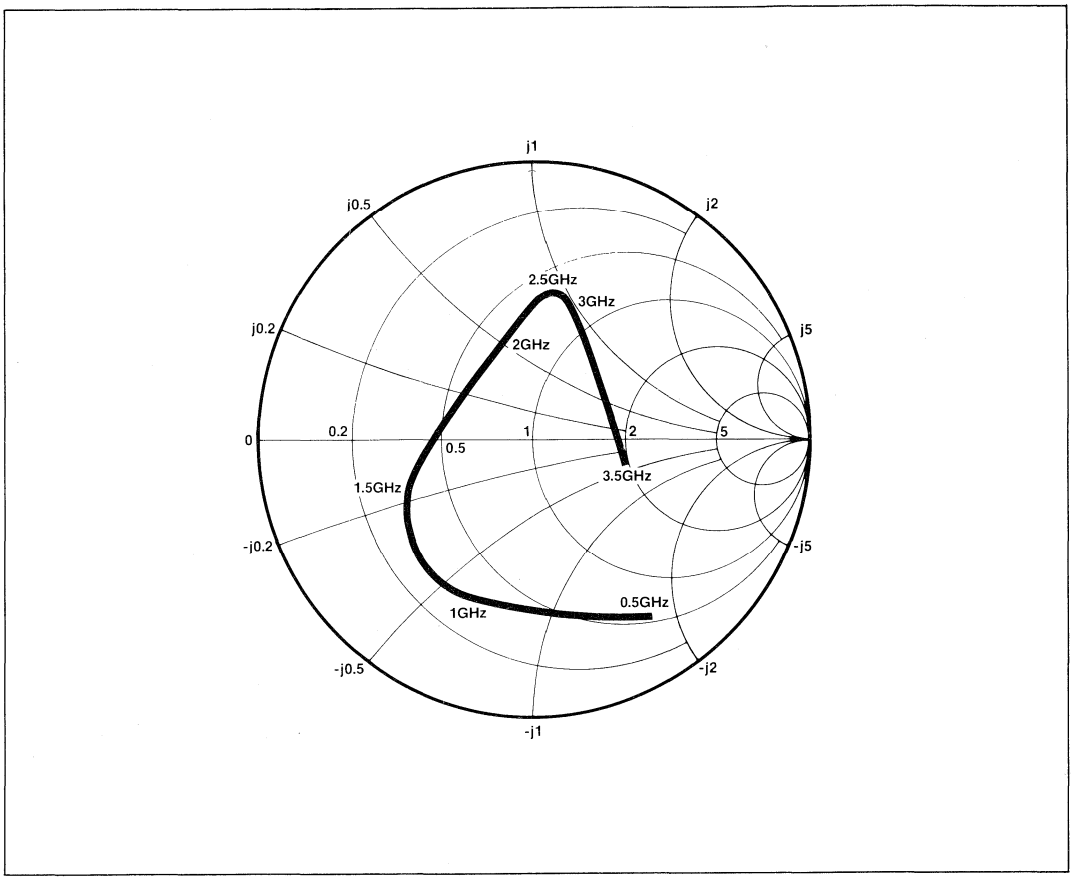


Fig.5 Typical input impedance

SP8835

3.5GHz ÷ 4 FIXED MODULUS DIVIDER

The SP8835B is one of a range of very high speed low power prescalers for professional applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

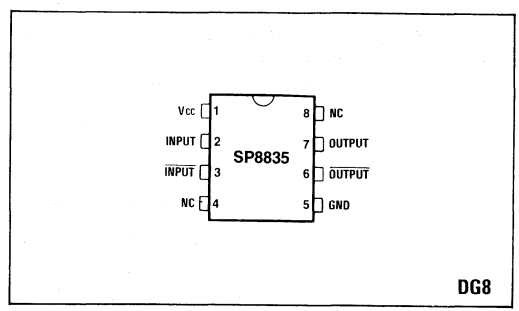


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.5GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Low Power Dissipation 370mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8835 B DG

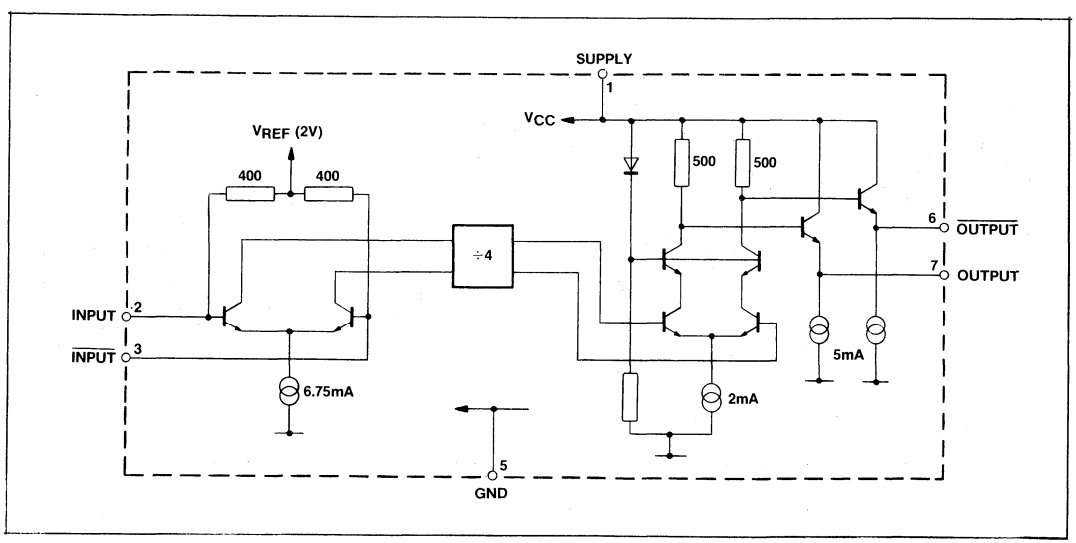
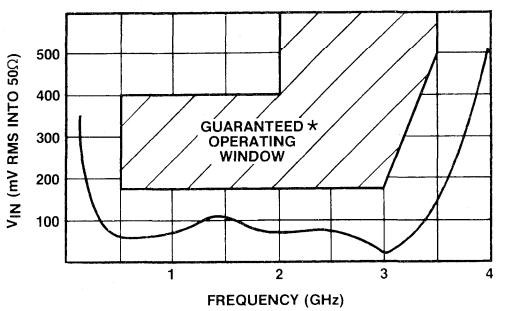


Fig.2 SP8835B block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		74	90	mA	
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.5GHz				500	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 500MHz	6,7	0.55	1		V p-p	
Output voltage with f_{in} = 3GHz	6,7		0.25		V p-p	Load as Fig.4



★ Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

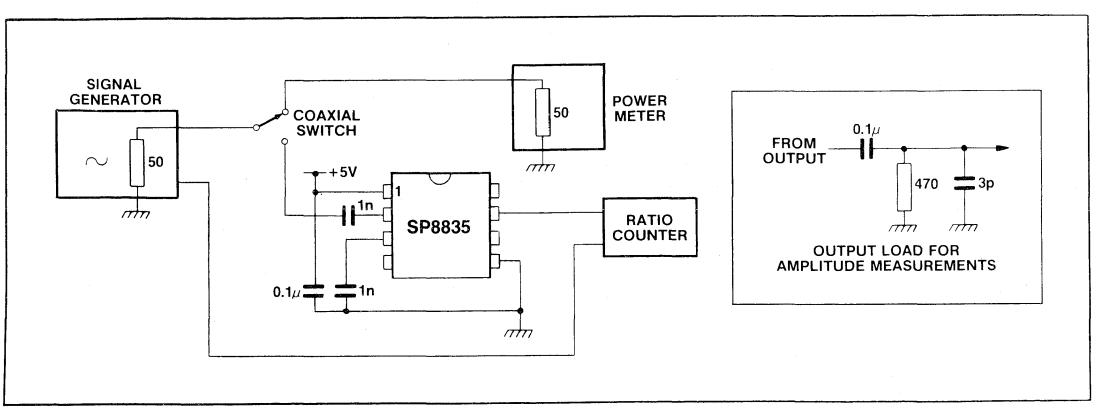


Fig.4 Test circuit

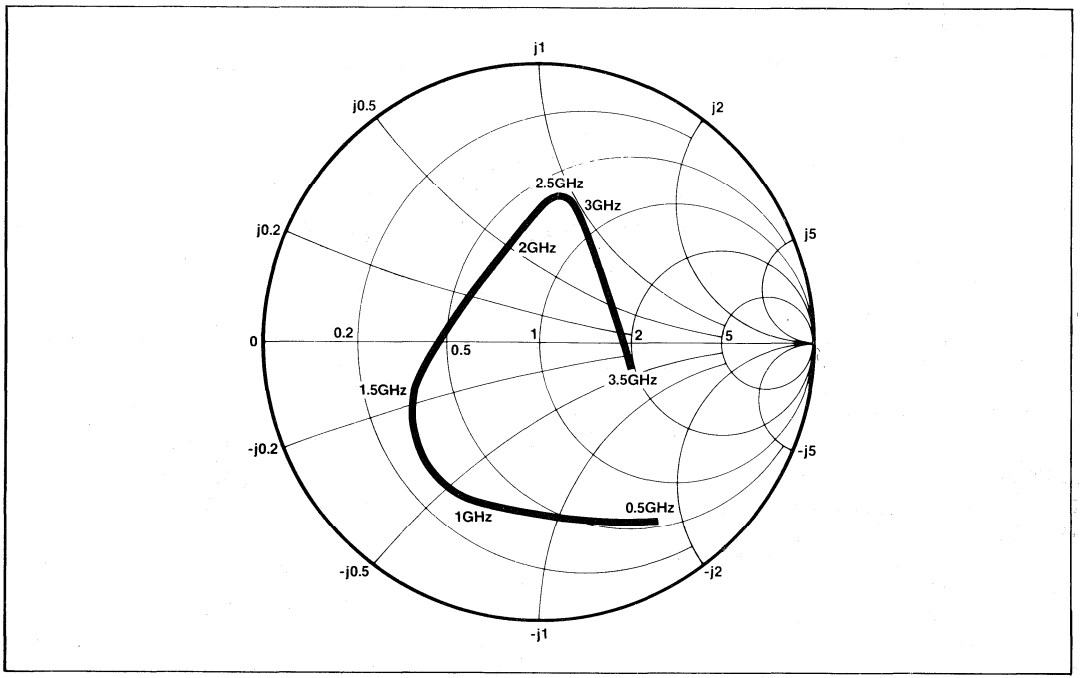


Fig.5 Typical input impedance

SP8838

3.5GHz ÷ 8 FIXED MODULUS DIVIDER

The SP8838B is one of a range of very high speed low power prescalers for professional applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

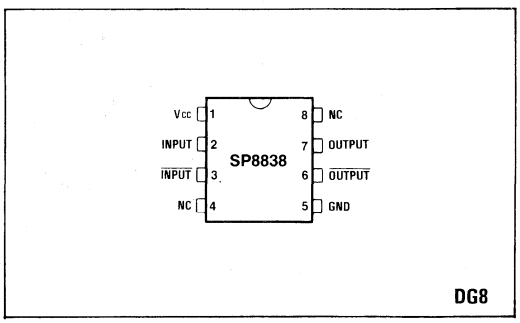


Fig.1 Pin connections - top view

FEATURES

- Very High Speed Operation 3.5GHz
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 10kHz
- Low Power Dissipation 345mW (Typ.)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage Vcc	6.5V
Clock input voltage	2.5V p-p
Storage temperature range	-55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8838 B DG

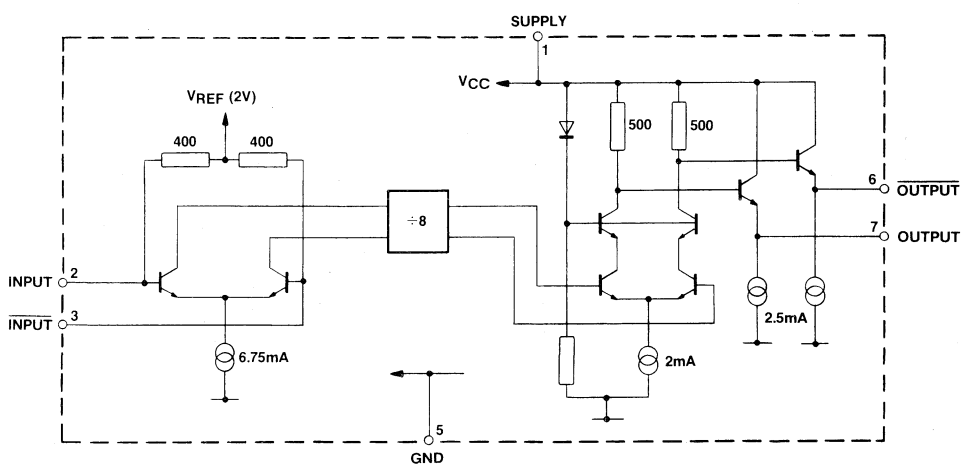
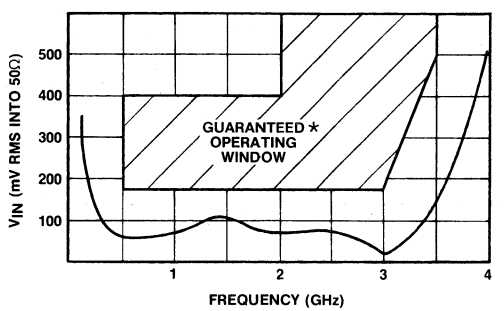


Fig.2 SP8838B block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to +85°C, V_{CC} = +4.75V to +5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	1		69	85	mA	
Input sensitivity	2,3					RMS sinewave
0.5GHz to 2.8GHz				175	mV	Measured in 50Ω
3.5GHz				500	mV	system. See Figs. 3 & 4
Input impedance (series equivalent)	2,3		50		Ω	
			2		pF	
Output voltage with f_{in} = 500MHz	6,7	0.55	1		V p-p	
Output voltage with f_{in} = 3GHz	6,7		0.4		V p-p	Load as Fig.4



★ Tested as specified in Table of Electrical Characteristics

Fig.3 Typical input sensitivity

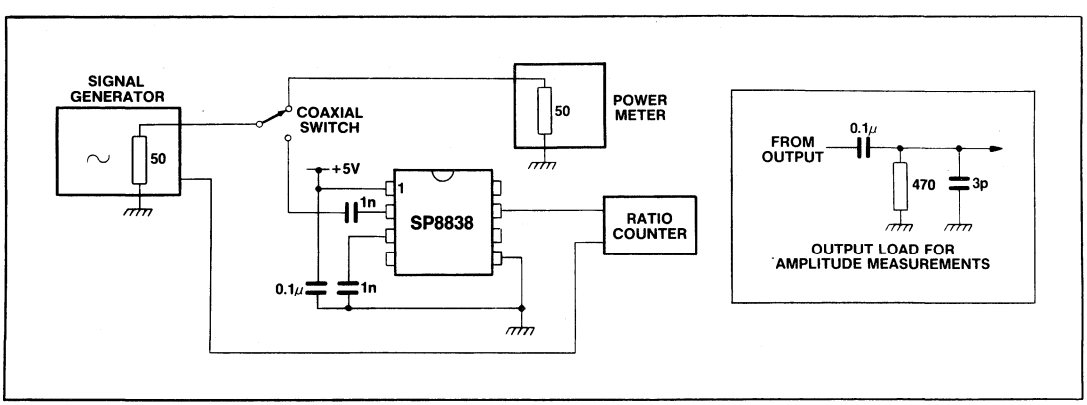


Fig.4 Test circuit

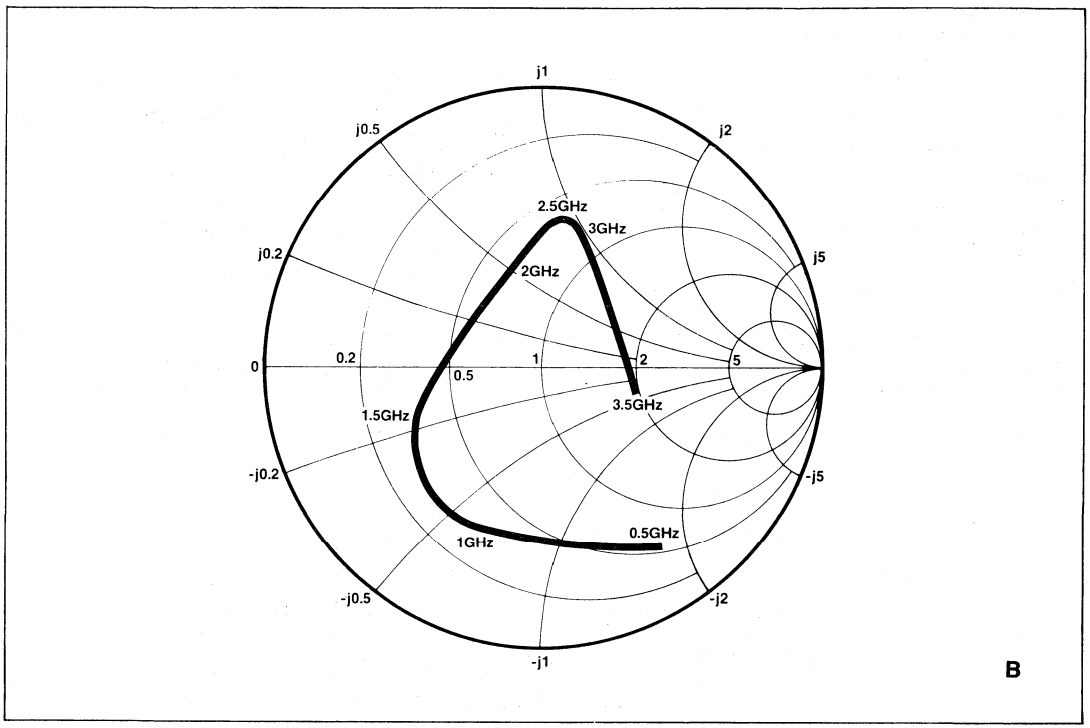


Fig.5 Typical input impedance

Section 4
Application Notes

Wideband VHF Antenna Booster using the SL560

The following is a brief description of a 40-260MHz antenna amplifier module suitable for any 50Ω VHF system. The module is constructed on a single sided PCB and layout is not critical as long as the usual precautions for VHF construction are observed.

An unusual feature of this module is the use of a transmission line transformer to provide 'noiseless' emitter feedback to the SL560.

The component count is minimal, i.e. 4 resistors, 7 capacitors, 2 inductors, 1 transformer, 1 SL560 IC and 2 diodes. The circuit for this application is shown in Fig.1.

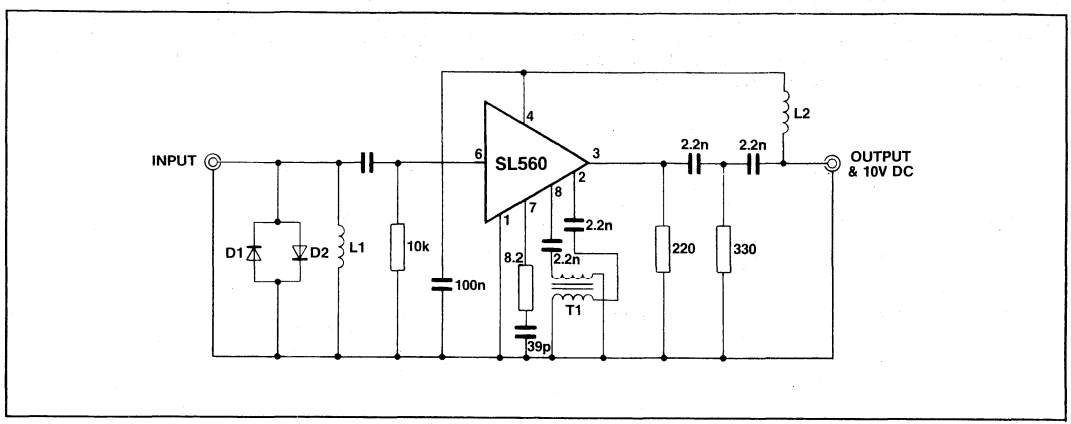


Fig.1

CONSTRUCTION

D_1 and D_2 are any general purpose silicon diodes.
L_1 is 8 turns of 26 gauge, $\frac{1}{8}$ inch internal diameter.
L_2 is 20 turns of 26 gauge, $\frac{3}{16}$ inch internal diameter.
T_1 consists of two lengths of 34 gauge wire approximately 6 inches in length, twisted together (8 twists/inch) and wound on a 6-hole ferrite bead (Mullard FX1898).
L_1 provides a degree of high pass filtering, some measure of protection against lightning by virtue of the DC path to earth, and it improves input SWR.
Resistor and capacitor values are not critical.
The module is powered through the coaxial cable and requires 10V at 30mA.

PERFORMANCE SPECIFICATION

The gain, 2nd and 3rd order intermodulation intercepts and SWR against frequency is shown in Fig.2. The gain flatness is within 5dB and the noise figure is better than 8dB.

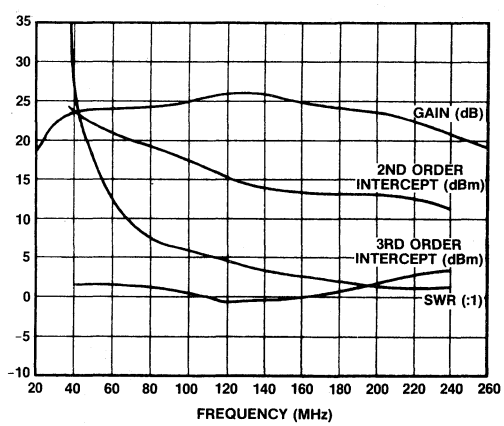


Fig.2

Using the SL561 in Pulse Amplifiers

The SL561 low noise preamplifier finds many applications in infra-red and ultrasonic equipments where a radar type signal is to be amplified. In such applications, large input signal levels can lead to unwanted pulse stretching. This application note describes the mechanisms involved and offers a simple remedy.

Generally, a large input signal which is of more than sufficient amplitude to severely overload the SL561 is applied and the amplifier is required to be at full gain as little as 10 microseconds later.

Study of the SL561 circuit diagram (Fig.1) shows that a large positive input pulse will lead to saturation of the input transistors. The effects of stored charge will lead to the transistors staying turned on for some time after the pulse, and a high source impedance will exacerbate the situation.

The amount of pulse stretching will vary from batch to batch of devices, as the amount of charge injected has a number of possible paths for its dissipation. By using a Schottky diode, as in Fig.2, the effects of the hard saturation can be avoided. When the cascode transistors saturate, the potential at the collector of the top transistor is low enough that the diode conducts, diverting input current away from the input transistor. The diode must be a Schottky barrier type and typically, the output pulse length is reduced by a factor of 12 to 15 when the diode is fitted.

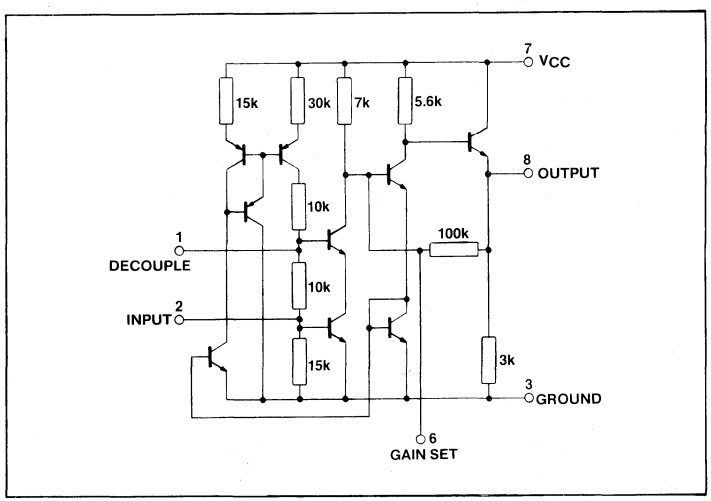


Fig.1 Circuit diagram

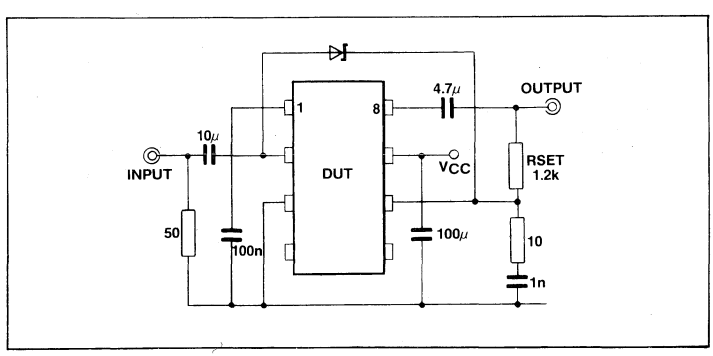


Fig.2 Application circuit

Tuned Amplifier using the SL6140

The SL6140 wideband AGC amplifier, when used in a 50Ω system, has a gain of 15dB. By tuning, or matching, the inputs and outputs of the device the gain can be increased. This produces a higher gain amplifier that will work over a limited bandwidth. The bandwidth of the amplifier depends on the Q factor of the tuned/matching circuits used. Fig.1 shows a single ended amplifier with a tuned input and output network.

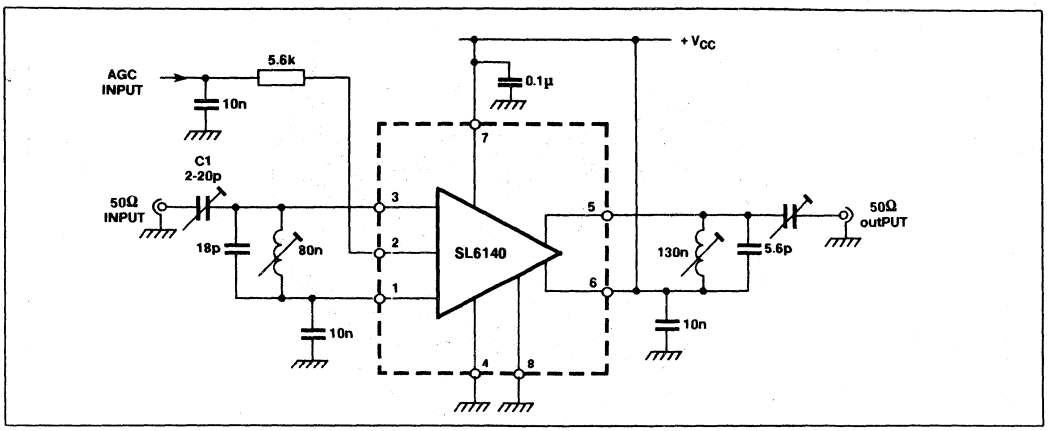


Fig.1 A 100MHz tuned amplifier application with 35dB power gain (CM pinout)

DESCRIPTION

The input circuit consists of a parallel LC network connected across the differential inputs. The input signal is applied to one input, via a coupling capacitor (C1), whilst the other input is decoupled. The coupling capacitor also forms part of the impedance matching network, matching a 50Ω source with the high input impedance of the device (see Smith chart, Fig.3).

The tuned frequency is given by the following equation:

$$f = \frac{1}{2\pi \frac{\sqrt{L \times C \times C1}}{\sqrt{(C + C1)}}}$$

The output circuit consists of a parallel LC network connected from one of the open collector outputs of the device to Vcc. The other output is connected directly to Vcc. The coupling capacitor (C2) and LC network transforms the 50Ω load to a high impedance load for the open collector outputs of the device, hence improving the gain.

By adjusting C1 and C2 the gain can be optimised. But if too high an impedance is seen by the input or output of the device the circuit may oscillate. L1 and L2 are adjusted to set the tuned frequency.

The high gain is achieved at the expense of bandwidth. So for maximum gain the matching network should be adjusted to provide the minimum bandwidth necessary, for the particular application.

An alternative method of tuning the output of the device is to transformer couple to the 50Ω load. The primary winding is connected across the outputs (a centre tap providing Vcc) and resonated, at the required frequency, with a capacitor, see Fig.2. This circuit has a 6dB improvement in gain over the previous circuit as both outputs are used.

PCB LAYOUT

For best performance a ground plane should be used with 50Ω track from the matching networks to the 50Ω source and load. The matching network and decoupling capacitors should be positioned as close to the device as possible.

If a very high gain, low bandwidth, amplifier is required the addition of some shielding between input and output may be necessary to prevent oscillation.

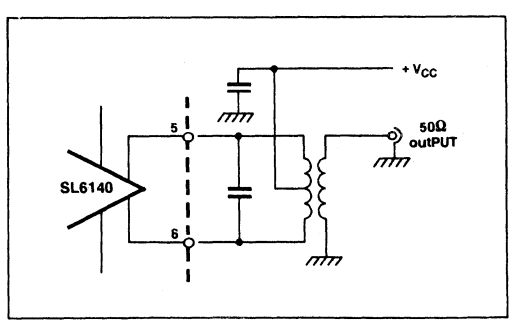


Fig.2 A Differential tuned output

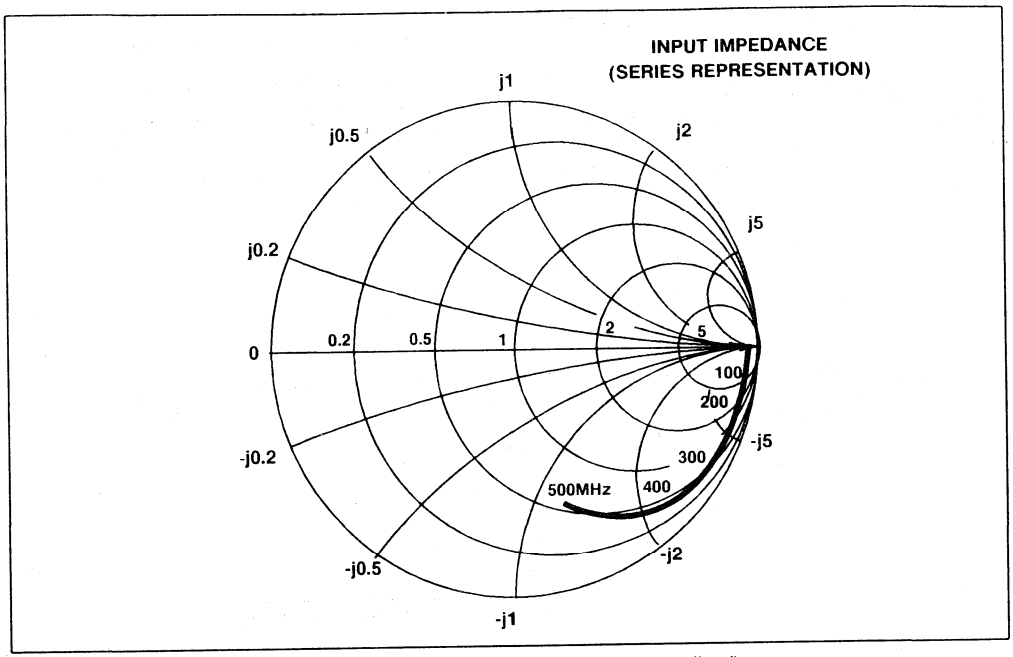


Fig. 3 Input impedance of SL6140 (50Ω normalised)

SL6270 — An Integrated VOGAD Circuit

The SL6270C is a monolithic integrated circuit intended for use in audio applications requiring constant output levels. It finds applications in radio communications, tape recorder applications, sound surveillance instrumentation and related areas. It has a differential input, and a constant output level of 90mV RMS, with a sensitivity of 1mV.

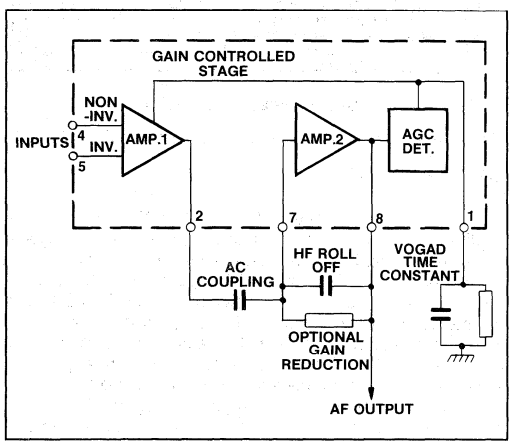


Fig.1

Voltages

The voltages given in Table 1 were measured in the circuit of Fig.2, with R2 = ∞, C1 = 2.2μF, C2 = 4700pF, C3 = 47μF and R1 = 1MΩ. The input was coupled via 2.2μF to pin 4, with pin 5 open circuit. Voltages were measured with a 20kΩ/V meter.

Pin	Input = 0mV	Input = 10mV	Input = 100mV
1	0V	1.6V	1.7V
2	3.5V	3.6V	3.6V
3	6.0V	6.0V	6.0V
4	1.6V	1.6V	1.6V
5	1.6V	1.6V	1.6V
6	0V	0V	0V
7	1.4V	1.4V	1.4V
8	1.4V	1.4V	1.4V

Table 1

DESCRIPTION

Refer to Block diagram - Fig.1.

The differential input amplifier is AGC controlled, and, being a true differential input, can be driven single ended, without the problems caused by other forms of push-pull input. The output from the AGC stage is coupled via a capacitor to the second stage, which is gain programmable by a single resistor. Adding a capacitor in parallel with this resistor allows the HF response to be programmed, if desired.

The output of this amplifier provides the main audio output from the device, and also drives the AGC detector. The detected output, which is input level dependent, is applied to the time constant circuit, and also to the gain controlled stage.

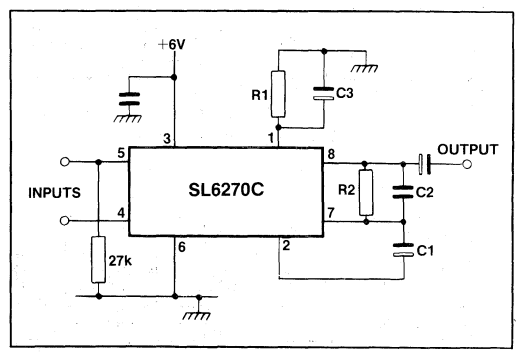


Fig.2 Connection diagram for SL6270C used as a microphone amplifier

Pin Functions

Pin	Function
1	**Gain control line.** An increasing voltage decreases the gain of the 1st amplifier.
2	**Audio output** from the gain controlled amplifier.
3	**Vcc supply.**
4	**Non-inverting input** to the gain controlled amplifier.
5	**Inverting input** to the gain controlled amplifier.
6	**Ground (0V).**
7	**Input to the second amplifier.** This is an inverting amplifier.
8	**Output of the second amplifier.**

The frequency response of the circuit of Fig.2 is shown in Fig.3: the input/output and overload characteristics are shown in Figs.4 and 5 respectively. Fig.8 shows the intermodulation distortion, and Figs.9 and 10 the pin connections. In the circuit of Fig.2, the microphone may be connected between pins 4 and 5 or between either pin 4 or 5 and ground.

Because of the careful design of the input stages, the device has an extremely high input dynamic range, and Fig.5 shows the distortion characteristics at various inputs.

The gain of the second amplifier can be programmed with a resistor between pins 7 and 8. This resistor value should not be less than 390Ω, while the threshold point is increased to about 8mV with a 1kΩ resistor. The gain of this amplifier without any feedback is approximately 50dB.

Decay rate is fixed by the RC network on pin 1, and with the values given is approximately 20dB/s.

In order to ensure that amplifier internal offsets are of such polarity as to inhibit oscillation at the onset of AGC, a 27kΩ resistor should be connected from pin 5 to the negative supply line.

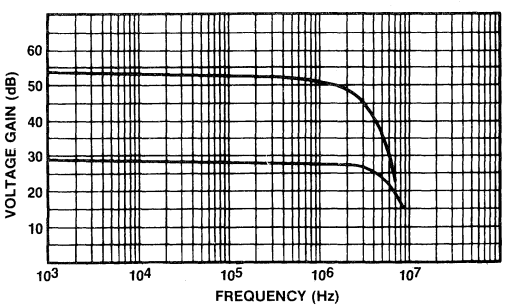


Fig.3 Frequency response

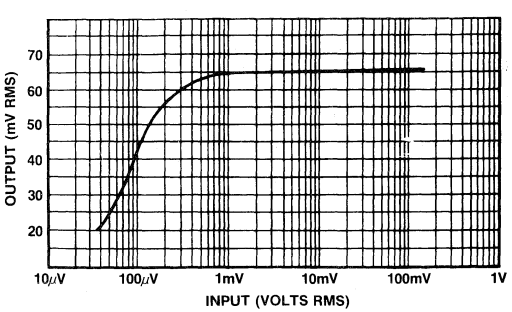


Fig.4 SL6270 Input/output characteristics Vs = +6V, T_{amb} = +25°C, f = 1kHz single ended input

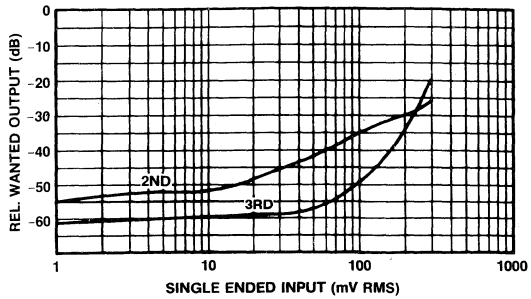


Fig.5 SL6270 distortion products v. input signal Vs = 6V 1kHz

APPLICATIONS

The simplest application for the SL6270C is in such applications as a radio transmitter. Fig.6 shows its use as a microphone amplifier and VOGAD with differential input.

Because of the separation of the gain controlled stages and the AGC generator, it is possible to use two SL6270C devices to control one audio signal by another one - see Fig.7. Here, a signal in Channel 1 causes gain reduction in Channel 2, and so, by suitable interconnection, a 'priority' system can prevent interference to the used channel.

IC1 acts as a VOGAD for Channel 1: IC2 for Channel 2. Whichever VOGAD is in operation reduces the gain of the other channel and thus, for multiple input sources, inteference from 'open' microphones is prevented.

Such a system may also be used for controlling voice operated switching devices since 'Antivox' can be applied to one device from a receiver output, and while the microphone is connected to the other. Receiver noise will then reduce the sensitivity of the transmit channel, preventing spurious triggering on received signals.

Where the SL6270 is used in applications with a DC path between pins 4 and 5, the resistance of this path should not exceed 10Ω. Otherwise, this path should remain open circuit.

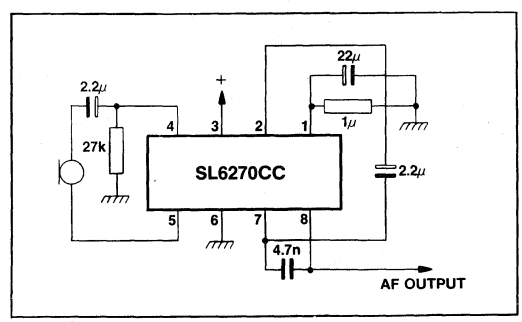


Fig.6

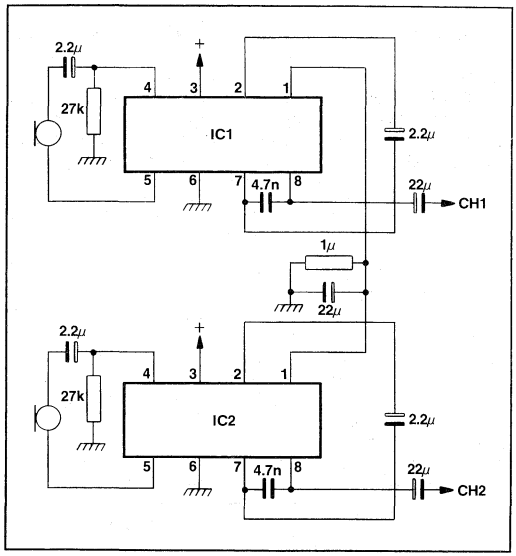


Fig.7

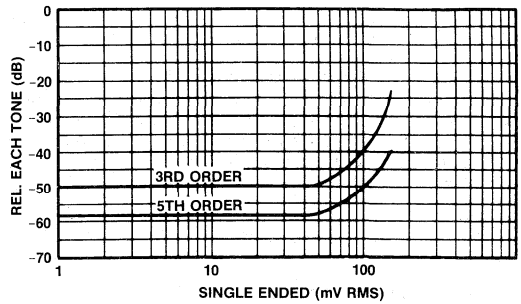


Fig.8 SL6270 3rd and 5th order IPs 1.55 and 1.85kHz Vs = 6V

Applications of the SL6310

The SL6310C is an integrated circuit designed specifically for use as an audio amplifier. It will operate from supplies of 4.5 to 15V, and will typically deliver an output of 500mW into 8Ω with less than 3% distortion at 9V, while at 12V, it can deliver up to 1W. It is a highly attractive circuit for hand held radio equipment, incorporating a mute or shutdown circuit, allowing the current consumption to be reduced to less than 600μA. In addition, being basically an operational amplifier with a power output stage, it is suitable for many other applications, such as a voltage regulator with shutdown, lamp driver, PIN diode driver, power comparator, and many other applications.

Fig.1 shows the block diagram of the SL6310C. In the AF amplifier application circuit (Fig.2), typical pin voltages and uses are as follows:

Pin 1 This is the non-inverting input pin, and is normally biased externally to half the supply voltage.

Pin 2 The inverting input: This will also be at half the supply voltage, being biased from the output.

Pin 3 Negative supply pin.

Pin 4 Output pin: This will be at half the supply voltage.

Pin 5 Positive Supply: This should be decoupled with an electrolytic capacitor connected with short, wide tracks.

Pin 6 Leave open circuit.

Pin 7 Mute control 1: This pin, when taken to earth via 100k, shuts down the circuit.

Pin 8 Mute control 2: This shuts down the circuit when taken to a potential greater than 2.2V above the negative supply line.

Both mute circuits should not be used simultaneously, but doing so will not damage the circuit.

A 1W AF AMPLIFIER APPLICATION

In this application (Fig.2) the circuit is biased by R1 and R2 to half the supply voltage on the non-inverting input, while DC feedback via R3 ensures that the amplifier acts as a voltage follower at DC.

The gain is fixed by R3 and R4, and is given by:

$$G = \frac{R3 + R4}{R4}$$

at mid-band frequencies.

The frequency response is fixed by C1, C2, and C4. C2 alters the amount of feedback at low frequencies, C4 is a series impedance with the load, while C1 is in series with the input. The HF response may be reduced by shunting R3 with a capacitor. As a guide, the LF response will be down by 6dB when XC4 = RL, or when XC2 = R4, while the reactance of any capacitor shunting R3 is equal to R3: With no capacitor across R3, and values of R3 and R4 to give a gain of 20dB (10 times), the frequency response exceeds 20kHz.

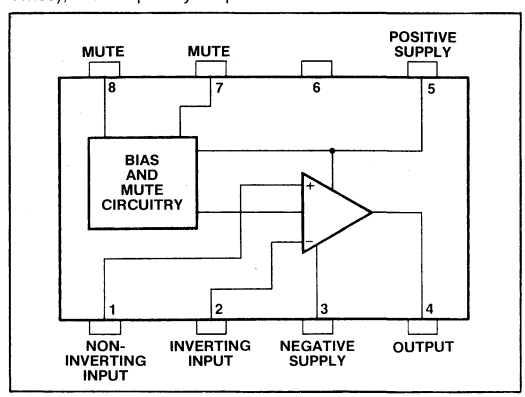


Fig.1 Circuit description

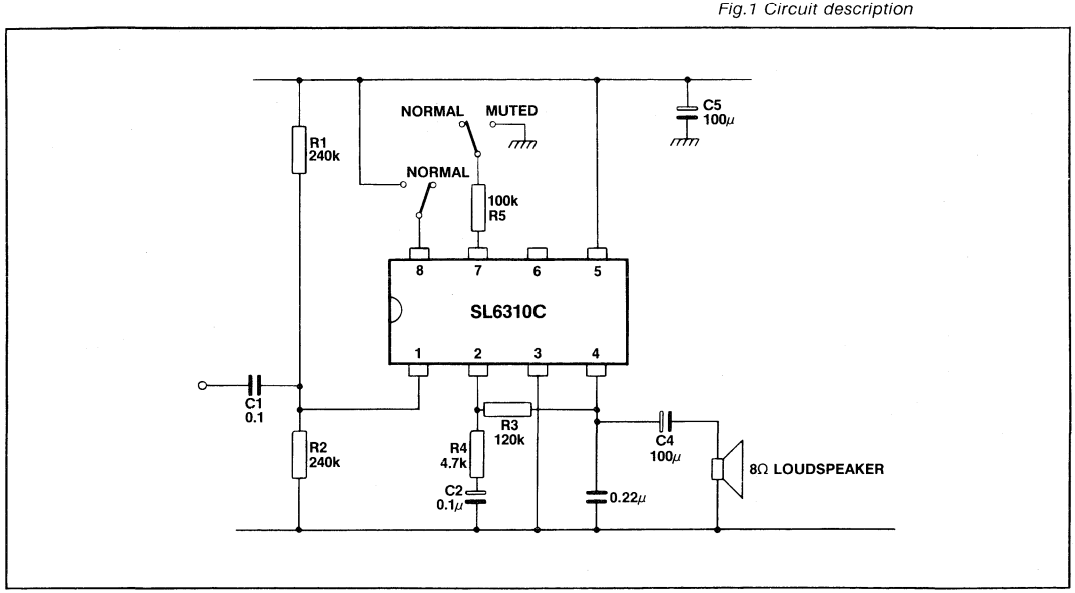


Fig.2 Test circuit

SL6440 High Level Mixer Applications

High performance modulators and frequency changers have historically used gain-less commutative mixer circuits such as the diode ring, or one of its derivations using FETs.

Integrated circuit mixers are available for only low signal levels, but also with relatively poor intermodulation performance. Other active mixers have not offered particularly good performance.

Typically, radio receivers requiring 3rd order intermodulation intercept points of +25 to +30dBm have used diode or FET commutative mixers with their inherent disadvantages of termination sensitivity and loss. The SL6440 is capable of 3rd order intermodulation distortion (IMD) performance far in excess of what has been previously available in integrated circuits together with gain and the advantages of integrated circuit technology.

MIXER TYPES AND DERIVATIONS

The basic balanced mixer is the single balanced type of Fig.1. This offers balance to the frequency f_2, but not f_1, and is analogous to a switch driven at f_2 opening and closing the connections between the transformers. Thus, f_1 is 'chopped' at f_2, and sidebands at $f_2 \pm f_1$ are produced. However, the output also contains components at f_1, and this is often an inconvenience. Fig.2 shows the diode ring modulator. In this, the signal current due to f_1 is switched alternately through the diodes to appear across the output transformer.

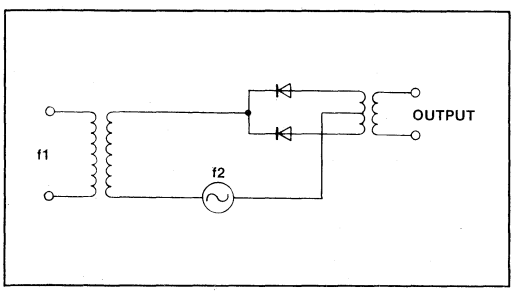


Fig.1 Single balanced mixer

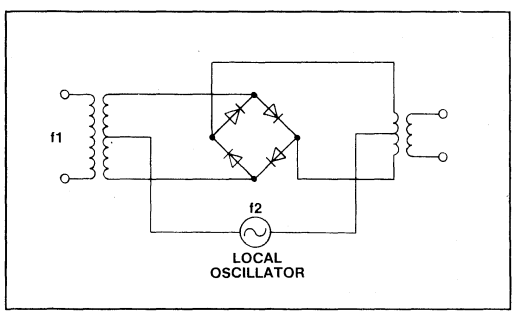


Fig.2 Diode ring

This switching is accomplished by the f_2 signal, which need not be applied across the centre taps of the transformers as shown but may be applied at a transformer port. The double balanced ring mixer of this variety is balanced to both input frequencies and is a very versatile and useful device. However, there are certain disadvantages, and these are:

1. High local oscillator power is required.
2. There is a loss inherent in the circuit.
3. The IMD performance is dependent upon the source and load termination impedances.
4. The balance (and thus the rejection of f_1 and f_2) is dependent upon the transformers and the diode matching.

Of these disadvantages, (1) is dependent upon the power handling required, while (2) can be shown to be $(3.12 + \log R_2/R_1)$dB, where R_1 and R_2 are the forward and reverse resistances of the diodes. This expression neglects transformer losses, and may be achieved only by proper termination. Unfortunately, this termination is one such that the image frequency components are reflected back into the mixer, and this can be shown to conflict with (3), where good IMD performance can be shown to require broadband terminations. Balance, however, can be relatively easily obtained with simple transformers and matched diodes.

One of the major disadvantages of the diode ring for very high performance is the amount of local oscillator power required, which is apparent if consideration is given to the diode characteristics. For example, if the total current through the diode is $I_{osc} + I_{sig}$, then at room temperature the forward resistance of the diode is $25/I_{total}$ ohms (where I is in mA). If I_{sig} is very small, the resistance of the diode is determined by I_{osc}, but if the I_{sig} is comparable with I_{osc}, the forward resistance is affected by the signal current. Because this is a non-linear relationship, intermodulation distortion will follow.

Where FETs are used, modulation of the ON channel resistance by the signal is a cause of Intermodulation Distortion. Unlike the ring mixer, this IMD cannot be decreased by increasing the local oscillator driver power, careful choice of FETs is required to achieve best results. Because the FET is used as a bi-lateral switch, the comments on terminations are as applicable to the quad FET mixer as to the diode ring. It should be noted that the simple non-commutative FET mixer is not particularly good on IMD or rejection of the LO signal.

One of the advantages of the double balanced mixer is its rejection of AM noise on the local oscillator, which can be a definite advantage in synthesised radio receivers.

The relative advantages and disadvantages of the various types of mixer are set out in Table 1. Although these tables provide a guide, they should not be considered as inviolable rules, applicable to all mixers of that particular type, because any particular mixer may or may not suffer from all the faults listed.

The transistor double balanced mixer is capable of minimising many of these problems. The circuit diagram is shown in Fig.3; because of the vertical stacking, it is often referred to as the 'transistor tree' mixer.

The performance of the 'tree' mixer of this sort is dependent upon several of the parameters of the transistors, and the ultimate performance requires some compromises of overall performance. However, noise figure and IMD can be easily optimised for best dynamic range, and this has indeed been done in the SL6440.

Because of high peak current (0.7A at 500mW in 8Ω), the supply pin (5) should be bypassed with an electrolytic capacitor, connected with short, wide leads, to obviate modulation of the supply rail.

The output power available is dependent on the supply voltage, and typical output powers range from 500mW into 8Ω at 9V to 1W at 12V and 1.3W at 15V.

Muting (or Shutdown)

There are two methods of muting the SL6310. Pin 8 may be lifted to a voltage greater than 3Vbe above the negative supply rail or, alternatively, Pin 7 may be pulled down to 1Vbe below the positive supply. Pin 7 should not be directly connected, but should have a resistor of 100kΩ in series to limit the current. Pin 8 has an input resistance of around 100kΩ, and so may be driven directly from TTL, LPTTL or CMOS is required. Both mutes should not be used simultaneously.

MORE APPLICATIONS

Fig.3 is a simple voltage follower application: the output current must be less than 0.4A and the dissipation must not exceed 1W at +25°C. The output voltage will need more than 2V below the supply voltage and will be equal to the voltage of the Zener diode, D1. The 220nF capacitor prevents instability.

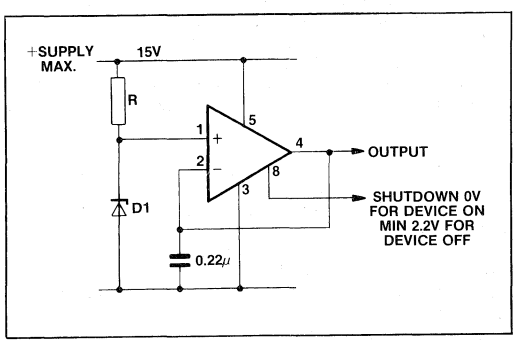


Fig.3 Power supply with shutdown

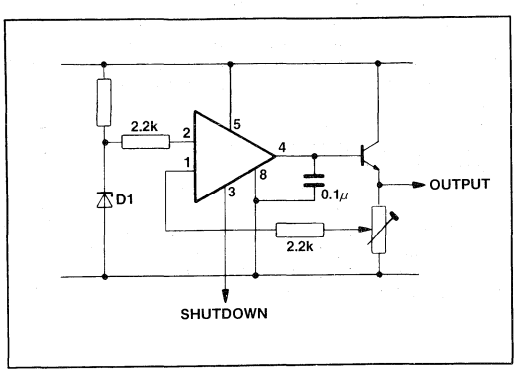


Fig.4 Preset power supply with boost transistor

In Fig.4 the output voltage is less than the Zener voltage, while the boost transistor allows a substantial increase in current capability. At high current levels, series pass transistors suffer from a drop in current gain, and thus require more base drive. The high output current capability of the SL6310C obviates the requirements for expensive Darlington transistors.

Applications of the SL6310C for use as a power comparator, lamp driver and DC servomotor driver are shown in Figs.5, 6 and 7, respectively.

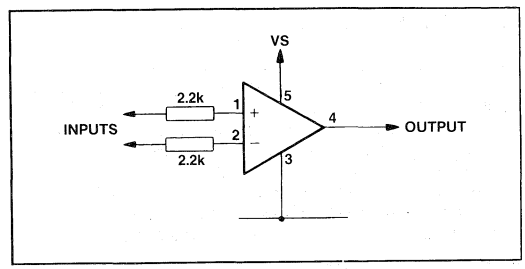


Fig.5 Power comparator

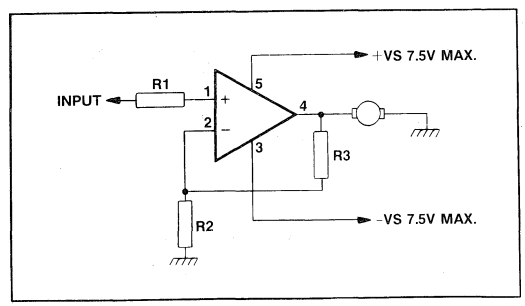


Fig.6 Lamp driver

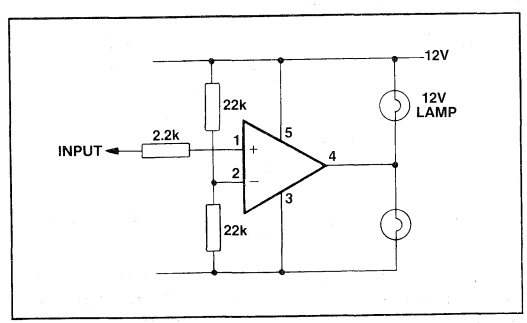


Fig.7 DC servo driver

Mixer type	Advantages	Disadvantages
Single diode	Wide bandwidth, low LO power, low cost.	No rejection of any component, no interport isolation, low input impedance.
Single FET transistor	Low noise, low loss or some gain, low cost.	Very poor IMD, no isolation, no AM rejection, poor overload, low input impedance.
Diode ring	Good IMD possible, high overload and compression.	6dB loss at least. IMD critically dependent on load termination. High LO drive power, and limited isolation. Low input impedance.
Quad FET	Good IMD range possible, overload good, low noise.	Expensive. Conversion gain, IMD and noise not easy to optimise. IMD performance is load dependent.
SL6440 IC balanced mixer	IMD performance set by current. Good LO isolation. Low LO power requirement. May be used with single ended or differential drive. IMD performance independent of load impedance. High input impedance. Can give gain by choice of output impedance.	Bandwidth limited to 200MHz. Noise figure 11dB for best IMD. Compresion Compression point lower than best diode rings.

Table 1

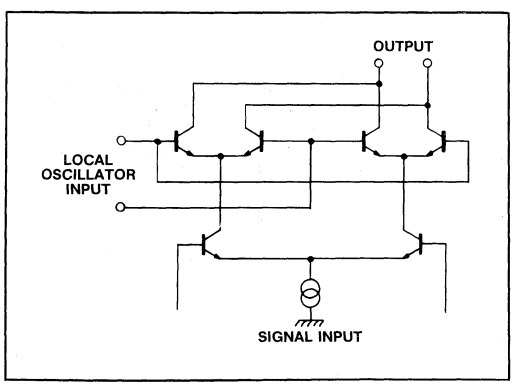


Fig.3 Transistor tree

THE SL6440 HIGH PERFORMANCE MIXER

Refinements to the transistor 'tree' allow the IMD of the simple tree to be improved. This improvement is dependent upon the amount of current in the transistors at the bottom of the tree. Obviously, for large input signals this current must be quite high and is modulated by the input signal current.

For best IMD results, the voltage-to-current conversion in the bases of the lower transistors should be as linear as possible, while minimum noise requires the lowest possible amounts of emitter resistance. The gain is also dependent upon the magnitude of the load resistance, but obviously, this magnitude must not be such as to saturate the transistors when the maximum current is flowing. In the SL6440, this current, and thus the IMD performance, is programmable by means of an external resistor, thus allowing a great deal of flexibility in use.

Figs. 4, 5 and 6 show the relationships between IMD performance, compression point, bandwidth and current and voltage. In general, it can be seen that increased supply power gives increased performance. However, it must be remembered that where the SL6440 is used such that conversion gain occurs, the compression point is reduced.

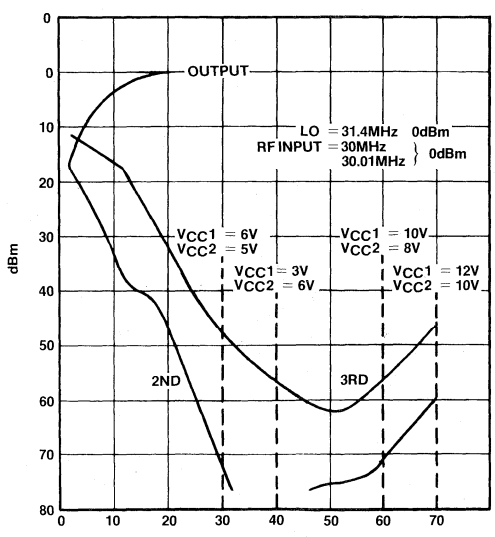


Fig.4 Intermodulation v. total output current (2IP). Average composite readings.

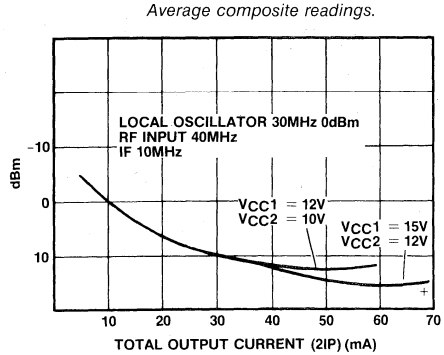


Fig.5 1dB compression point

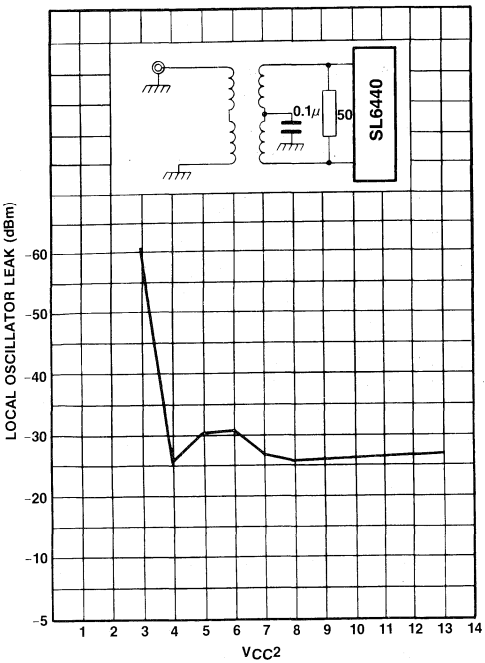


Fig.9 Local oscillator leak, LO = 31.4MHz 0dBm, Vcc1 = 15V, direct coupled transformer input.

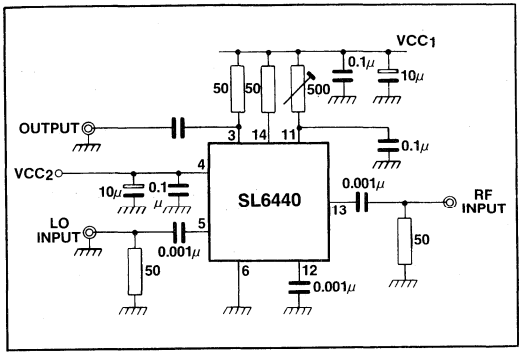


Fig.10 SL6440 basic application circuit

The simplest use of the SL6440 is in the circuit of Fig.10. Here the input and outputs are single ended, and because of the voltage drop in the output load resistors, Vcc1 should be at a voltage of [(51 x I programme) + 2 + Vcc2] V. By increasing Vcc1 and the load resistors, gain can be obtained.

If transformer coupling is used, then the high input impedance can be utilised, and Fig.11 shows an application as the signal frequency stage of a high performance HF receiver. Table 2 lists the characteristics of this mixer stage, which can be improved for transmitter use by increasing the supply voltages to improve the compression point. The 500Ω resistor allows the current to be programmed as desired. The use of transmission line transformers increases the frequency range over which a good match can be obtained: those used in Fig.11 are adequate for most applications in the HF range.

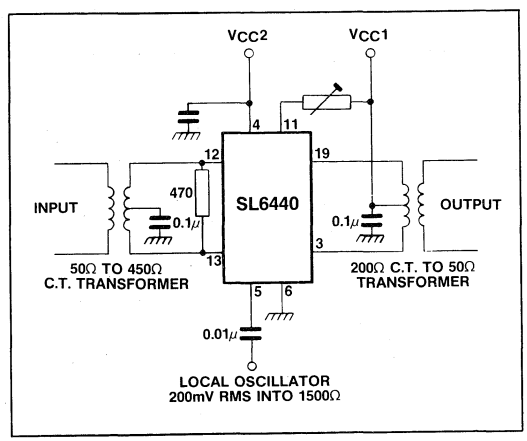


Fig.11 High performance HF receiver mixer

Parameter	Performance	Conditions
Sensitivity	15dB S + N/N	1μV EMF, SSB Bandwidth 30MHz, f = 1MHz
IMD 3rd	> 70dB	Input = 142mV EMF each signal 10kHz separation
IMD 2nd	-80dB	Input = 142mV EMF each signal
LO Radiation	-65dBm	Measured in 50Ω at input port
Blocking	100mV EMF	3dB blocking 1μV EMF wanted signal
IF Rejection	30dB	Rejection measured at input port
Input Matching	22dB	Returned loss in a 50Ω system
Gain	10dB	

Table 2 Performance of Fig.11

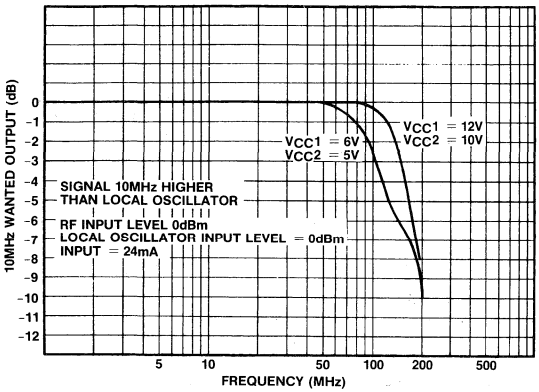


Fig.6 Frequency response with constant output IF

USING THE SL6440

The SL6440 is very flexible insofar as it can be used with differential or single ended inputs and outputs. For best balance, the use of a differential input is recommended, and Figs.7, 8 and 9 show that variation in carrier rejection with circuitry. The use of the differential output allows 6dB gain to be obtained while the high input impedance allows voltage step-up to be achieved.

Pin Functions

Pin	Function
13 & 12	**Signal input.** These pins may be connected together for best carrier suppression, but should not be DC coupled to any external voltage source or load.
3 & 14	**Open collector outputs.** These are connected to Vcc1, via load resistors, transformer windings, or as required.
4	**Vcc2,** normally about 2 to 3V lower than Vcc1, but for large output swings should be such that the instantaneous voltage at pins 2 and 3 is greater than Vcc2 + 2V.
5	**Local oscillator input.** The LO requirements are for approximately 200mV RMS with an impedance of about 1500Ω.
6	**The negative supply line.**
11	This is the current programming pin. It is connected to Vcc2 via a suitable value of resistor or fed from a current source. The current in at this pin is equal to the current in Pin 2 or Pin 3.

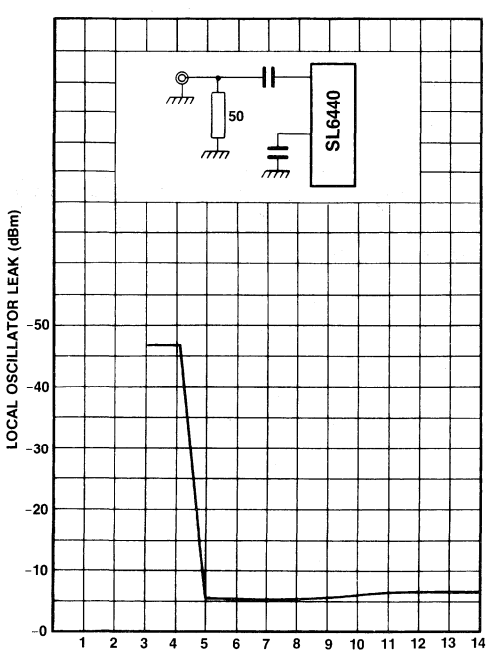


Fig.7 Local oscillator leak, LO = 31.4MHz 0dBm, Vcc1 = 15V, single ended input.

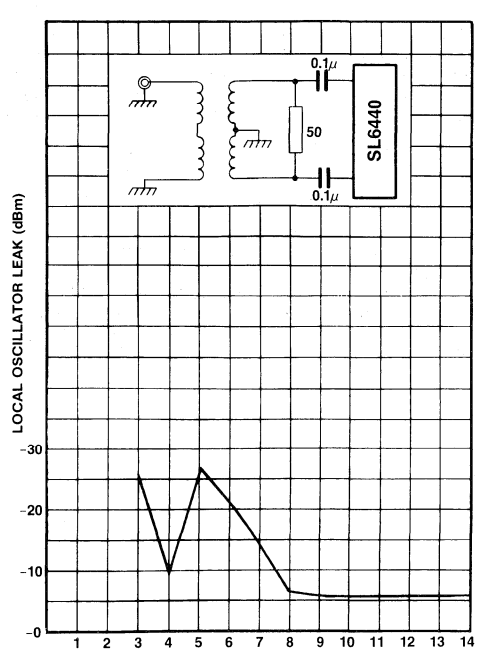


Fig.8 Local oscillator leak, LO = 31.4MHz 0dBm, Vcc1 = 15V, capacitively coupled transformer input.

THERMAL CONSIDERATIONS

The SL6440 chip temperature should not exceed 170°C. As a result of this limitation, the maximum power dissipation depends upon the thermal resistance from junction-to-ambient θ_{JA}, which is in free air, approximately 125°C/W. This may be reduced by using a suitable heat dissipator, such as the IERC PEP50AB, which reduces θ_{JA} to about 65°C/W. Dissipators designed to be attached by thermally conductive epoxy generally have a somewhat higher thermal resistance.

The dissipation is given by the expression:

$$P_{dmW} = 2\ Ip\ Vo + Vp\ IP + 0.75\ (V_{CC}2)^2 + 1.5\ V_{CC}2$$

where Vo = DC level at pin 3 or 14, Vp = Voltage on pin 11 and Ip = Programming current in mA.

Vp is approximately 3Vbe, and may be assumed for most purposes to be 2.0V. Curves given on the data sheet indicate the typical performance for given dissipations.

In many applications, it will be possible to run the mixer at a low enough dissipation to allow use with minimal heat-sinking. The circuit of Fig.11 is usable without a heatsink to +60°C under the conditions shown while a simple 'glued-on' dissipator, such as an EG & G Wakefield 651B allows operation to an ambient of +80°C. For the full military temperature range of -55°C to +125°C a dissipator similar to the IERC PEP50AB coupled with a maximum dissipation of 0.75W is required for the SL6440A to be satisfactorily cooled. Note that the SL6440C is only available for the -30 to +80°C temeperature range.

The use of forced air, thermoelectric or 'cold wall' cooling systems allows increased dissipation at high temperature where required. Nevertheless, it is good practice to maintain chip temperature below the maximum rated wherever possible.

DESIGNING WITH THE SL6440

Because of its programmable capabilities, the SL6440 needs slightly more consideration in the design of the circuitry around it than is required for simple mixers. The following parameters may be chosen, although some characters are relaxed: Gain, intercept point, compression point and dissipation.

Gain is given by the expression:

$$G = 20\ \text{Log}\ \frac{R_L\ Ip}{56.6\ Ip + 0.0785}\ \text{dB}$$

for single ended output, and is 6dB greater where a differential output is used.

R_L is the load resistance in Ohms from pin 3 or 14 to $V_{CC}2$, Ip is the programming current. Intercept point is primarily dependent upon the value of Ip and can be chosen from the graphs.

Compression point is more complex. It is more convenient to work in terms of output compression, as input compression is dependent upon the gain. The voltage on the output pins should not be so low that the output transistors can saturate. This means that the quiescent voltage on these pins must be greater than $V_{CC}2$. Should the output transistors approach saturation, the frequency response may be reduced, which is most noticeable when using the SL6440 for 'up-conversion'. The minimum value of $V_{CC}1$ is:

$$V_{CC}1\ (\text{min}) = (Ip\ R_L) + Vs + V_{CC}2$$

where

Ip is the programming current
R_L is the DC load resistance
Vs is the peak output voltage.

If $V_{CC}1$ is set such that

$$V_{CC}1 = (2\ Ip\ R_L) + V_{CC}2$$

then compression will occur at the input of the device.

The information given above, in conjunction with the data sheet allows the optimum working conditions to be decided. Because of the flexibility inherent in the SL6440, there are many possible modes of operation, but once the required circuit parameters are known, these conditions are readily determined.

The measurement techniques required for the accurate and repeatable evaluation of intermodulation performance covered in Plessey Semiconductors Radio Telecoms IC Handbook (Publication No. PS2123). When measured with a correctly designed test system, the SL6440 performance can be evaluated, while its flexibility in use coupled with its high performance offer many advantages to equipment designers.

REFERENCES

1. Mixers for High Performance Radio, Session 24, WESCON, 1981. Published by Electronic Conventions Inc., 999 N. Sepulveda Blvd., El Segundo CA.
2. CHADWICK P.E. High Performance Integrated Circuit Mixers. I.E.R.E.Conference on Radio Receivers and Associated Systems, Leeds, 1981. (I.E.R.E. Conference Publication No. 50)

SL6700 — A Versatile Radio Integrated Circuit

The SL6700 is designed for use in low voltage AM applications. However, its versatility and access to internal functional blocks allows its use in many more applications. The original use of this circuit required the incorporation of a specialised noise blanker, which is still present, and may be used if desired. The low power consumption (<60mW) of this circuit makes it ideal for a number of applications, while its design, optimised for use with ceramic filters, allows lower cost circuitry to be obtained.

The SL6700 block diagram is shown in Fig.1. The IC contains the following functions:

Amplifier 1, input on pin 18 and output on pin 3. This amplifier is AGC controlled.

Amplifier 2, input on pin 3 and output on pin 5. This amplifier is also AGC controlled, but has a lower signal handling capacity than amplifier number 1.

Double balanced mixer, input on pin 7, oscillator on pin 9 and output on pin 8. The output is an open collector, and the mixer has a 3rd order intermodulation intercept point of about -9dBm.

Monostable multivibrator, used for the noise blanker, connected to pins 11 and 12.

Amplifier and detector, input on pin 13, with AF output on pin 15.

AGC amplifier with delayed output, output on pin 5.

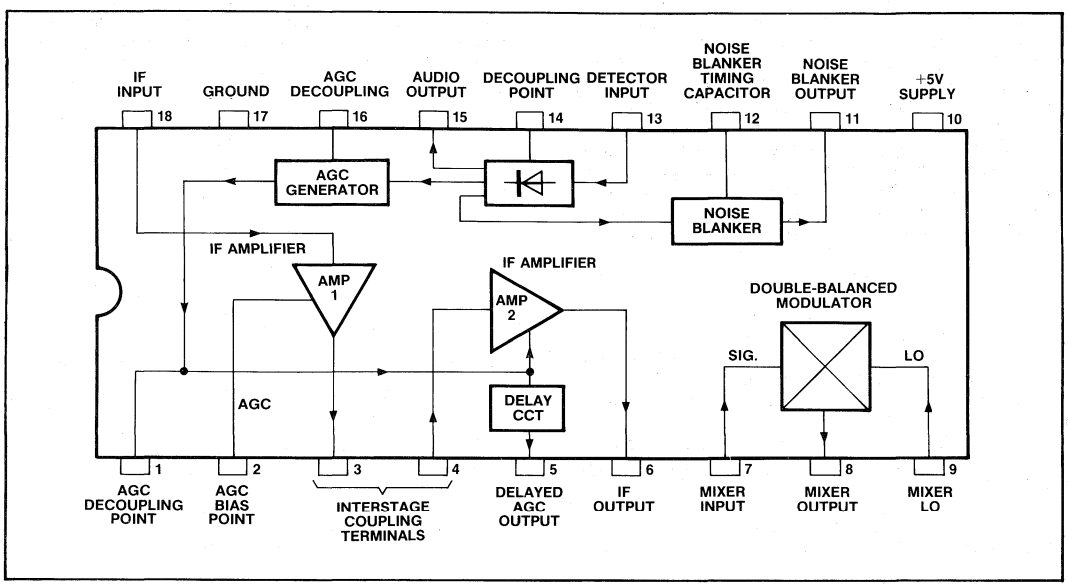


Fig.1 SL6700 block diagram

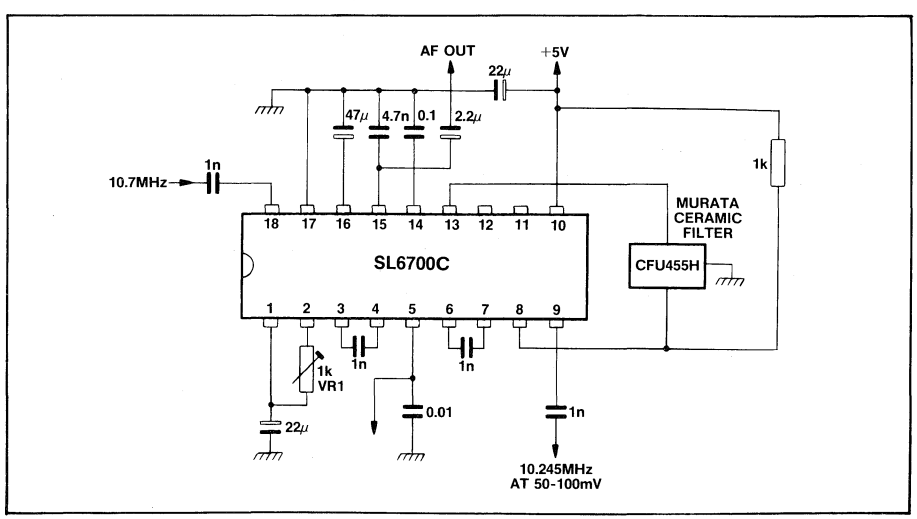


Fig.2 Double conversion IF strip 10.7MHz and 455kHz

DOUBLE CONVERSION IF STRIP (Fig.2)

The 10.7MHz input is amplified in both IF amplifiers and converted to 455kHz in the mixer. The 455kHz output is filtered in a ceramic filter, and applied to the detector input. AGC is applied to the two amplifier stages, and the 1kΩ variable resistor, RV1, is used to set the delayed AGC threshold level. This AGC output is positive going with increasing signal, and reaches a sufficient voltage to control the Plessey SL600 and SL1600 series amplifier devices.

The sensitivity of this circuit is typically 5μV RMS, with 30% modulation for a 10dB signal to noise ratio, and it will accept signals up to 100mV RMS at 80% modulation with distortion below 5%.

The frequency response of the AGC controlled amplifiers extends up to 25MHz, allowing a wide choice of IF to suit any particular requirement.

The type of detector used in the SL6700C has the great advantage of producing carrier-derived AGC. It is a full wave detector (see Fig.3) in which the input signal is an emitter coupled transistor pair with common collectors (TR53 and TR54), and the signal, phase inverted by TR50 and TR52, to the other input. TR53 and TR54 act as a full wave rectifier, and the emitters rise to a voltage determined by the input. The modulation also appears on the emitters, and is fed out via pin 15, whle a further transistor, with suitable filtering, provides the AGC voltage. The detector is extremely linear - for example, the increase in audio output from 30% to 80% modulation is 8dB, against a theoretical rise of 8.52dB.

AM BROADCAST RADIO (Fig.4)

The SL6700C is ideally suited for this application. Its high linearity and low distortion allow quality reproduction of AM broadcast signals, while the minimum of external components allows small size and low cost. TR1 is the oscillator transistor: almost any small signal NPN device will function.

C1, L1 and C2, L2 are proportioned to track - L1 may, of course, be a ferrite road aerial. The values of C1, L1, C2, L2 and C3 may be determined from any of the standard formulae (Refs. 1,2,3,4).

Where minimum component count is necessary, and degradation of selectivity may be accepted, the filter F2 may be replaced with a 100pF capacitor. Similarly, R1 and C2 may be omitted where a well-filtered supply line is available.

The input impedance of the mixer is typically 300Ω, allowing a tight coupling to the coil L1 without excessive loss of Q, which is an important consideration when using ferrite rod aerials.

The delayed AGC line is not used in this receiver and is left disconnected. However, should it be desired to produce a broadcast receiver covering the SW broadcast bands, the addition of an SL1610C RF amplifier will improve the sensitivity by a useful amount, while an extra tuned circuit will be given extra image rejection. Under these circumstances the 22kΩ resistor from pin 1 to ground should be omitted, and a 1kΩ potentiometer connected between pins 1 and 2 as in Fig.2. In the majority of cases, a 330Ω resistor will provide a suitable AGC characteristic, if some variation between ICs is not objectionable. The low supply voltage and current requirements make this ideal for portable applications.

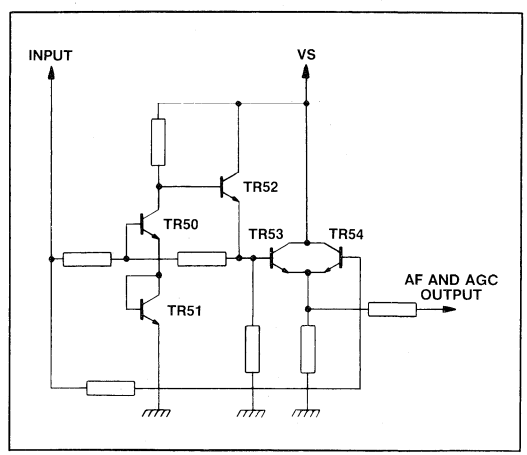


Fig.3 AM detector

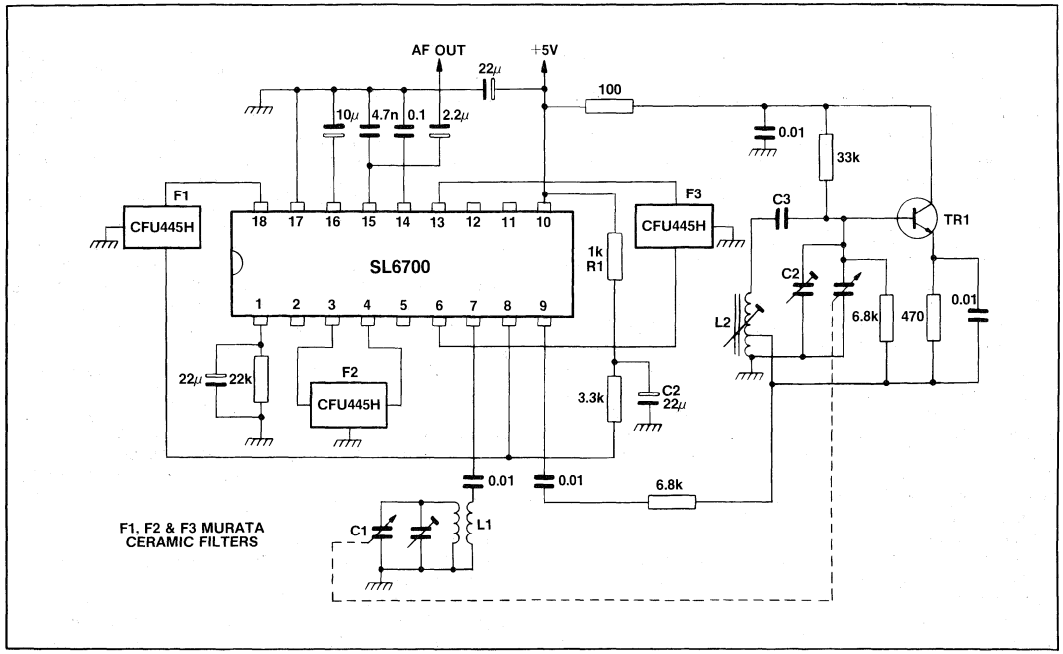


Fig.4 SL6700 AM broadcast receiver

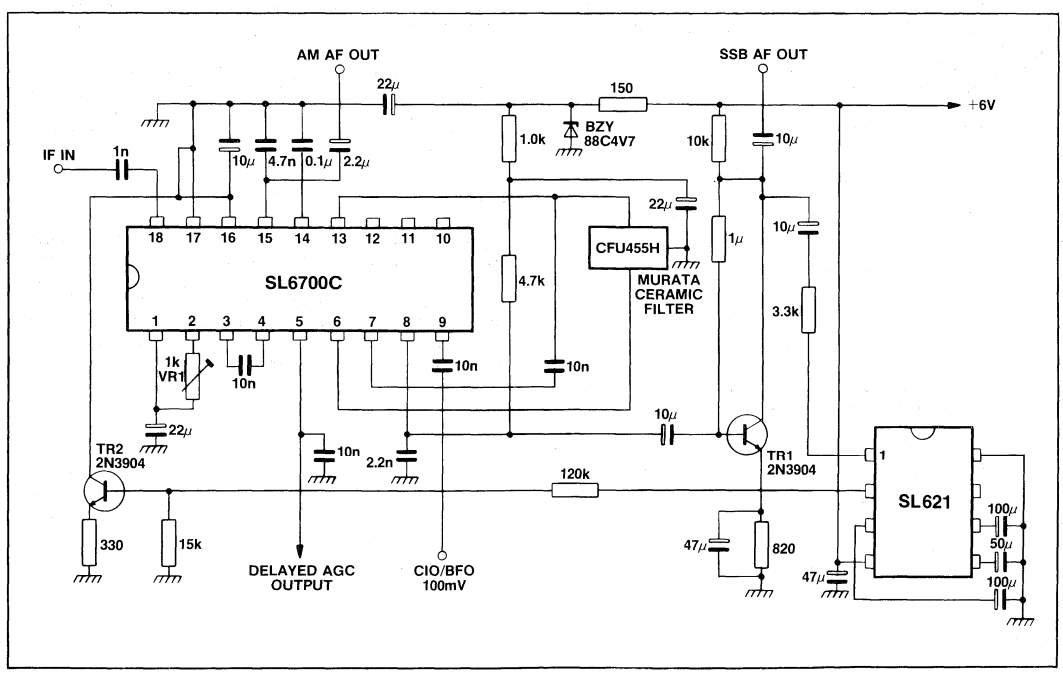


Fig.5 AM/SSB/CW IF strip

AM/SSB/CW IF STRIP (Fig.5)

This is one of the more complex applications of the SL6700C. The two gain controlled amplifiers are cascaded, and feed, via a band limiting filter, the detector and AGC circuits, and the input of the mixer, which is used as a product detector. Although a ceramic filter is shown in Fig.5, a suitable tuned circuit may be used. The load appearing across the circuit is low (1.5kΩ) and to obtain a suitable Q, it may be necessary to tap down the circuit, either by means of capacitive or inductive taps.

Because of the limited frequency response of the detector and the amplifier feeding it, this circuit is not recommended for use above 1.6MHz.

The audio output from the product detector is amplified in TR1, and the output applied to the input of an SL621 AGC generator. The output of this stage controls the internal AGC circuitry via TR2. For AM operation, the carrier insertion oscillator (or BFO for CW) is switched OFF, and as a result, there is little output from the product detector. The AM detector and AGC thus work normally, while the SL621 provides no output. In the SSB/CW modes, the product detector output activates the SL621, and the AGC is 'taken over' by this stage. However, RF derived AGC is still applied in the event of strong signals at zero beat. R1 was chosen to set the outputs on AM and SSB approximately equal for single SSB and 80% modulated AM signals respectively.

Although selectivity will usually be obtained by means of block filters, it often happens that provision of a multi-element filter for CW reception is not viable, although some narrowing of the passband from the SSB condition is required.

Under these conditions, a useful narrowing of the passband can be obtained by replacing the capacitor between pins 3 and 4 with a suitable selective network, such as Fig.6. With a quartz crystal, this gives a very narrow peak to the passband, and the use of a single ceramic resonator may be preferred (at 455kHz). At 1.4MHz or 1.6MHz, the 2200pF capacitor should be reduced to around 470pF, and the response will be less sharp then at 455kHz, but will still be found to be adequately narrow.

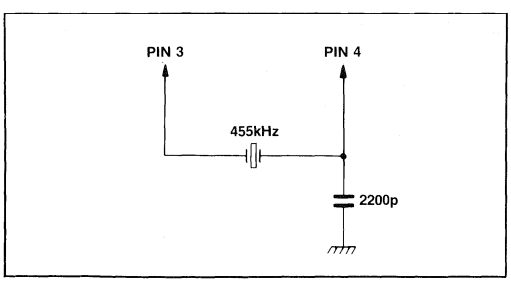


Fig.6 CW selectivity network

The AM and SSB outputs should be kept completely separate, and should be switch selected. During AM reception, the BFO/CIO must be switched OFF to avoid heterodyne interference and production of audio derived AGC. For CW reception only the circuit in Fig.9 may be used. The SL621C is designed for use as a fast attack SSB AGC generator, and, because of the large capacitors used, draws a large transient current from the supply when an SSB signal is first applied. To avoid instability, pin 4 of this device, the supply pin should be decoupled by a 47μF capacitor with short leads. In this connection, it must be remembered that a capacitor mounted on a PCB with long, thin tracks connected to it may have an appreciable increase in its ESR (Equivalent Series Resistance). The decoupling of the product detector output load (1kΩ and 47μF connected to the 4.7kΩ load at pin 6) gives an appreciable reduction in supply line noise, and should not be omitted.

The SL6700 has, unlike some ICs attempting to offer similar facilities proved remarkably 'tame', and provided sensible layouts and grounding are attained, should not give any problems with instability. In fact, attempts to use one of the amplifiers as an oscillator have proved rather fruitless - unusual phenomena to many IC users.

Nevertheless, under some conditions, the SL6700 may give the impression of instability at low signal levels. This manifests itself as a heterodyne whistle at low inputs, typically around 5μV. This is caused by some samples of the ceramic filter from pin 6 to 13 appearing to ring, and substitution of a tapped tuned circuit obviates these problems.

The performance of the AM/SSB/CW strip is set out in Table 1. The ultimate signal to noise ratio on SSB is not exceptionally high, but is adequate for all except the highest grade of point-to-point, independent sideband type communications. Intermodulation products were typically at -30dB representing 3% distortion, and are thus better than those of most received transmissions.

For designers of battery operated equipments, the low power requirements of the SL6700/SL621 combination (typically 90mW), combined with the small size and simplicity of use, after an attractive method of obtaining high performance.

SSB GENERATOR (Fig.7)

This is perhaps the most unusual application for a device designed for use in receivers. It is possible to obtain simple circuits offering adequate quality SSB, with no adjustments - a time consuming and expensive part of production. Indeed, it is considered that in many companies, the real cost of a trimming potentiometer is £2 - £3 ($4 - $6) when consideration is given to the real cost of adjustment by skilled testers.

Parameter	AM mode	SSB mode	Notes
Sensitivity	7dB SND/ND 15dB SND/ND	15dB SND/ND	5μV RMS input,m = 0.3 5μV RMS input, m = 0.8
AF output	42mV RMS -	- 43mV RMS	5μV RMS input, m = 0.8, fm = 1kHz f audio 1kHz
AGC	4dB	5dB	Change in AF output from 5μV to 100mV RMS input
Distortion	2.8 %	- 4.2 %	V_{IN} = 100mV RMS, m = 0.8 at 1kHz V_{IN} = 100mV RMS, f_{OUT} = 1kHz
Signal-Noise Ratio at higher inputs	28dB 36dB -	- - 35dB	V_{IN} 50μV, m = 0.3 V_{IN} = 50μV, m = 0.8 V_{IN} = 50μV, f_{OUT} = 1kHz
Ultimate Signal to Noise ratio	50dB	40dB	V_{IN} = 100mV RMS

Table 1 Results obtained from Fig.5

The SL6270 is a Voice Operated Gain Adjusting Device (VOGAD) which maintains a constant output level for a wide range of inputs. The input may be fed differentially, if desired, by removing the 2.2μF capacitor from pin 5 and feeding between pins 4 and 5. The usual precautions should be taken against RF pickup in transmitter, and bypass capacitors of 10nF should be provided on the inputs.

The mixer of the SL6700 is used as a balanced modulator, giving some 20dB of carrier suppression. The SSB filter gives another 20-25dB to produce an acceptable signal. (-40dB relative to each tone, -46dB rel. PEP is the usual professional standard). Rt and Ct are the termination components for the filter and should be chosen accordingly. However, impedances in the range 1-4kΩ are preferred. Less than 1kΩ gives greater loss in the balanced modulator, thus degrading carrier suppression, and more than 4kΩ needs other techniques to maintain the DC feed to the mixer. However, filters at 455kHz such as the Collins 526-9939-010, with Rf at 2.7kΩ and Ct at 360pF give very good results - see Table 2. At 1.4MHz, stray capacitances make the carrier leak somewhat worse, but still usable. Suitable filters at this frequency are the Cathodeon BP4707/BP4708, which require values of Rt = 1kΩ and Ct = 15pF. At 1.4MHz, it may prove useful to connect a 6.8kΩ resistor in series with pin 18 of the SL6700, breaking a ground loop through the low Z22 of the filter, minimising degradation of the carrier suppression.

The value of R1 should be set at the design stage. This resistor controls the input to the detector stage, and thus the amount of AGC produced, so setting the gain of the first amplifier. The value of this resistor sets the ALC threshold, and values vary from 47kΩ at 1.4MHz to 120kΩ at 455kHz, depending on the desired output and amount of ALC required. An additional ALC input is available at pin 13: feeding in an ALC voltage derived from later in the transmitter via a suitable resistor will give a multiple level ALC action. The 47μF capacitor from pin 15 sets the ALC time constant, and should not be reduced: otherwise distortion will introduced. The 1kΩ resistor from pin 3 to ground increases the current through the emitter follower driving this pin, and allows an undistorted output to be obtained in as low an impedance as 50Ω.

For transceiver use, the switching required between receive and transmit is probably too complex to be economical, and the use of two SL6700s with a switched filter is recommended.

Typical results are shown in Table 2.

Parameter	455kHz	1.4MHz	Notes
Carrier Suppression	50dB	46dB	Relative PEP
3rd order IMD	-40dB	-40dB	Relative each tone of a 2 tone signal, with separations down to 50Hz.
2nd order IMD	-43dB	-38dB	as 3rd order
Output Level	200mV pk-pk	200mV pk-pk	Into 600Ω load
Carrier Level	50mV	50mV	RMS
Audio Level	30mV	30mV	RMS input to SL6700 pin 7

Table 2 Results of the SSB generator in Fig.7

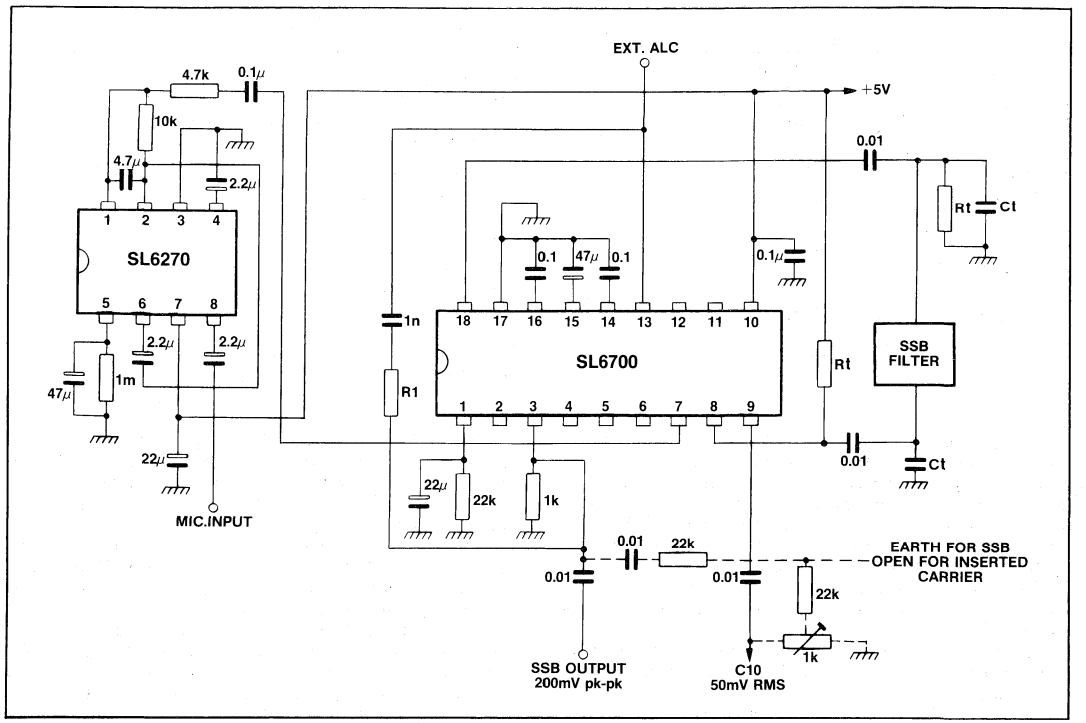


Fig.7 SL6700 SSB generator

Shown dotted in Fig.7 is a means of re-inserting carrier for A1A, J2H, J3A or J3H operation. The level of the carrier is set by the potentiometer: however, care should be exercised in the return from the carrier switch to avoid earth loop currents. For J3H operation, it is recommended that the carrier be set between -4 and -5dB rel. PEP to avoid excessive distortion at modulation peaks. To obviate carrier 'pumping' (carrier level being dependent on AF level) no more than 2 or 3dB of ALC should be used.

Use of this circuit above 1.6MHz requires care for several reasons. Firstly, the balance of the balanced modulator degrades, and, secondly, the ALC detector sensitivity falls. However, it may, by careful design and layout prove practicable up to about 12MHz. By decreasing R1, the fall in sensitivity of the detector and its amplifier may be compensated, but filters at this frequency do not generally have the carrier suppression obtainable at lower frequencies. Nevertheless, acceptable results may be obtained at 9MHz. For a very simple SSB generator, the 'spare' amplifier in the SL6700C may be used as a VOGAD, although the input range is limited. However, the circuit shown in Fig.8 produces very effective results for simple low power SSB generation - and will run effectively with power levels of the order of 50mW drawn from the supply. This makes the circuit attractive for hand held CB, manpacks etc., where power consumption is extremely important.

Despite these minor disadvantages, the advent of low cost ceramic and mechanical filters at 455kHz designed for CB use, offer, with the SL6700, a low cost 'no adjustment' system drawing low power while performing adequately for the majority of SSB applications.

MODEL CONTROL

The majority of RC models are operated on the 27MHz band. At this frequency, the SL6700 performs quite adequately - see Fig.9. However, for many applications, operation from a lower voltage is necessary, and some redesign of Fig.9 would be required. Nevertheless, the advantage of the SL6700 in this application is that operation at 4.5V presents no difficulty to the IC, and so only circuits such as the oscillator need to be altered. For minimum component count R1 may be omitted, and L1 and the 56pF and 1nF input capacitors replaced by a ceramic filter such as the Murata SFE 27MA4. Should greater sensitivity be required, a transmistor RF amplifier and another ceramic filter would give the required increase. The low current consumption (typically 5mA at 4.5V) of the SL6700 is a decided advantage in this application.

The SL6700 supply voltage is best fixed at 4.5V-5.0V although operation up to 6V is generally practicable. The supply should not exceed 7V een momentarily as permanent damage may result.

The SL6700 is a versatile linear integrated circuit, providing an extremely wide range of RF applications in the HF range.

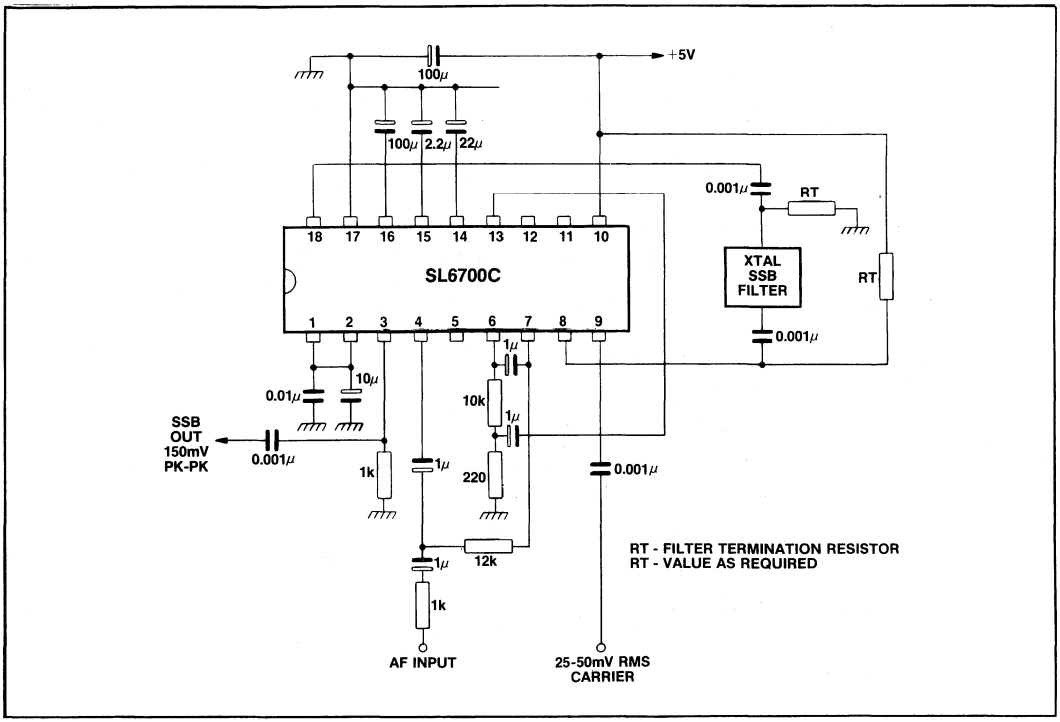


Fig.8

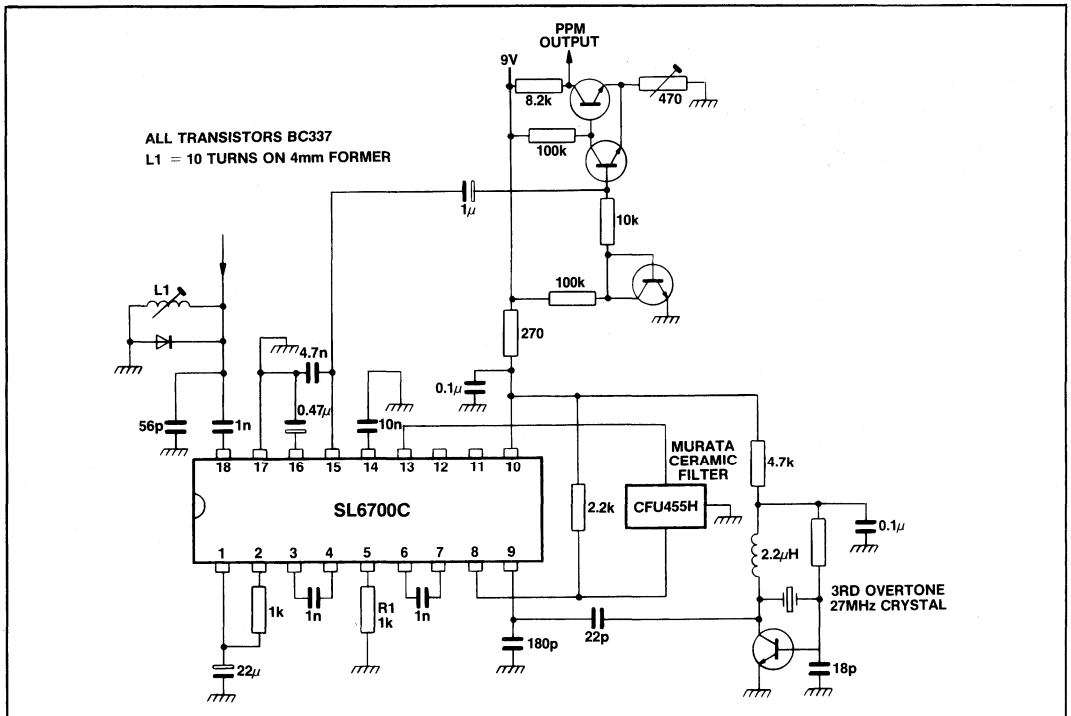


Fig.9 27MHz remote control receiver

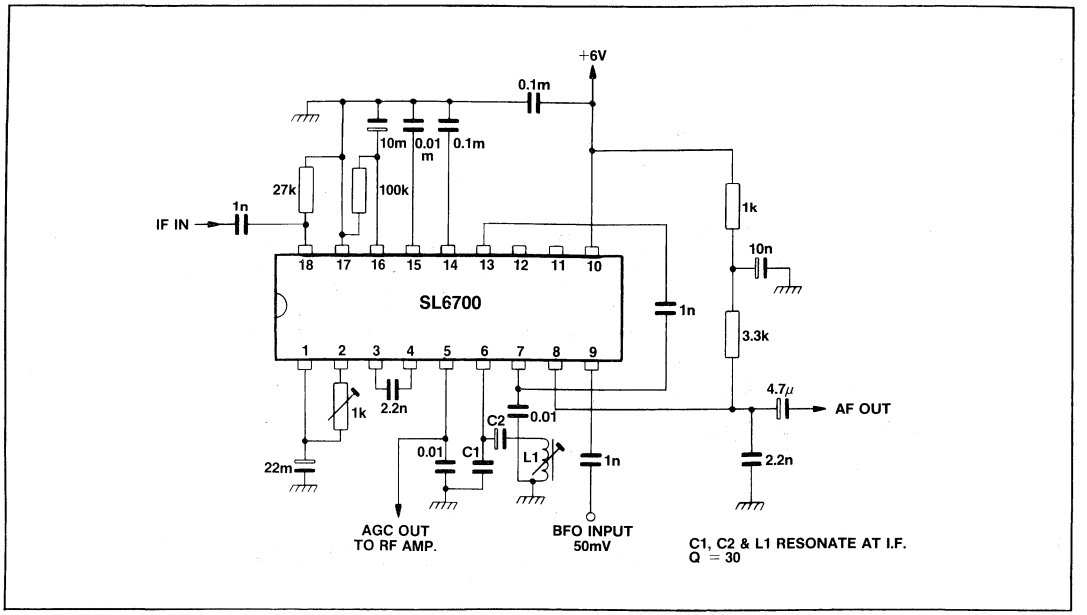


Fig.10 SL6700 CW receiver

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Intermodulation, Phase Noise and Dynamic Range

The radio receiver operates in a non-benign environment. It needs to pick out a very weak wanted signal from a background of noise at the same time as it rejects a large number of much stronger unwanted signals. These may be present either fortuitously, as in the case of the overcrowded radio spectrum, or because of deliberate action, as in the case of Electronic Warfare. In either case, the use of suitable devices may considerably influence the job of the equipment designer.

Dynamic range is a 'catch all' term, applied to limitations of intermodulation or phase noise: it has many definitions depending upon the application. Firstly, however, it is advisable to define those terms which limit the dynamic range of a receiver.

INTERMODULATION

This is described as the *'result of a non linear transfer characteristic'*. The mathematics have been exhaustively treated, and Ref.1 is recommended to those interested.

The effects of intermodulation are similar to those produced by mixing and harmonic production, insofar as the application of two signals of frequencies f_1 and f_2 produce outputs of $2f_2 - f_1$, $2f_1 - f_2$, $2f_1$, $2f_2$ etc. The levels of these signals are dependent upon the actual transfer function of the device and thus vary with device type. For example, a truly square law device, such as a perfect FET, produces no third order products ($2f_2 - f_1$, $2f_1 - f_2$). Intermodulation products are additional to the harmonics $2f_1$, $2f_2$, $3f_1$, $3f_2$ etc. Fig.1 shows intermodulation products diagrammatically.

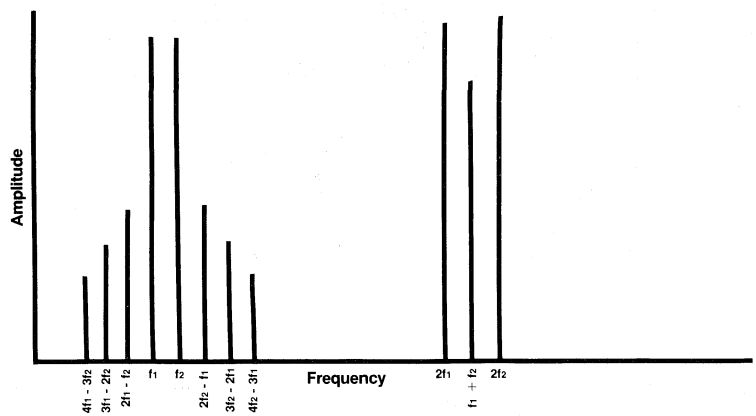

Fig.1 Intermodulation products

The effects of intermodulation are to produce unwanted signals, and these degrade the effective signal to noise ratio of the wanted signal. Consider firstly the discrete case of a weak wanted signal on 7.010MHz and two large unwanted signals on 7.020 and 7.030MHz. A third order product (2 x 7.02 - 7.03) falls on the wanted signal, and may completely drown it out. Fig.2 shows the total HF spectrum from 1.5 to 41.5MHz and Fig.3 shows the integrated power at the front end of a receiver tuned to 7MHz. It may be seen that just as white light is made up from all the colours of the spectrum, so the total power produced by so many signals approximates to a large wide band noise signal. Now, it has already been shown that two signals, f_1 and f_2, produce third order intermodulation products of $2f_1 - f_2$ and $2f_2 - f_1$. The signals will produce third order products somewhat greater in number, viz: $2f_1 - f_2$, $2f_1 - f_3$, $2f_2 - f_1$, $2f_2 - f_3$, $2f_3 - f_1$ and $2f_3 - f_2$. An increase in the number of input signals will multiply greatly the effects of intermodulation, and will manifest as a rise in the noise floor of the receiver.

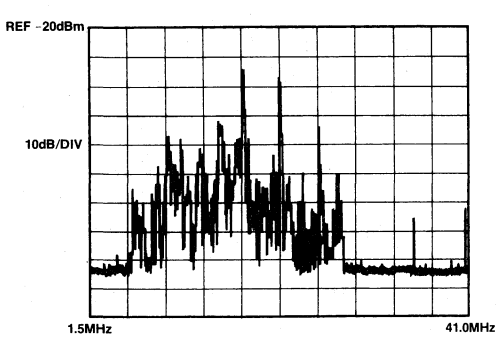

Fig.2

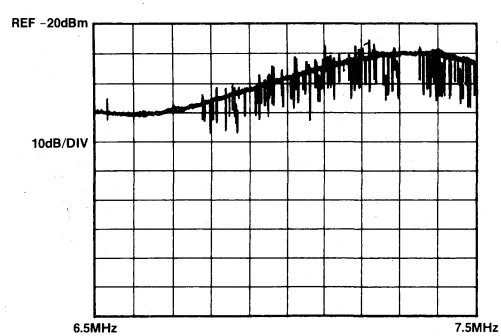

Fig.3

The amplitude relationships of the third order intermodulation products and the fundamental tones may be derived from Ref.1, where it is shown that the intermodulation product amplitude is proportional to the cube of the input signal level. Thus an increase of 3dB in input level will produce an increase of 9dB in the levels of the intermodulation products. Fig.4 shows this in graphic form, and the point where the graphs of fundamental power and intermodulation power cross is the *Third Order Intercept Point*.

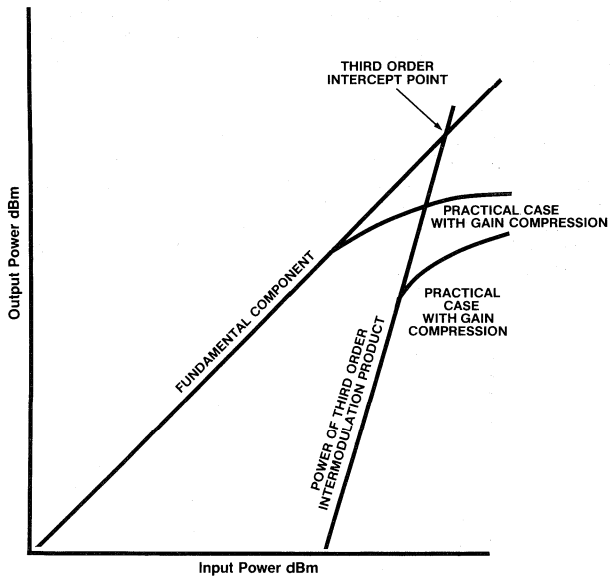

Fig.4 3rd order intercept

The third order intercept point is, however, a purely theoretical concept. This is because the worst possible intermodulation ratio is 13dB (Ref.2), so that in fact the two graphs never cross. In addition, the finite output power capability of the device leads to *Gain Compression*.

Thus, it is apparent that the intermodulation produced noise floor in a receiver is related to the intercept point. Figs.5, 6 and 7 show the noise floor produced by various intercept points, in a receiver fed from an antenna - a realistic test! Fig.5 shows that a large number of signals are below the noise floor and are thus lost; this represents a 0dBm intercept point. Fig.7 shows a +20dBm intercept noise floor, and it is obvious that many more signals may be received.

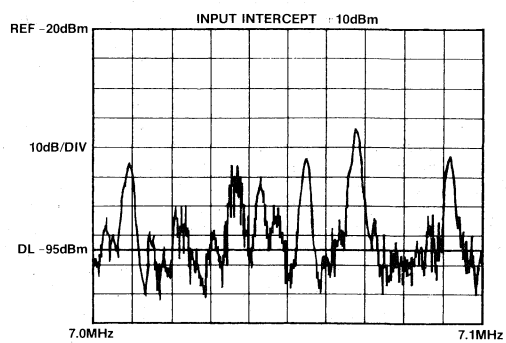

Fig.6

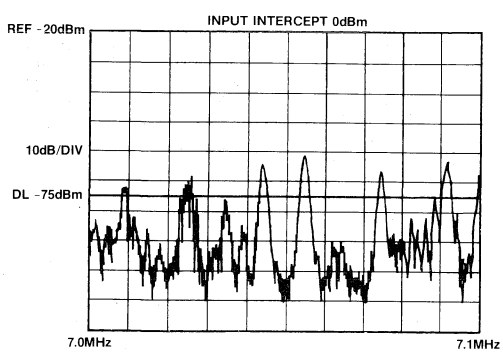

Fig.5

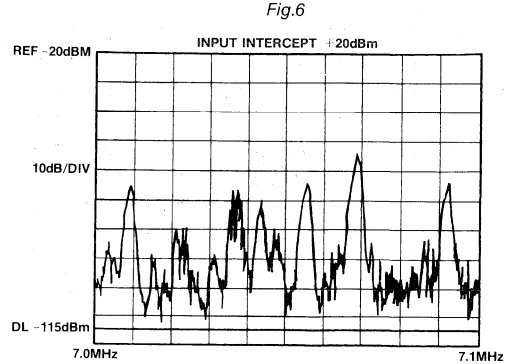

Fig.7

Because of the rate at which intermodulation products increase with input level (3dB on the intermodulation products for 1dB on the fundamental), the addition of an attenuator at the front end can improve the signal to noise ratio, as an increase in attenuation of 3dB will reduce the wanted signal by 3dB, but the intermodulation will decrease by 9dB. However, it is a fair comment that aerial attenuators are an admission of defeat, as suitable design does not require them!

The concept of dynamic range is often used when discussing intermodulation. Fig.8 shows total receiver dynamic range, which is defined as the spurious Free Dynamic Range. Obviously an intermodulation product lying below the receiver noise floor may be ignored. Thus the usable dynamic range is that input range between the noise floor and the input level at which the intermodulation product reaches the noise floor. In fact

$$DR = \frac{2}{3}(I_3 - NF) \qquad \ldots (1)$$

Where DR is the dynamic range in dB
I_3 is the intermodulation input intercept point in dBm
NF is the noise floor in dBm.

Note that in any particular receiver, the noise floor is related to the bandwidth; dynamic range is similarly so related.

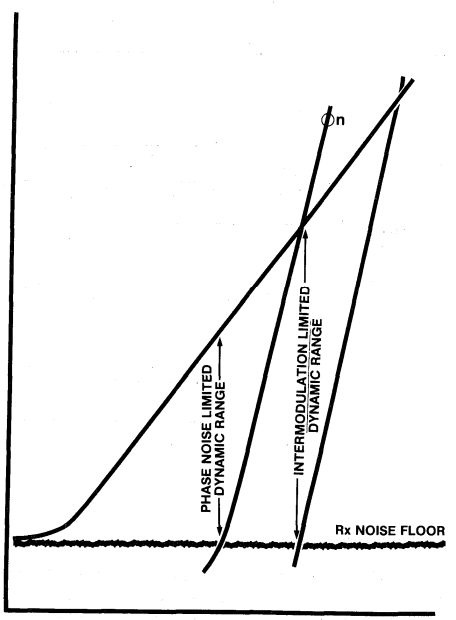

Fig.8

HF receivers will often require input intercept points of +20dBm or more. The usable noise factor of HF receivers is normally 10-12dB: exceptionally 7 or 8dB may be required when small whip antennas are used. An SSB bandwidth would have a dynamic range from (1) of 105.3dB. The same receiver with a 100Hz CW bandwidth would have a dynamic range of 114.6dB and thus dynamic range is quite often a confusing and imprecise term.

Appendix A defines a quantitive method of Intermodulation Noise Floor assessment, developed later than the data in Figs.5 to 7.

VHF receivers require noise figures of 1 or 2dB for most critical applications, and where co-sited transmitters are concerned, signals at 0dBm or more are not uncommon. However, such signals are usually separated by at least 5 % in frequency and filters can be provided. Close-in signals at levels of -20dBm are not uncommon, and dynamic ranges in SSB bandwidths of about 98dB are required.

The achievement of high input intercept points and low noise factors is not necessarily easy. The usual superhet architecture follows the mixer with some sort of filter, frequently a crystal filter, and the performance of this filter may well limit the performance. Crystal filters are not the linear reciprocal two-port networks that theory suggests, being neither linear nor reciprocal. It has been suggested that the IMD is produced by ferrite cored transformers, but experiments have shown that ladder filters with no transformers suffer similarly. Thus, although ferrite cored transformers can contribute, other mechanisms dominate in these components. The most probable is the failure of the piezo-electric material to follow Hooke's Law at high input levels, and possibly the use of crystal cuts other than AT could help insofar as the relative mechanical crystal distortion is reduced. The use of SAW filters is attractive, since they are not bulk wave devices and do not suffer to such an extent from IMD; however, it is necessary to use a resonant SAW filter to achieve the necessary bandwidths and low insertion losses.

The design of active components such as amplifiers is relatively straightforward. Amplifiers of low noise and high dynamic range are fairly easy to produce, especially with transformer feedback, although where high reverse isolation is required, care must be taken. Mixers are however, another matter.

Probably the most popular mixer is the diode ring (Fig.9). Although popular, this mixer does have some drawbacks, which have been well documented. These are:

Insertion loss (normally about 7dB)
High LO drive power (up to +27dBm)
Termination sensitive (needs a wideband 50Ω)
Poor interport isolation (40dB)

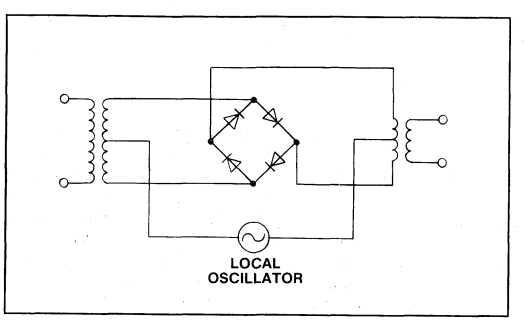

Fig.9 Diode ring

The insertion loss is a parameter which may be classed merely as annoying, although it does limit the overall noise figure of the receiving system. The high LO drive power means a large amount of DC is required, affecting power budgets in a disastrous way, while termination sensitivity may mean the full potential of the mixer cannot be realised.

For the diode ring to perform adequately, a good termination 'from DC to daylight' is required - definitely at the image frequency (LO ± sig. freq.) - and preferably at the harmonics as well. Finally, interport isolation of 40dB with a +27dBm LO still leaves -13dBm of LO radiation to be filtered or otherwise suppressed before reaching the antenna.

A further problem with the simple diode ring of this form is that the 'OFF' diodes are only off by the forward voltage drop of the ON diodes. Thus the application of an input which exceeds this OFF voltage leads to the diodes trying to turn ON, giving gain compression and reduced IMD performance.

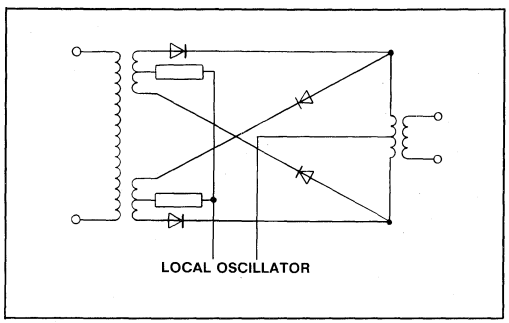

Fig.10 Resistive loaded high intercept point mixer

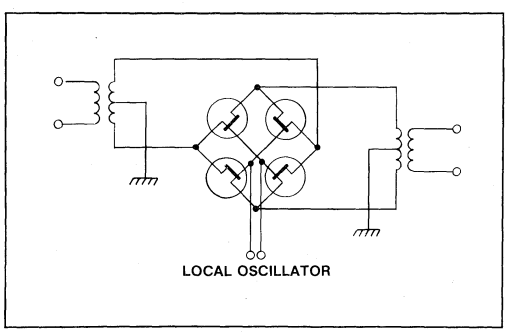

Fig.11 Quad MOSFET commutative mixer

Fig.10 shows a variation of this in which series resistors are added. The current flow through these resistors increases the reverse bias on the OFF diodes which gives a higher gain compression point: such a mixer can give +36dBm intercept points with a +30dBm of LO drive. Nevertheless, as is common to all commutative mixers, the intermodulation performance is related to the termination, and the LO radiation from the input port is relatively high.

Variations of this form of mixer include the Rafuse Quad MOSFET mixer of Fig.11, which suffers with many of the same problems. Fig.12 shows a dual VMOS mixer capable of good performance, but requiring a large amount of DC power and with limited isolation of the LO injection.

Many advantages accrue to the choice of the transistor tree type of approach (Fig.13). Here the input signal produces a current in the collectors of the lower transistors and this current is commutated by the upper set of switching transistors. Because the current is to a first order approximation independent of collector voltage, the transistor tree does not exhibit the sensitivity to load impedance that the diode ring does, and indeed, by the use of suitable load impedances, gain may be achieved. The non-linearity of the voltage to current conversion in the base emitter junctions of the bottom transistors is the major cause of intermodulation, but by using suitably large transistors and emitter degeneration, very high performances (+32dBm input intercept) can be achieved. The Plessey SL6440 has been described (Refs.3, 4, 5) and uses these techniques to achieve a high standard of performance (see Fig.16).

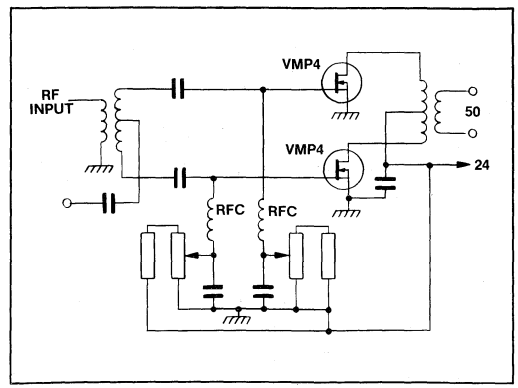

Fig.12 VMOS mixer

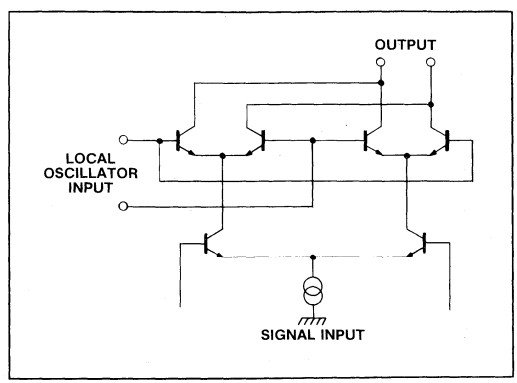

Fig.13 The transistor tree

PHASE NOISE

The mixing process for the superhet receiver is shown in Fig.14, where an incoming signal mixes with the local oscillator to produce the intermediate frequency. Fig.15 shows the effect of noise modulation on the LO, where the noise sidebands of the LO mix with a strong, off channel signal to produce the IF. This means that the phase noise performance of the LO affects the capability of the receiver to reject off channel signals, and thus the receiver selectivity is not necessarily defined by the signal path filters. This phenomena is referred to as *Reciprocal Mixing*, and has tended to become more prominent with the increased use of frequency synthesisers in equipments.

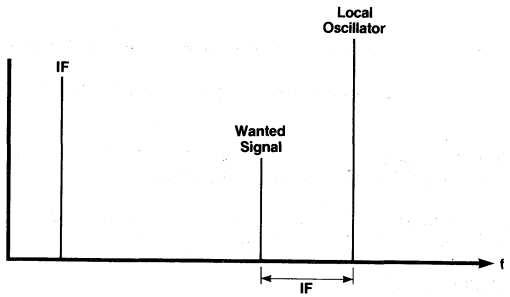

Fig.14 Superhet mixing

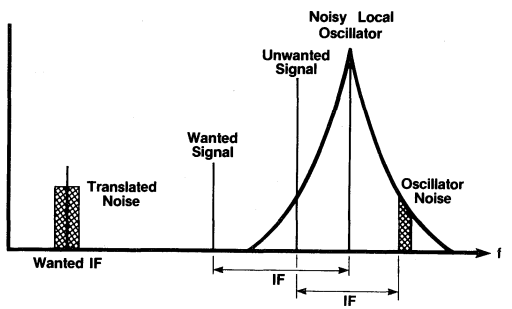

Fig.15 Reciprocal mixing

The performance level requirements of receivers is dependent upon the application. Some European mobile radio specifications call for 70dB of adjacent channel rejection, equating to some -122dBc/Hz, while an HF receiver requiring 60dB rejection in the adjacent sideband needs -94dBc/Hz at a 500Hz offset. The use of extremely high performance filters in the receiver can be completely negated if the phase noise is poor. For example, a receiver using a KVG XF9B filter with a rejection in the unwanted sideband of 80dB at 1.2kHz, would require a local oscillator with -114dBc/Hz phase noise at 1.2kHz if the filter performance was not to be degraded.

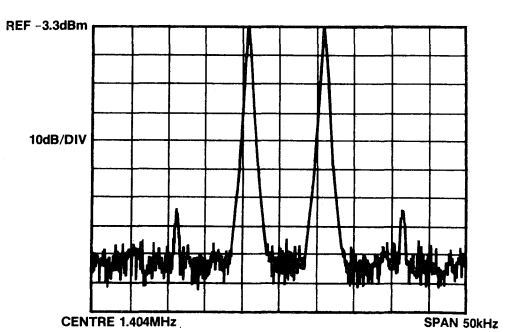

Fig.16 SL6440 intermodulation performance

To put these levels in perspective, relatively few signals generators are adequate to the task of being the LO in such a system. For example, 'Industry Standards' like the HP8640B are not specified to be good enough: neither are the HP8642, Marconi 2017/2018, or Racal 9082, all of which are modern, high performance signal generators.

All this suggests that it is very easy to over-specify a receiver in terms of selectivity, and simple synthesisers are not necessarily ideal in all situations.

The ability of the receiver to receive weak wanted signals in the presence of strong unwanted signals is therefore determined not only by the intermodulation capabilities of the receiver, but by phase noise and filter selectivity.

The usual approach to high performance synthesis has used multiple loops for good close-in performance. Notable exceptions are those equipments using fractional N techniques with a single loop. Nevertheless, such equipments not generally specified as highly as multi-loop synthesisers. A vital part of the synthesiser is still the low noise VCO, for which many approaches are possible. This VCO performance should not be degraded by the addition of the synthesiser: careful choice of technologies is therefore essential. For example, Gallium Arsenide dividers are much worse in phase noise production than silicon, and amongst the silicon technologies, TTL is better than ECL.

From equation (1)

$$DR = \frac{2}{3}(I_{p3} - NF)\ \text{dB}$$

where I_{p3} = input intercept point dBm
NF = noise floor dBm

The phase noise governed dynamic range is given by

$$DR_{\Phi} = P_n + 10\log_{10}B\ Db \qquad (2)$$

Where P_n is the phase noise spectral density in dBc/Hz at any offset and B is the IF bandwidth in Hz.

(N.B. This is not quite correct if B is large enough such that noise floor is not effectively flat inside the IF bandwidth).

Ideally the ratio

$$\frac{DR_{IM}}{DR_{\Phi}}$$

should be 1 in a well designed receiver - i.e. the dynamic range limited by phase noise is equal to the dynamic range limited by intermodulation.

Certain aspects of low noise synthesiser design have been touched upon and Ref.6 provides further information.

The performance of a receiver in terms of its capabilities to handle input signals widely ranging in input level is dependent upon the receiver capability in terms of intermodulation and phase noise. Neglect of either of these parameters leads to performance degradation, and it has been shown that specifications are not only often difficult to meet, but sometimes contradictory in their requirements.

This paper was first presented at the RF Technology Expo, Anaheim, Jan 1986.

P.E. Chadwick

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APPENDIX A

Intermodulation is caused by odd order curvature in the transfer characteristic of a device. If two signals f_1 and f_2 are applied to a device with third order term in its transfer characteristic, the products are given by:

$(\text{Cos}f_1 + \text{Cos}f_2)^3 = \text{Cos}^3f_1 + 3\text{Cos}^2f_1\,\text{Cos}f_2 + 3\text{Cos}f^2f_2\,\text{Cos}f_1 + \text{Cos}^3f_2$

from the trig identities Cos^3A, Cos^2A and CosACosB, this is

$\frac{1}{4}\text{Cos}^3f_1 + \frac{3}{4}\text{Cos}f_1 + \frac{3}{2}\text{Cos}^2f_1\text{Cos}f_2 + \frac{3}{2}\text{Cos}f_1\text{Cos}^2f_2 + \frac{3}{4}\text{Cos}f_2 + \frac{1}{4}\text{Cos}^3f_2 + \frac{3}{4}\text{Cos}f_2$

(where $f_1 = A$ and $f_2 = B$). Neglecting coefficients, the terms $\text{Cos}^2f_1\,\text{Cos}f_2$ and $\text{Cos}f_1\,\text{Cos}^2f_2$ are equal to

$\text{Cos}(2f_1 + f_2) + \text{Cos}(2f_1 - f_2)$ and
$\text{Cos}(2f_2 + f_1) + \text{Cos}(2f_2 - f_1)$

By inspection, it may be seen that frequencies of f_1, f_2, $3f_1$,$3f_2$, $(2f_1 \pm f_2)$ and $(2f_2 \pm f_1)$ are present in the output. Of these, only $2f_2 - f_1$, and $2f_1 - f_2$ are close to wanted frequencies f_1 and f_2.
The application of three signals f_1, f_2 and f_3, produces a similar answer, in that the resulting products are:

$3f_1$, $3f_2$, $3f_3$, $f_1 + f_2 + f_3$, $f_1 + f_2 - f_3$, $f_1 - f_2 + f_3$, $f_1 - f_2 - f_3$, $f_2 - f_1 + f_3$, $f_2 - f_1 - f_3$, $-f_1 - f_2 - f_3$, $-f_1 - f_2 + f_3$

in addition to the products

$2f_1 \pm f_2$, $2f_2 \pm f_1$, $2f_2 \pm f_3$, $2f_3 \pm f_2$, $2f_1 \pm f_3$, $2f_3 \pm f_1$

if a greater number of signals are applied such that the input may be represented by:

$\text{Cos}f_1 + \text{Cos}f_2 + \text{Cos}f_3 + \text{Cos}f_4 \ldots \text{Cos}f_n$

The result from third order curvature can be calculated from:

$(\text{Cos}f_1 + \text{Cos}f_2 + \text{Cos}f_3 + \text{Cos}f_4 \ldots \text{Cos}f_n)^3$

This expansion produces terms of

$\text{Cos}(f_1 \pm f_2 \pm f_3)$, $\text{Cos}(f_1 \pm f_2 \pm f_4)$, $\text{Cos}(f_1 \pm f_2 \pm f_n)$ etc from which it can be seen that the total number of products is:

$$\frac{n!}{3!(n-3)!} = 4 \times \tfrac{1}{6}n\,(n-1)(n-2)$$

(The factor of 4 appears because each term has four possible sign configuratons i.e. $\text{Cos}(f_1 + f_2 + f_3)$, $\text{Cos}(f_1 + f_2 - f_3)$ etc). This agrees with Ref A1.
By a similar reasoning, n signals produce:

$2n(n-1)$ products of the form $(2f_1 \pm f_2)$ $(2f_2 \pm f_1)$ etc and n 3rd harmonics.

Thus the total number of intermodulation products produced by third order distortion is:

$$n + 2n(n-) + \tfrac{2}{3}n\,(n-1)(n-2) \qquad (1)$$

Reduction of the input bandwidth of the receiver modifies this. Consider, for example, a receiver with sub-octave filters, rather than the 'wide-open' situation analysed above. In this case, the third harmonics produced by any input signals will not fall within the tune band, as will some of the products such as $f_1 + f_2 + f_3$, $f_1 - f_2 - f_3$, etc. In this case, the total number of intermoduation products is reduced. There are only three possible sets of products of the form f_1 $f_1 \pm f_2 \pm f_3$, i.e. $f_1 + f_2 - f_3$, $f_1 - f_2 + f_3$ and $f_3 - f_1 - f_2$ which can give products within the band. Note that for products to be considered, they must have an effective input frequency at the receiver mixer equivalent to an on-tune desired signal. In addition, products of the form $2f_1 + f_2$, $2f_2 + f_1$ etc are again out of band. Thus half of the $2n\,(n-1)$ products of this class are not able to cause problems and the total number of products to be considered is now:

$$n\,(n-1) + \tfrac{1}{2}n\,(n-1)(n-2) \qquad (2)$$

This result does not agree with Barrs (Ref A2) who uses the results in (1). The results in (2) are an absolute worst case, insofar as a number of the intermodulation products are out of band.

(For the purposes of this analysis, IMD in a mixer is assumed to produce an 'on tune' signal. Thus not all the possible intermodulation frequencies appearing in a half octave bandwidth will be able to interfere).

The same arguments apply to narrower front end bandwidths. However, the narrower the front end bandwidth, the higher is the probability that the distribution of signals will produce IMD products outside the band. For example, a receiver with ±2.5% front end bandwidth tuned to 10MHz will accept signals in a band from 9.75 to 10.25MHz. Signals capable of producing a product of the form $2f_1 - f_2$ must have one of the signals (f_1 or f_2) in the band 9.875 - 10.25 for a product to appear on tune. Thus the two signal apparent bandwidth is less than would be expected. Similar constraints apply to the $f_1 + f_2 - f_3$ product.

Similar arguments apply to other orders of curvature. Second order curvature, for example, will not produce any products in band for input bandwidths of less than 2:1 in frequency ratio.

The actual levels of intermodulation produced can be predicted from reference A1. In practice, the situation is that the input signals to a receiver are rarely all of equal unvarying amplitude and assumptions are made from the input intercept points and the input signal density.

If a series of amplitude cells are established for given frequency ranges, such as that in Table 1, then a prediction of the number of intermodulation products for any given number of input signals and amplitudes may be obtained, either from equation (1) or (2) (as applicable) or from Ref A1 (for higher orders). Where the input bandwidth of the receiver is deliberately minimised, the maximum cell size in the frequency domain should be equal to the input bandwidth.

The total input power in each cell is

$nPav$

where n is the number of signals and Pav is the average power of each signal.

A worst case situation is to assume that all signals in the cell are equal to the cell upper power limit boundary, e.g. if the cell amplitude range is from -40 to -30dBm, then an assumption that all signals in this cell are at -30dBm is a worst case.

If, however, it is assumed that signals will have a Gaussian distribution of input levels within a cell, then the total input power becomes:

$$Pt = 0.55nP$$

where Pt is the total power
n is the number of signals
P is the power level at the upper boundary of the cell

Because the total IMD power is the sum of all the IMD powers, the average input power is

$$Pav = \frac{0.55nP}{n}$$

The IMD power produced by third order curvature is:

$10 \log_{10} [\frac{1}{3}n(2n^2 + 1)]$ Antilog $\frac{1}{10}[Pav - 3(I_3 - Pav)]$dBm

where P_{IM} is the total power of the intermodulation products
I_3 is the third order input intercept point

Because the coefficients of the amplitudes of the intermodulation products are (depending on product)

a^3, a^2b, ab^2, abc, b^3

where a, b and c are approximately equal, the use of a^3 as the general coefficient is justified.

From equations (1) or (2) and (3), the total IMD power and number of products may be calculated. As 'n' increase in number, the number of products will mean that the resultant IMD tends more to a noise floor increase in the receiver, thus reducing the effective sensitivity.

The amount of this degradation is such that the noise floor is:

$$\frac{\frac{2}{3}(0.55nP)^3}{I_3} \times \frac{I_3}{(f_{max} - f_{min})} \times \Delta f$$

where $(f_{max} - f_{min})$ is the bandwidth prior to the first intermodulating stage. Δf is signal bandwidth in a linear system. The Gaussian Factor of 0.55 is somewhat arbitrary, since errors in this assumption are cubed.

The intermodulation Limited Dynamic Range is

$$\frac{2}{3}(I_3 + 174 - 10 \log_{10} \Delta f - NF)$$

where NF is the Noise Figure in dB.

The effects of Reciprocal Mixing are similar, except that signals may be taken one at a time. The performance is affected by the frequency separation between an 'off-tune' interfering signal and an 'on-tune' wanted signal unless the separation is such that the oscillator noise floor has been reached. Here again, reduction of front end bandwidth reduces the number of signals.

Generally speaking, the effects of reciprocal mixing are limited to close in effects - say within ±50kHz, unless very poor synthesisers are used.

The response at some separation f_0 from the tune frequency is: $(L - 10 \log_{10} 10\Delta f)$dB where L is phase noise spectral density in dBc/Hz and Δf is the IF bandwidth.

This assumes that the spectral density does not change within the receiver bandwidth: Ref A1 shows this to be generally applicable for narrow bandwidths.

The intermodulation free dynamic range is defined as:

$$\frac{2}{3}[I_3 - \text{noise floor}] = \frac{2}{3}[I_3 + 174 - 10 \log_{10} \Delta f - NF]dB$$

where I_3 is the input 3rd order intercept point in dBm
NF is the noise figure in dB
Δf is the IF bandwidth in Hz

It has been claimed that there is 6dB rejection of phase noise in diode commutative mixers. Thus the relationship between IMD and phase noise can be expressed as:

IMD dynamic range = phase noise dynamic range +6dB = (L - 10 $\log_{10}$ Δf) + 6dB

Thus at any offset, it is important to ensure that the two dynamic ranges are approximately equal if performance is not be be compromised.

A receiver for example with an input intercept point of +20dBm and input signals of -30dBm will produce an IMD product at -130dBm which, for an HF receiver with a noise factor of 8dB, will be just above the noise floor, in an SSB bandwidth. The noise floor of the LO will need to be such that the noise is at -133dBm if degradation is not to occur, and this will be produced by a noise floor of -137dBc/Hz in the synthesiser at the frequency separation of the signals in question. Thus the high intermodulation performance may well be compromised by poor phase noise.

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Radio Synthesiser Circuits

LOOP FILTER DESIGN

Loop Bandwidth

An important choice in the design of the Phase Locked Loop is the Loop Bandwidth. This determines parameters such as lock up time, noise and modulation capability, and generally is made as wide as possible in single loop synthesisers. There are conflicting requirements however, and single loop synthesisers are not always practicable - Refs. 1, 2.

The NJ8820 series use two phase detectors, a digital 'steering' detector and an analog high gain linear detector. This latter detector is a sample-and-hold type in which an internal 50pF capacitor is discharged at a constant current. This current is set by the gain programming resistor *RB*, and the voltage on the capacitor is sampled at the reference frequency. Thus the gain of the detector is fixed by the time available for the capacitor to be discharged. If the discharge current was constant, the phase detector would have a gain directly proportional to frequency and current, but the departure from constant current gives a correcting factor, and the gain is thus:

$$K_\Phi = 10\ \frac{[V_{SUPPLY} - 0.7 - 89\ (RB)^{-\frac{1}{2}}]}{[2\pi \times (50 \times 10^{-12} + CAP) \times RB \times FR]} \quad ...(1)$$

where *RB* is the gain programming resistor and *FR* is the phase comparison frequency. The value of *CAP* is 0 for the NJ8820/1 and is fixed externally in the NJ8822.

The analog phase comparator has a very high gain and so can only operate over a narrow phase range. This phase window is given by:

$$\Delta\Phi = 4.5/K_\Phi \text{ radian}$$

where K_Φ is the phase detector constant (volts/radian).

When the analog phase detector is outside this range, the digital detector operates to provide steering. Inside the analog detector phase range, the digital output is in its 'Tri-State' high impedance condition.

The 2nd order analog loop has a bandwidth and damping factor given by:

$$\omega_n = \sqrt{\frac{K_\Phi K_V}{NR_2C}} \quad ...(2)$$

$$D = \frac{R_3C}{2} \cdot \omega_n \quad ...(3)$$

If the loop is slewed at too high a rate by the digital output, then a longer lock up time may result because of overshoot; in extreme cases, the loop will become unstable, because the VCO frequency will sweep too quickly.

$$CR_2 = \frac{2\pi\ K_\Phi K_V}{\omega_n^2 N} \quad ...(4)$$

$$\frac{R_2}{R_3} = \frac{\pi\ K_\Phi K_V}{DN\omega_n} \quad ...(5)$$

$$R_1 \geqslant 5R_2\ \frac{2D}{\omega_n} + 1 \quad ...(6)$$

where ω_n = loop bandwidth in rads/sec
K_Φ = analog phase detector gain in volts/rad
K_V = VCO sensitivity in Hz/volt
D = loop damping factor
N = divide ratio

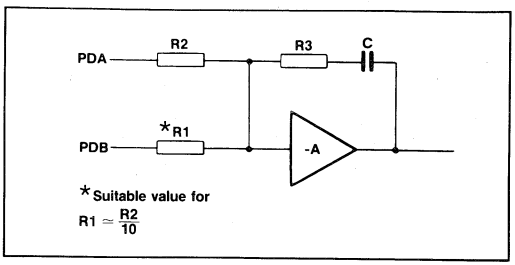

Fig.1 Augmenting integrator for loop filter

VCO Noise

Phase noise of the VCO inside the loop bandwidth will be reduced by the loop, while outside the loop bandwidth it will be unaltered. The phase noise of the reference oscillator will add to the VCO noise at frequencies inside the loop bandwidth and this effect also influences the choice of loop bandwidth. For example, a loop with a 5kHz loop bandwidth operating at 900MHz with a reasonable 5MHz crystal oscillator noise floor (-125dBc/Hz at 1kHz oscillator) would have a noise power of some -80dBc/Hz at 1kHz offset at final frequency. For a further discussion of phase noise and other compromises see Ref. 2.

Where a high phase detector gain is used with a noisy oscillator, or with a high value of K_V, it may well happen that the analog phase detector is driven outside the phase window. This will lead to the digital output becoming active, and instability is likely to result.

Modulation Techniques

Modulation of the PLL may take place inside or outside the loops bandwidth. Modulation outside the loop bandwidth requires the loop bandwidth to be less than the lowest modulating frequency, and the amount of modulation will vary over the frequency range as K_V, the VCO constant varies.

Various techniques may be used to minimise the variation in modulation sensitivity, and probably the easiest in the use of a separate modulation diode. The variation in capacitance is very small for normal NBFM variations and thus the deviation may well remain sensibly constant over a wide range, e.g. +0.75kHz for 5kHz nominal deviation over an 18MHz range at VHF.

Modulation outside the loop bandwidth leads to a signal appearing at the phase detector output corresponding to the phase error between reference frequency and the divided VCO. Should this phase error be such as to lead to the phase detector being driven outside its phase window, then problems may occur, with reference frequency sidebands appearing and possibly even unlocking of the loop.

Avoidance of this condition may be achieved by limiting the phase deviation at the detector such that detector is operating within its linear range. For devices with programmable phase detector gain, such as NJ8820 series, this may be achieved by using a low gain and high deviation ratio.

Modulation index, m, is given by:

$$m = \frac{\text{frequency deviation}}{\text{modulating frequency}} \quad \text{...(7)}$$

For a modulation index of 1 at the VCO, the phase variation is 1 radian. Thus an NBFM transmitter with a deviation of 2.5kHz and modulation frequency of 500Hz has a phase deviation of 5 radians.

In a 25kHz channelled system at 30MHz, the deviation at the detector would be 5/1200 rads or 0.24 degrees. Attempting to operate the NJ8820 at 800 volts/rad would give problems because of limiting in the analog phase detector.

Modulation inside the loop bandwidth avoids this problem, but care must be taken to ensure that the reference frequency sidebands do not become appreciable. In addition, the wideband noise of the phase detector and loop filter can cause problems when K_V, the oscillator constant in MHz/volt, is high.

Modulation of the reference oscillator is another possible technique of modulating inside the loop bandwidth. However, all modulation inside the loop bandwidth produces phase rather than frequency modulation and there are, in addition, limits on the frequency deviation and modulation frequency that can be accepted without the loop becoming unlocked. Generally, the modulation frequency must be much less than the loop bandwidth. Gardner (Ref.4) has derived the equation:

$$\Delta\omega = \frac{\omega_n^2}{\omega_m} \quad \text{...(8)}$$

where $\Delta\omega$ = frequency deviation
ω_n = loop natural frequency (bandwidth)
ω_m = modulating frequency

This equation is only valid for $\omega_m \ll \omega_n$

In general, modulation outside the loop bandwidth is used, because the required bandwidth is greater than the reference frequency. The loop bandwidth is usually 1/5 and 1/10 of the lower modulating frequency.

Note that modulation applied such that

$$\frac{\Delta\omega}{dt} \geqslant \frac{K_\Phi K_V}{R2C} \quad \text{...(9)}$$

will cause the loop to unlock.

In addition, modulation such that the analog phase detector limits is not advisable. This will occur when

$$\Delta_\Phi \geqslant 4.5N/K_\Phi \text{ rads} \quad \text{...(10)}$$

Δ_Φ is equivalent to m, the modulation index: when $m = 1$, $\Delta_\Phi = 1$ radian.

Thus, a synthesiser operating at 145MHz with a 25kHz comparison frequency and a modulation index of 30 for the lowest modulating frequencies would need K_Φ to be less than 870 volts/rad. Operation at lower frequencies are used. However, large amounts of LF phase noise can have appreciable phase deviations and thus low noise oscillators should be used.

Noise from the amplifier used in the loop filter should be minimised: the use of a low noise amplifier such as the SL562 is suggested. Filtering after the amplifier, such as in Fig. 2, is advisable but care should be taken to ensure that the added phase shift does not cause the loop to become unstable.

Loop Stability

Calculation of loop stability may be carried out in a number of ways. It has been claimed (Ref.4) that a true 2nd order PLL does not exist because of strays. In addition, an extra section (at least) of RC filtering is generally required to minimise the effects of noise in the operational amplifier. Various computer programs exist in which such analysis can be undertaken, but it is possible to evaluate loop stability in a relatively easy manner using a programmable calculator.

For a 2nd order loop such as Fig.2, it may be shown that the transfer function is

$$\frac{AoK_\Phi K_V}{N\omega} \cdot \frac{j\omega T2 + 1}{j(1-\omega^2 E) - \omega(F - \omega^2 D)} \quad \text{...(11)}$$

where $D = T3To(T1 + T2)$
$E = T3(Ao\,T1 + To + T1 + T2) + To(T1 + T2)$
$F = Ao\,T1 + To + T1 + T2 + T3$

and Ao, K_Φ, K_V, N, ω, have the previously assigned definitions.

Ao = open loop amplifier gain
To = $1/fo$, amplifier open loop 3dB bandwidth
$T1$ = $R2C1$
$T2$ = $R3C1$
$T3$ = $R4C2$

The finite modulation bandwidth of the VCO is ignored in this analysis.

Evaluating equation (11) in terms of gain and angle ($r\angle\theta$) at various frequencies allows the stability to be evaluated. An example of a frequency synthesiser design is given in the following pages

FREQUENCY SYNTHESISER DESIGN

A frequency synthesiser is required for a transmitter covering 144-148MHz. the supply voltage for the synthesiser is 10 volts, pre-emphasised frequency modulation is required with an upper limit of 3kHz, adjacent channel noise is required to be -70dB at 12.5kHz channel spacing and a 'lock-up' time of 25ms is required.

12.5kHz channel spacing systems use an IF bandwidth of 7.5kHz, which gives approximately 39dB more noise than a 1Hz bandwidth. Thus the VCO for this synthesiser must have a phase noise characteristic of -109dBc/Hz at 12.5kHz (see Ref.1) and from Refs. 2 and 3 this may be shown to be practical with a single loop synthesiser using a narrow bandwidth.

The choice of prescaler should be made from a consideration of programming - see the relevant data sheet.

The lowest modulation frequency is 300Hz and the transmitter will attenuate components below this frequency at 12dB/octave or more. Standard pre-emphasis rises at 6dB/octave from 300Hz to 2700Hz: thus the deviation at 300Hz is approximately 18dB down on that at 2.7kHz and at 50Hz will be about -45dB. With a deviation at 2.7kHz of 2.5kHz, the deviation at 50Hz will be about 15Hz.

At 144MHz, the divide ratio is 145000/12.5 = 11600. Thus the 15Hz deviation it caused by the 50Hz modulation becomes

$$15/50 \times 1/11600$$

radians at the phase detector, which is negligible. Thus the analog phase detetor will operate inside its window at low frequencies. Even at 300Hz where the modulation index is 8.33, the phase deviation at the phase detector is only 0.041 degrees.

Since a 10V supply is available, a VCO control line swing of 8 volts may be assumed. Allowing overlap, the VCO will cover 143-149MHz, giving K_V (the VCO constant) as 0.75MHz/volt. This gives a residual deviation caused by the phase detector noise of about 0.75Hz.

A loop bandwidth of 50Hz is well below the lowest modulating frequency and values may be readily calculated. K_Φ, the phase detector gain, is an independent variable; a reasonable mid-range value of 320 volts/rad gives a phase window of 0.89 degrees.

From these constants, values of $R1$, $R2$, $R3$ and C in Fig.1 may be calculated.

$$CR2 = \frac{2\pi K_\Phi K_V}{\omega_n^2 N}$$

$$\frac{R2}{R3} = \frac{\pi K_\Phi K_V}{DN\omega_n}$$

$$R1 \text{ min} = \frac{6R2}{K_\Phi}$$

Thus, at the mid-band frequency of 146MHz, where N = 11680:

$$CR2 = \frac{2\pi \times 320 \times 0.75 \times 10^6}{(2\pi \times 50)^2 \times 11680} = 1.3$$

$$\frac{R2}{R3} = \frac{\pi \times 320 \times 0.75 \times 10^6}{0.7 \times 11680 \times 2\pi \times 50} = 293$$

$$R1 \geqslant \frac{5R2}{K_\Phi}\left(\frac{2D}{\omega_n}\right) + 1$$

The use of high values of resistance leads to greater noise generation in the loop filter because of KTB noise, while low values lead to larger current swings, which can give slew rate limiting in the op-amp. If $R3$ is set to 2200Ω, thus preventing slew rate limiting,

$R2$ = 664kΩ (use 680kΩ)
$C1$ = 1.9μF (use 2.2μF)

From these standard values

$$\omega_n = \sqrt{\frac{K_\Phi K_V}{NCR2}} = 293.3 \text{rads/sec} \equiv 46.7\text{Hz}$$

$$\text{and } D = \frac{R3C}{2} \cdot \omega_n = 0.71$$

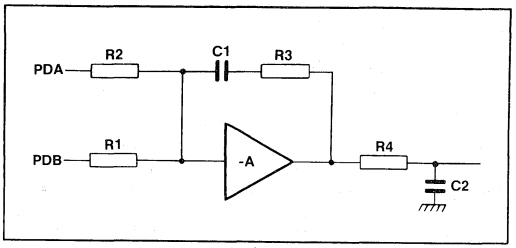

Fig.2 Augmenting integrator amplifier with filtering

$$R1 \text{ min} = \left(\frac{5 \times 680k\Omega}{320}\right)\left(\frac{2 \times 0.71}{2\pi \times 46.7} + 1\right) = 10.7\text{k}\Omega$$

(use 12kΩ or 15kΩ).

A further section of filtering may be added as in Fig.2, and the cut-off frequency may be arbitrarily set at 500Hz. Again, a reasonable compromise is required on CR values for the same reasons. The added filter section reduces noise from the op-amp and resistors, and so is a useful addition.

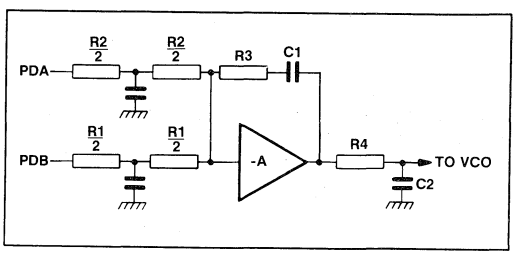

Fig.3 Loop filter with input sections

In cases where the operational amplifier 'locks up' because of overdrive, the circuit of Fig.3 may be used, often with success. The time constants $C3R2/2$ should be about $10/fn$ where fn is the loop bandwidth. It should be noted that the capacitor $C1$ *must* be of the non-polarised variety, as the voltage across it can reverse. Similarly, the external capacitor provided in the phase detector of the NJ8820 should be a low leakage type, such as polystyrene: ceramic capacitors are not generally good enough.

Bypassing the gain setting resistor of the NJ8820 series with a large capacitor may reduce noise derived from this resistor.

MULTIMODULUS DIVISION

Phase Locked Loop Frequency Synthesisers of the form shown in Fig.4 suffer from the problems inherent in producing fully programmable dividers required to operate at appreciable frequencies while not consuming excessive power. Although advances in small geometry integrated circuit technology make any figures obsolete, guaranteed operation above about 50MHz requires relatively high power.

The use of fixed prescaling, as in Fig.5, is widely used, but for a division ratio of N in the prescaler and a channel spacing of f kHz, the phase comparison frequency of Fig.4 has been reduced by the factor f/N. This lower frequency necessitates a lower bandwidth in the phase locked loop, and thus a greater susceptibility to microphonics etc., and, generally speaking, a longer lock up time.

The alternatives to fixed division are mixing, as in Fig.6 or 'multimodulus division' ('pulse swallowing') as in Fig.7. The use of mixers requires great care in the choice of frequencies if spurious products are not to be a problem and although widely used, is certainly more complicated than multimodulus division in terms of its physical realisation, requirements for 'adjust-on-test' parts, and its susceptibility to layout problems.

The multimodulus divider system is shown in Fig.7. It is built up from a number of blocks:

1. A two-modulus divider which will divide by one of two numbers N or $N + 1$ (e.g., 10/11, 64/65 etc.).

2. An A counter which is programmable and the output of which controls the modulus of the divider.

3. An M counter which is programmable, is clocked in parallel with the A counter, and the output of which resets both itself and the A counter.

The counters may count 'down' to zero from the programmed input, or count 'up' from zero.

The principle of operation is as follows:

The A counter is programmed to a smaller number than the M counter and assuming the counters to be empty, the system starts with the divider ($N/N + 1$) dividing by $N + 1$. This continues until the A counter reaches its programmed value, whereupon the divider divides by N until the M counter is full. As the M counter has received A pulses, this counter overflows after (M - A) pulses, corresponding to $N(M - A)$ input pulses to the divider. Thus the total division ratio P is given by:

$$P = (N + 1)A + N(M - A)$$
$$= NM + A$$

Obviously, A must be equal to or less than M for the system to work, while for every possible channel to be available, the minimum total divide ratio is $N(N - 1)$ while the maximum total divide ratio is $M(N + 1)$. A_{max} should be equal to or greater than N.

Although deceptively simple in theory, there are a few points which require consideration in the design of such a divider system. Of these probably the most important is Loop Delay.

Consider the counter chain at the instant that the $(N + 1)$th pulse appears at the two modulus divider input. After some time $tp1$ the output produces a pulse, which clocks the A and M counters. Assume that the A counter is filled by the pulse, and so after a time $tp2$ (determined by the propagation delay of the A counter) an output is produced to set the dual modulus divider ratio to N. After a set-up time ts, the dual modulus divider will divide by N. But if $tp1 + tp2 + ts$ is greater than N cycles of input frequency, the divider will not be set to divide by N until after N pulses have appeared, and the system will fail. Thus

$$\frac{N}{fin} > \text{total loop delay}$$

Design in this region is critical: worst case tolerances *MUST* be used if the reproducibility and reliability of the design under temperature and voltage extremes is not to be compromised.

The value of N must also be large enough that the output frequency from the divider does not exceed the maximum input frequency of the following circuitry. In single chip MOS controllers, this may well be as high as 50MHz under some conditions, but under others, such as high temperature and low voltage, much lower. Generally, however, the limitation on such circuits is the loop delay rather than input frequency.

The loop delay is affected by the edge of the waveform on which the divider and the A and M counters trigger. If the edges are opposite then the loop delay may be increased by large amount, and if in these circumstances, the use of an inverter at the output of the divider is justified.

The minimum value of N is therefore settled by these constraints, but the actual choice of N may be determined by the ease of programming. This may be seen by considering a synthesiser with a 25kHz phase comparison frequency and 25kHz channelling, using a 40/41 divider.

At 156MHz:

$$P = \frac{156}{0.025} = 6240$$

therefore $NM + A = 6240$
therefore $40M + 0 = 6240$ ($A = 0$ for the lowest channel)
therefore $M = 156$

In general, where

$$fN = 1 \text{ or } 10 \text{ or } 100$$

$$M = f, \frac{f,}{10} \frac{f,}{100} \text{ etc.}$$

and similarly for binary divide ratios.

The choice of prescaler is therefore fixed by

1. Total allowable loop delay.

$$\frac{N}{fin} > \text{controller delays}$$

2. Output frequency within the controller input frequency band.

3. Programming ease.

Reference Frequency Division Ratio (R)

The value of R is set by the input frequency and the phase comparison frequency. Higher input frequencies require greater power and offer lower stability, while lower frequencies (below 4MHz) generally require larger physical crystal case sizes. Normally, a frequency between 4 and 10.7MHz is used, especially as in double conversion equipments commonality of oscillators may be possible.
e.g. for a 2.5kHz comparison frequency and 10.245MHz 2nd local oscillator frequency,

$$R = \frac{10.245 \times 10^6}{2.5 \times 10^3} = 4098$$

Note that R is *always* an even number.

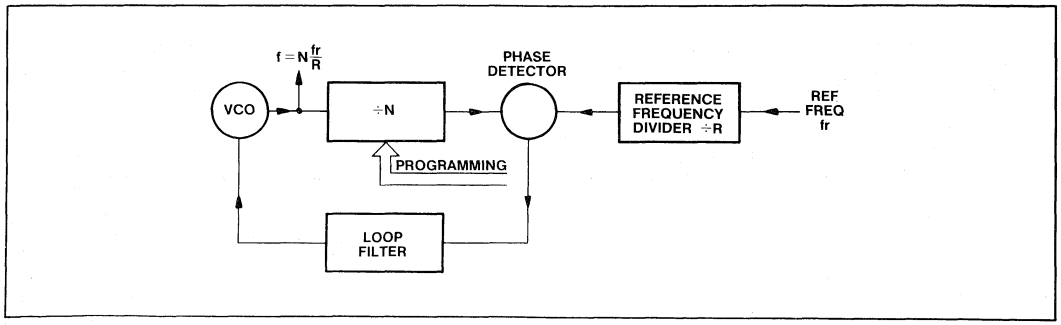

Fig.4 Direct division

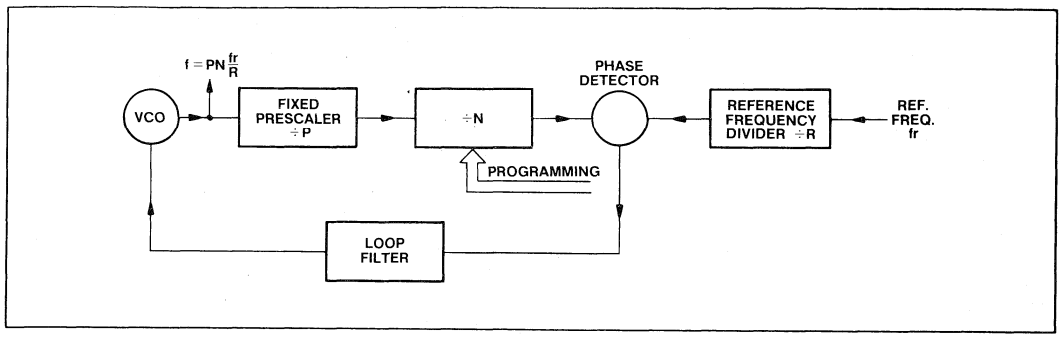

Fig.5 Fixed prescaling

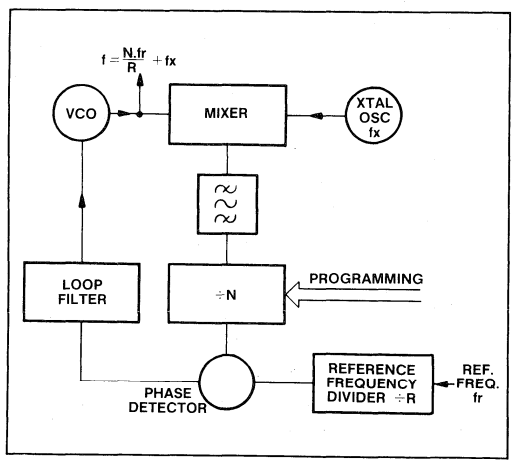

Fig.6 Mixing in the loop

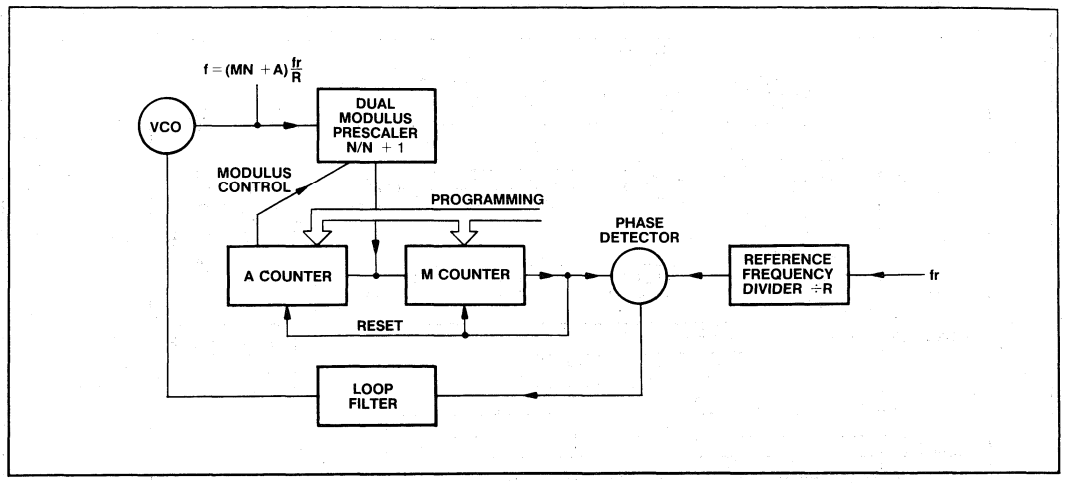

Fig.7 Dual modulus prescaling

PROGRAMMING THE NJ8820/21/23

The NJ8820 and NJ8821/23 are versatile high performance CMOS frequency synthesiser controllers. The differences between devices lies in hardware programming methods. *NOTE: Technical Data for these ICs is included in the Personal Communications IC Handbook (Publication No. PS2123). Data for the NJ8821 is also given on pages 2-42 to 2-46 of this Handbook.*

The basic system of a single loop frequency synthesiser is shown in Fig.8, where a 2-modulus prescaler is used to divide the VCO frequency down to a suitable range for use in the CMOS device. The NJ8820/1/3 is programmed by 8 of 4 bit words on the data inputs: the addresses for these words may be obtained internally or externally and appear on the Data Select inputs/outputs. To program any frequency, it is necessary to program the *A* counter, the *M* counter and the reference or *R* counter: these counters are respectively, 7, 10, and 11 bits long.

ADDRESSING

Addressing is by one of three modes: These are:

A. Self Programming Internal Mode

Here the reference oscillator (either an internal crystal oscillator or from an external source) signal is divided in the reference counter by 64 and a DATA READ cycle commences every 1024/fosc seconds.

In this DATA READ cycle, the MEMORY ENABLE pin is pulled low, and the DATA SELECT outputs DS0, 1 and 2 count in binary from 0 to 7. This provides addresses for the DATA on D0, 1, 2 and 3, the data being transferred to internal latches on the trailing edge of the DATA SELECT pulses -see Fig.9. Note that the Program Clock is internally derived and is at a frequency of fosc/64. The PE (Program enable) pin is grounded, and the cycle continuously repeats. This mode is not recommended, as noise may be picked up by the phase locked loop.

B. Single Shot Internal Mode

In this mode, the PE pin is provided with a pulse input. This pulse initiates a data read cycle as outlined above, and at the end of the cycle, the ME (Memory Enable - NJ8820 and NJ8820HG only) pin goes high and thus system power consumption is minimised. 'Power-on' initiation is used, in which the application of power to the device is sensed and a programming cycle initiated. In order to avoid corruption of the data, a delay of 53248 cycles of reference oscillator frequency is provided before the programming cycle occurs. This delay is approximately 5ms for a 10MHz reference frequency.

C. External Mode

The address is presented to DS0, 1 and 2, and a pulse is applied to the PE pin to transfer data to the internal latches. The data is transferred from the latches to the counters simultaneously with the transfer of data into Latch 1: thus this word should be the last one entered.

WORD VALUES

For any particular set of conditions, viz operating frequency, prescaler ratio, comparison frequency and input frequency from the reference oscillator, a unique set of programming words exist.

Reference Divider

This divider produces the comparison frequency required by the synthesiser. It is programmable from 6 to 4094 in steps of 2. The division ratio is twice the programmed number. Therefore, if for example a 10MHz crystal is used, and a 12.5kHz reference required, this counter would be programmed to give a ratio of 100000/12.5 = 800. The actual programming would then be 400, which would be entered in binary according to the data map, **Table 4**.

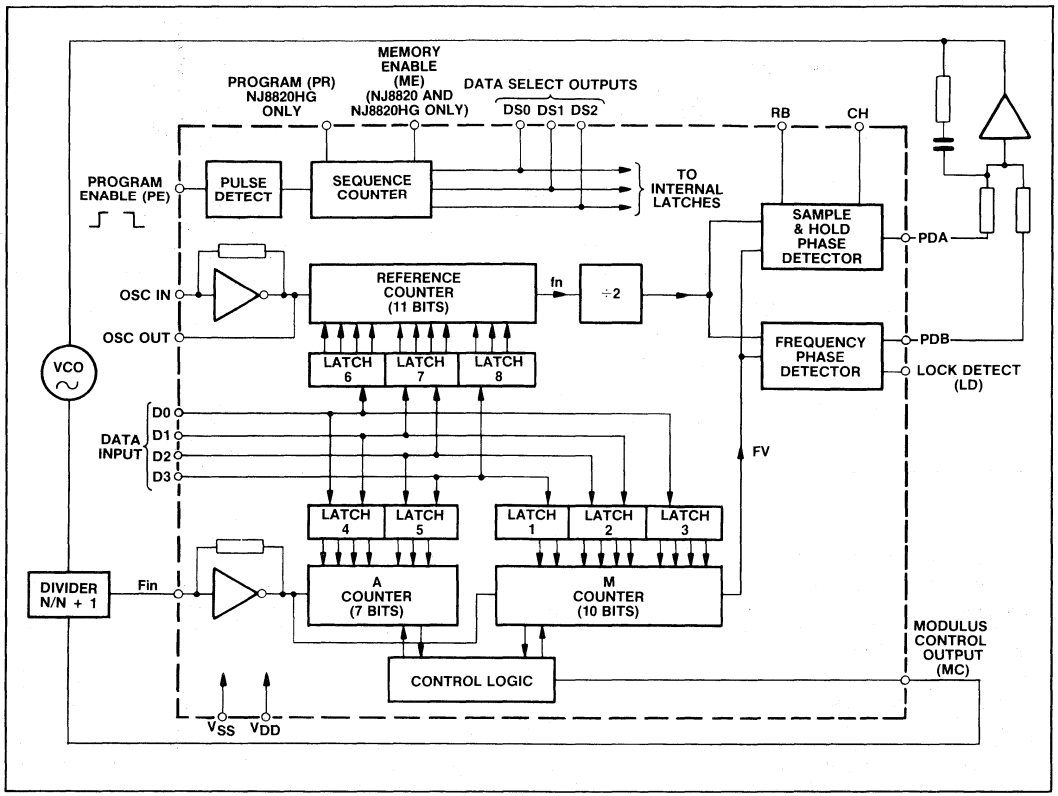

Fig.8 The phase lock loop

A and N Dividers

The *A* counter is a 7-bit counter and the *M* counter is a 10-bit counter. The programming calculations are as follows:

1. The *A* counter should contain *x* bits such that $2^x = M$.

2. If more bits are included in the *A* counter, these should be programmed to zero.

e.g. $M = 64 = 6$ bits
$A = 10$ bits
then the 4 MSB are programmed to zero.

3. The *M* and *A* counters are treated as being combined so that the MSB of the *M* counter is the MSB of the total and LSB of the *A* counter is the LSB of the total.

e.g. A synthesiser operating from 430-440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.
P = f/fref and fref = channel spacing = 25kHz
$Pmin = 430/0.025 = 17200$
$Pmax = 440/0.025 = 17600$

Minimum possible divide ratio is $N^2 - N = 4032$
where N is two modulus divider ratio

$$\text{maximum allowable loop delay} = \frac{64}{440 \times 106} = 145\text{ns}$$

Total divide ratio, P, is given by
$P = NM + A$
$N = 64$, as a 64/65 divider is used
$Pmin$ from above is 17200

Therefore $17200 = 64M + A$
And $M \geqslant A$
Let $A = 0$ Then $Mmin = \frac{17200}{64} = 268.75$

$= 268$
and $Mmax = \frac{17600}{64} = 275.0$

Thus the *M* counter must be programmable from 268 to 275 as required: the *M* counter must have at least 9 bits.
For a frequency of 433.975MHz

$P = 433.97/0.025 = 17359$

$$\text{therefore} \quad M = \frac{17359}{64} = 271.2343$$

The *A* counter is programmed for the remainder i.e.

$$0.2343 \times 64 = 15$$

From this, the *A* counter is programmed to 15 and the *M* counter to 271. The output frequency can bow be checked.

$P = NM + A$
$= 271 \times 64 + 15 = 17359$
and this is the required divider ratio.

Repeated calculations for memory programming may be evaluated using a programmable calculator. The program listed in Table 1 is suitable for most Hewlett Packard calculators.

Line	Function	Display
001	hLBLA	25 13 11
002	ENTER	31
003	RCL0	24 0
004	-	71
005	STO2	23 2
006	RCL1	24 1
007	-	71
008	STO3	23 3
009	hFRAC	25 33
010	ENTER	31
011	RCL1	24 1
012	X	61
013	STO4	23 4
014	RCL3	24 3
015	ENTER	31
016	RCL3	24 3
017	hFRAC	25 33
018	-	41
019	STO3	23 3
020	hPSE	25 74
021	hPSE	25 74
022	RCL4	25 4
023	hRTN	25 12

Table 1. Calculator program for values of M and A

To use the program, enter the comparison frequency in STO0, and the dual-modulus prescaler ratio in STO1 (this is the value of N in an $N/N + 1$ divider).

Enter the frequency to be synthesised in Hz and press the R/S button. The calculator will flash twice and display the decimal value of M: pressing R/S again will display the value for the A counter. The M counter value is in STO3: the A counter value is in STO4.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Table 2. Data map

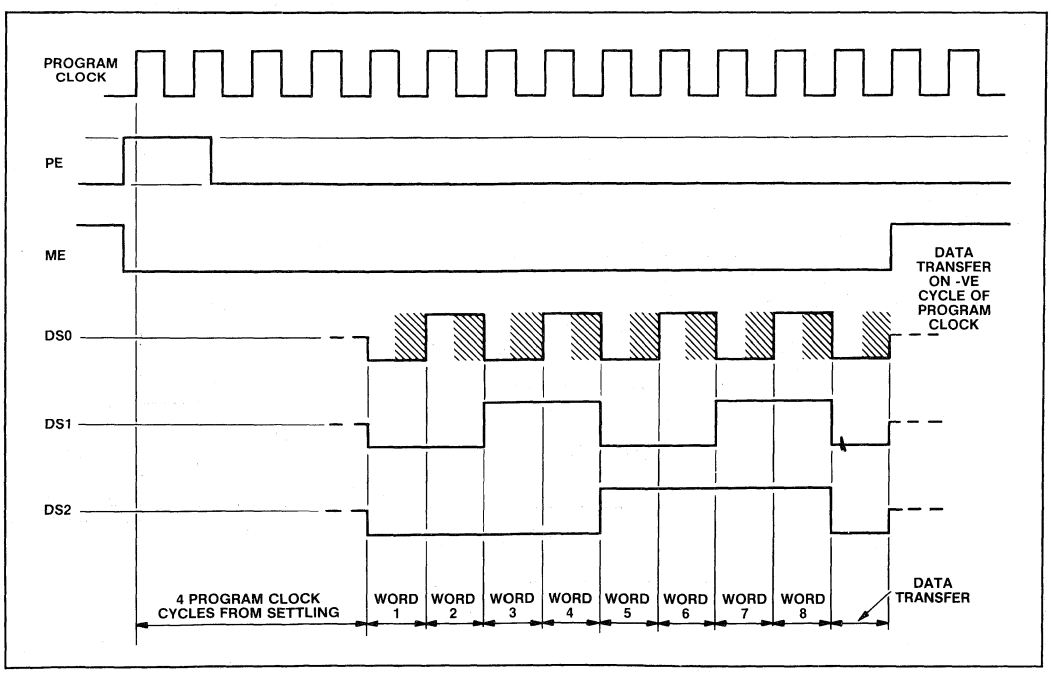

Fig.9 Data selection

NJ8820/1 SYNTHESISER DESIGN SUMMARY

1. Choose a suitable prescaler

- Check that input frequency range is suitable.
- $\frac{fin}{N} < 10.7\text{MHz}$
- $\frac{N}{fin} > 50\text{ns} + tr + tp$

  (tr is 'set-up' or 'release' time - whichever is longer; tp is propagation delay).
- Minimum division ratio is $N^2 - N$.

2. Choose the crystal frequency and value of R

- The phase comparison frequency should be as high as possible - usually the channel spacing.
- Higher crystal frequencies use more current and are less stable, but frequencies below 4MHz need larger case styles.
- R *must* be an even number.

3. Set values for A and M

- A is between 0 and 127.
- A is always equal to or less than M.
- Total division ratio is $NM + A$.
- M is between 3 and 1023.

4. Set loop values

- Choose the loop bandwidth ω_n rads/sec - normally less than $\frac{fx \,.\, 2\pi}{10R}$ (fx = crystal frequency)
- Choose the Damping Factor D - normally 0.7.
- Choose phase comparator gain such that at the lowest modulation frequency the phase deviation

$$\frac{\text{Modulation index}}{(MN + A)} < \frac{4.5}{K_\Phi}\text{ rads}$$

5. Calculate the values:

- $$CR2 = \frac{2\pi K_\Phi K_V}{\omega_n^2 \,.\, (NM + A)}$$

  (K_Φ in volts/rad)
  (K_V in rads/volt-sec)
  (ω_n in rads/sec)
- $$\frac{R2}{R3} = \frac{\pi K_\Phi K_V}{D(NM + A)\ \omega_n}$$
- $$R1 > \frac{6R2}{K_\Phi}$$
- $$\frac{1}{R4C2} \geqslant \frac{10\ \omega_n}{2\pi}$$

6. Check the time to reach a new frequency

- $$t = \frac{\Delta\omega}{2.5K_V}\left(\frac{1}{R1R3} + CR1\right)$$

  ($\Delta\omega$ is the frequency step in rads/sec).

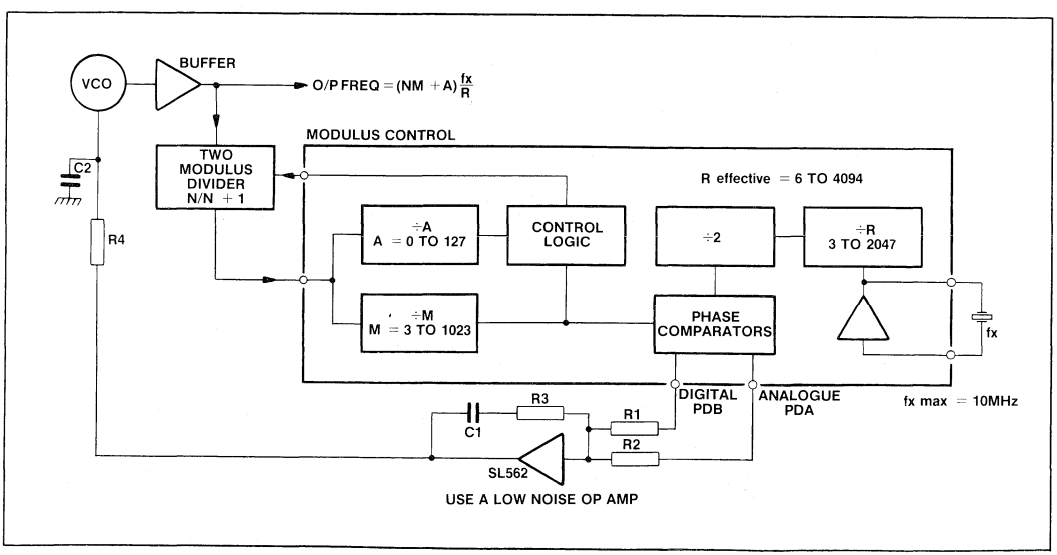

Fig.10 PLL using NJ8820/1/3

7. Check the loop stability using Bode or Nyquist plots.

8. Derive the program numbers for the A and M counters - or use the calculator program listed in Table 1.

9. An example

A synthesiser is to operate from 430 to 440MHz in 25kHz steps (the channel spacing is 25kHz):

- **Choose the divider** The SP8718 is one choice. Since it divides by 64/65 then $N = 64$.
- **Choose the reference frequency** 25kHz is the channel spacing and is the best choice in this case.
- **Choose the crystal frequency** 2.5MHz is one possibility. The value of R can now be calculated:

  Crystal frequency = Reference frequency x R x 2
  So $R = 50$
- **Calculate the division ratio** (the ratio between the VCO output frequency and reference frequency)
  This is 17200 to 17600 in steps of 1.
- **Calculate values for A and M** The division ratio $NM + A$ is 17200 to 17600.

  So for the **minimum** frequency: $64M + A = 17200$
  If $A = 0$, $M = 268.75$
  This is not possible (it must be an integer) so this must be **decreased** to make $Mmin = 268$.
- **Draw up a table** for the required values of A and M

  Division ratio $(P) = NM + A$
  $= 64M + A$

  or use the calculator program listed in Table 1.

M	A	Division ratio	Output frequency (MHz)
268	48	17200	430.000
..	49	17201	430.025
..	50	17202	430.050
..	..	..	..
..	..	..	..
..	..	..	..
268	63	17215	430.375
269	0	17216	430.400
..	..	..	..
..	..	..	..
..	..	..	..
..	..	..	..
274	63	17599	439.975
275	0	17600	440.000

Table 3. Decimal values of A and M

These figures are acceptable:

$$N \geqslant A$$
$$P > M^2 - M$$

The values of M, A and R must be fed into the NJ8820/1 for each value of frequency required. (In this example the value of R is constant). The values must first be converted into BINARY format as shown in Table 4.

M (decimal	M (10 bit binary)									
	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
268	0	1	0	0	0	0	1	1	0	0
268										
268										
..										
..										
..										
..										
..										
..										
..										
274	0	1	0	0	0	1	0	0	1	0
275	0	1	0	0	0	1	0	0	1	1

Table 4a. Binary values for M

A (decimal)	A (7 bit binary)						
	A6	A5	A4	A3	A2	A1	A0
48	0	1	1	0	0	0	0
49	0	1	1	0	0	0	1
50	0	1	1	0	0	1	0
..							
..							
..							
..							
..							
..							
..							
63	0	1	1	1	1	1	1
0	1	0	0	0	0	0	0

Table 4b. Binary values for A

R (decimal)	R (11 bit binary)										
	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
50	0	0	0	0	0	1	1	0	0	1	0
50											
50											
..											
..											
..											
..											
..											
..											
..											
50											
50											

Table 4c. Binary values for R

In each case the LSB is identified by the heading $M0$, $A0$ or $R0$.

The NJ8820 and NJ8821/23 require 32 bits of data to be transferred for each value of frequency. These 32 bits are composed of the 28 bits above (10 + 7 + 11) plus 4 redundant bits. The method of transferring this data is different for the two device types.

NJ8820 - data obtained from a PROM

NJ8821/23 - data obtained from a Microprocessor.

USING THE NJ8820

The NJ8820 operates with an external 4-bit wide PROM. Information is transferred automatically from the PROM to the NJ8820 when the PE pin is activated. a 1024-bit PROM (256 × 4) will store 32 channels because each channel requires the transfer of 8 words (32 bits) of data. A 256 × 4 PROM has 8 address lines (A0 to A7), of which the NJ8820 can address 3 (A0 to A2, connected to DS0 to DS2). The remaining 5 address lines allow the unique identification of the channel required (32 channels in this case), as shown in Table 5; so for each channel number there 8 words, each of four bits. The composition of these words is as shown in Table 6. X indicates that this is not read; normally, the 8-bit value is 0.

The value of bits D3, M1 etc. can be either 0 or 1 and can be found from Tables 2 through 5. For example, when M = 268 then (from Table 4a) M1 = 0, M0 = 0 and (from Table 5) word 1 = 0000.

USING THE NJ8821/23 IN A PARALLEL MODE

The NJ8821/23 operates with an asynchronous stream of data supplied from a microprocessor. When used in a 4-bit parallel mode it requires the transfer of 8 words (32 bits) of data. Word numbers 1 to 3 control the '*M*' counter, 4 and 5 the '*A*' counter, 6 to 8 the '*R*' counter. It is not necessary to transfer all the words every time; WORD 1 indicates to the NJ8821/23 that the data should be transferred from all latches to counters and so WORD 1 must always be sent last. There are 8 data connections between the microprocessor and NJ8821/23:

- *DS*0, *DS*1 and *DS*2 to select the correct word
- *D*0, *D*1, *D*2 and *D*3 are the input data for *A*, *M* and *R* counters
- *PE* is the strobe

To enter channel information follow the sequence listed below:

1. Ensure the *PE* (strobe) is 0.
2. Select any word (except word 1)...(*DS*0 to *DS*2) and the relevant input data (*D*0 to *D*3).
3. Wait for 1 microsecond or more.
4. Pulse the strobe (to 1) for 2 microseconds or more and return to 0.
5. Wait for 1 microsecond or more.
6. Repeat (2) to (5) as required.
7. Repeat (2) to (5) for word 1.

The composition of the data words is identical to that for the NJ8820.

USING THE NJ8821/23 IN A SERIAL MODE

When used in a serial mode (using a single external shift register) the NJ8821/23 requires the transfer of 8 words, each of 7 bits (56 bits) of data to program the *A*, *M* and *R* counters but only 5 words (35 bits) subsequently to reprogram the *A* and *M* counters. There are thus only 3 data inputs from the microprocessor: DATA, CLOCK and STROBE, as shown in Fig.11.

	ADDRESS LINES								
	A7	A6	A5	A4	A3	A2	A1	A0	
CHANNEL NUMBER 0					0	0	0	0	word 1
					0	0	0	1	word 2
					0	0	1	0	word 3
					0				..
					0				..
					0	1	1	1	word 8
CHANNEL NUMBER 1	0	0	0	0	1	0	0	0	word 1
					1	0	0	1	word 2
					1	0	1	0	word 3
					1				..
					1				..
					1	1	1	1	word 8

Table 5. Channel identification

ADDRESS LINES			DATA LINES				WORD
A2	A1	A0	D3	D2	D1	D0	
0	0	0	M1	M0	X	X	1
0	0	1	M5	M4	M3	M2	2
0	1	0	M9	M8	M7	M6	3
0	1	1	A3	A2	A1	A0	4
1	0	0	X	A6	A5	A4	5
1	0	1	R3	R2	R1	R0	6
1	1	0	R7	R6	R5	R4	7
1	1	1	X	R10	R9	R8	8

Table 6. Channel number composition

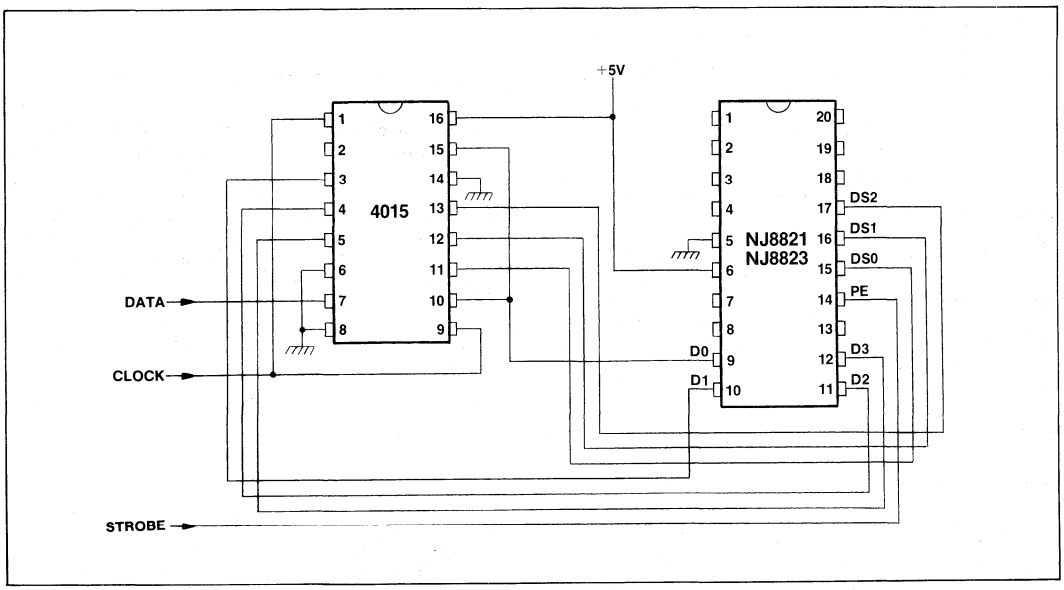

Fig.11 NJ8821/23 serial mode connections

The composition and entry sequence of the data words is identical to that of the NJ8820 except that the data is transmitted serially.

Once again, there is no need to transfer all the words every time provided that WORD 1 is always sent last.

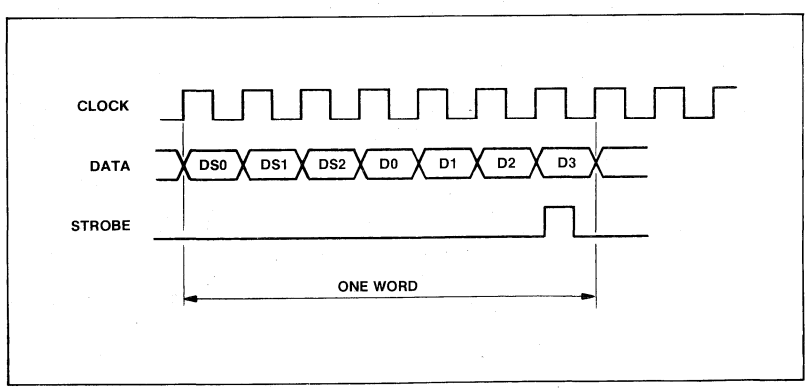

Fig.12 Serial data timing

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1. "Design Compromise in Single Loop Frequency Synthesisers" P.E. Chadwick, RF Design Expo, Anaheim, Ca. Jan 1985
2. Frequency Synthesisers, Theory and Design, V. Manassewitsch, Wiley, 1980, ISBN 0-471-07917-0
3. Digital PLL Frequency Synthesisers, U.L. Rohde, Prentice Hall, 1983, ISBN 0-13-214239-2
4. Phaselock Techniques, F.M. Gardner, Wiley 1979, ISBN 0-471-04294-3

A Serially Programmable VHF Frequency Synthesiser

This demonstration circuit uses three Plessey Devices - the NJ8822 single chip synthesiser, the SP8793 dual-modulus prescaler and the SL562 low noise op-amp in the configuration shown in Fig.1. The NJ8822 is programmed via a serial microprocessor interface.

The VCO is a J FET oscillator using a transmission line as the resonator. This VCO is modulated by applying the audio signal to the cathode of a reversed biased PIN diode as shown in the circuit diagram. The loop filter uses the SL562 which with the values shown has a loop bandwidth of 60Hz and a damping factor of 0.6. This filter is followed by a low pass pole at 3.7kHz to attenuate the 12.5kHz reference sidebands. The lock up time for a 1MHz change in frequency is 80ms (determined empirically). The output frequency range is 144-146MHz and the level is +3dBm into 50Ω.

The output spectra at 12.5kHz reference frequency is shown in Fig.2, and Fig.3 is a graph of modulating frequency against percentage distortion at several values of deviation. The circuit performs normally at a supply voltage of 5V ± 0.5V and within a temperature range of -30°C to +70°C. the only observable effect of varying the temperature was a frequency drift of 3kHz between the temperature extremes due to the uncompensated reference oscillator.

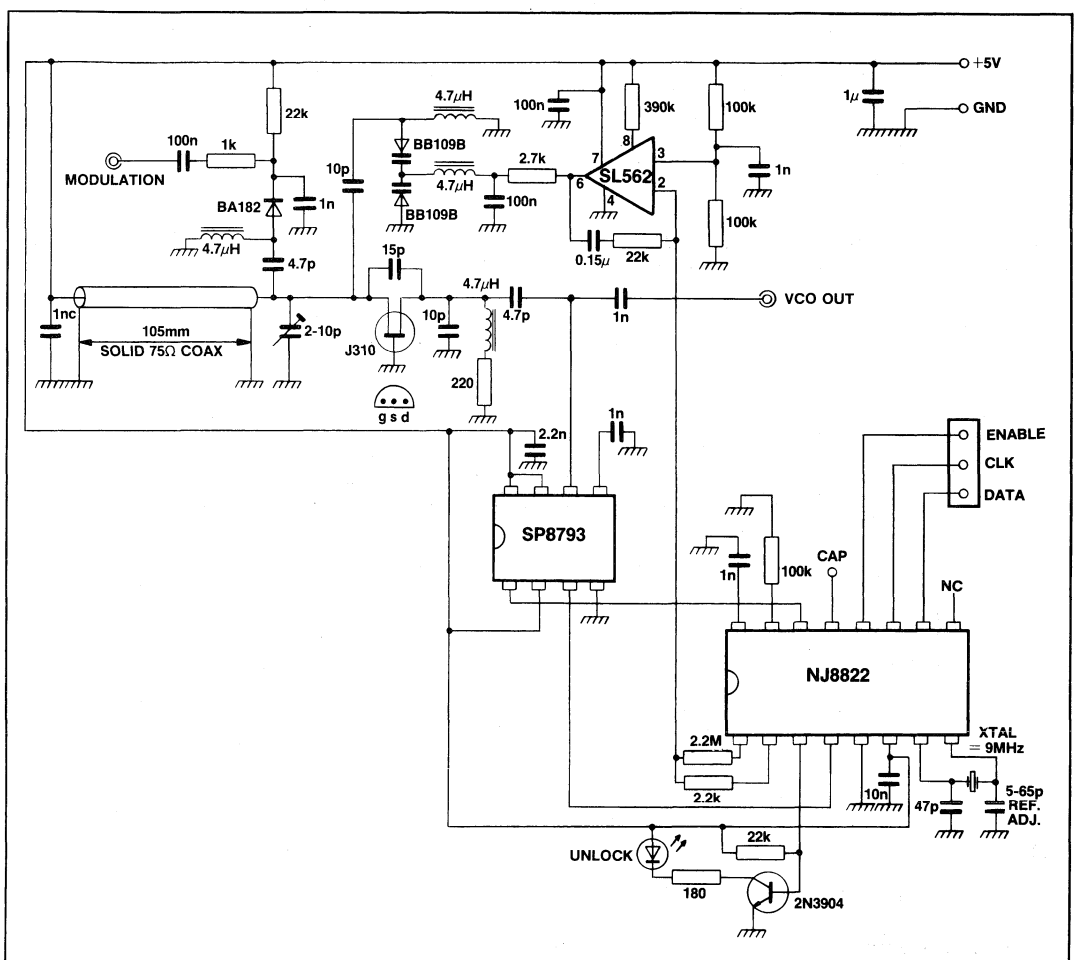
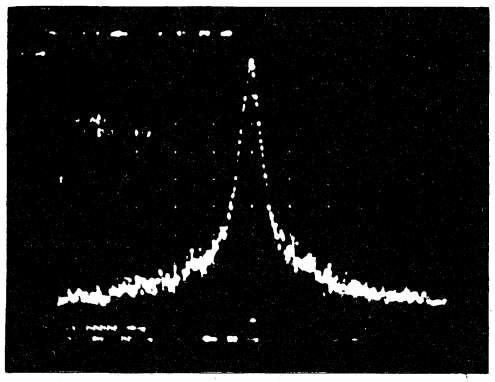
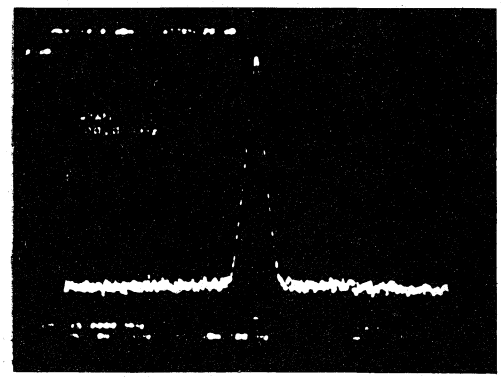


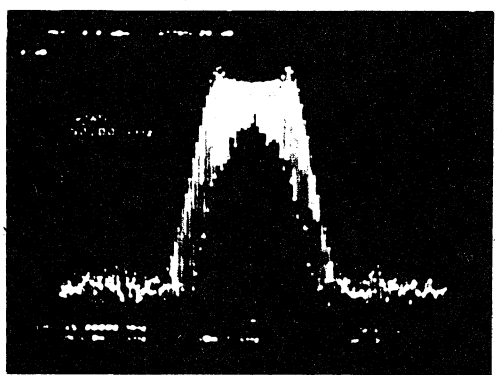
Fig.1 NJ8822 serially programmable VHF synthesiser



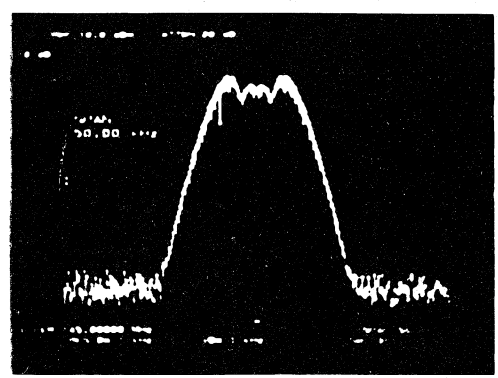
(a) Unmodulated 10kHz span



(b) Unmodulated 100kHz span



(c) Modulated 400Hz 5kHz deviation 50kHz span



(d) Modulated 1kHz 5kHz deviation 50kHz span

Fig.2 NJ8822 frequency synthesiser spectral performance

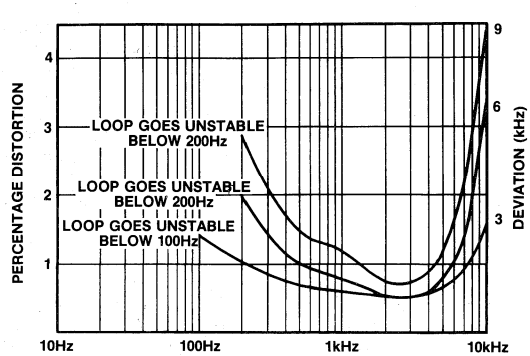


Fig.3 Graph of distortion against modulating frequency at various deviations for the NJ8822 VHF frequency synthesiser

Design Compromises in Single Loop Frequency Synthesisers

The single loop frequency synthesiser is justly popular as an approach to frequency synthesis. It has the merit of simplicity, and because of this, low cost, especially as a large amount of the circuitry is easily produced in monolithic integrated circuit form.

Certain performance parameters of the synthesiser are defined by the equipment performance. For example, a marine VHF radio frequency synthesiser has requirements for phase noise and discrete spurious outputs defined by the adjacent channel specification, and the phase noise performance may well need to be several dB better than would at first be expected. If the adjacent channel rejection is 70dB for example, then a single sideband phase noise level in the receiver bandwidth must be more than 70dB, see Fig.1. In fact, the translated noise level should be reduced by an amount dependent upon the performance of other areas of the equipment and these specification levels are typically determined by the system architect. Frequently, however, during design of a project, some modifications in architecture become apparent, but an understanding of practical limitations is vital at an early stage if delay and consequent expense is to be avoided. For further details on the effects of phase noise on receiver performance, see Ref.1.

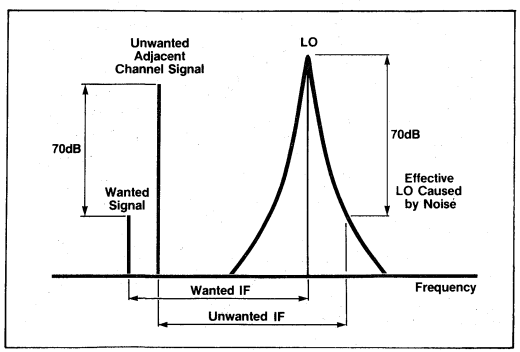


Fig.1 Phase noise and adjacent channel rejection

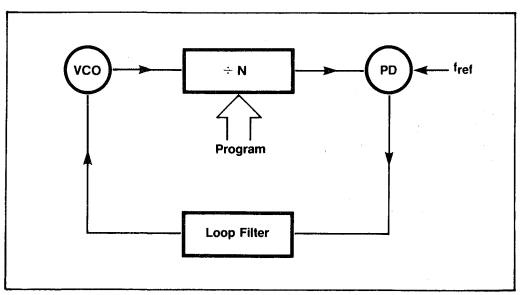


Fig.2 Simple PLL

DIVIDERS

Single loop synthesisers using direct division as in Fig.2 suffer from certain limitations. Fully programmable dividers are not generally available for frequencies above about 50MHz without high power consumptions, and even CMOS dividers currently available are limited in applications at low (5V) supply voltages and extreme temperatures. Newer devices are appearing, however, and experimental 250MHz operation has been observed.

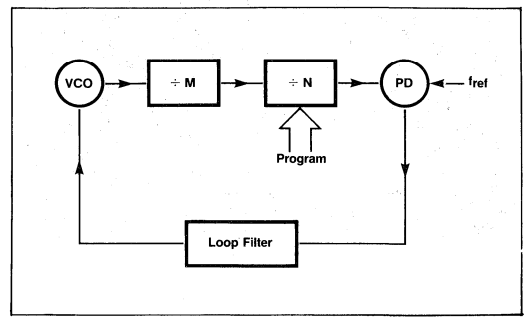


Fig.3 Use of a fixed prescaler

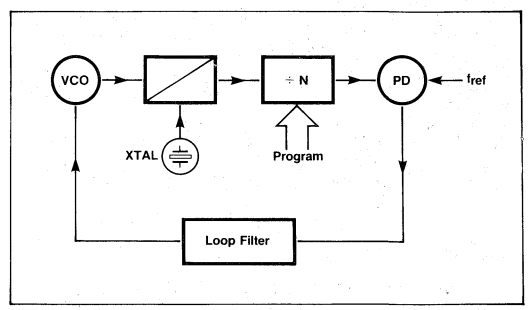


Fig.4 Mixing in the loop

Early synthesisers used fixed prescalers to divide the VCO down to a suitable frequency for the programmable counter as in Fig.3, or used mixing techniques as in Fig.4. Indeed, a large number of CB radios use the mixing technique, but this system can suffer from spurious products unless carefully designed in choice of frequencies, input levels and particular mixers used, see Refs. 2,3,4 and 5. In addition, the large variation in subsequent division ratio may give problems with loop dynamic performance.

A major area of conflict lies in the choice of reference frequency. In synthesisers such as Fig.3, the output frequency step size is *M* times, the reference frequency, where *M* is the prescale ratio. In a system where every channel is used, the problem is then that the reference frequency has to be decreased by a factor of *M*, and as a result, the bandwidth of the feedback loop must decrease. The bandwidth and damping factor of the loop filter are vitally important parameters in determining such loop characteristics as lock up time as well as the phase noise characteristics. (The effects of loop bandwidth on phase noise will be discussed later.) In general, the widest possible loop bandwidth is required to minimise lock up time and to confer the greatest immunity to shock and vibration. However, the loop bandwidth cannot be greater than the reference frequency and so the use of a fixed prescaler is obviously somewhat limited. The alternative is the widely used 'Two Modulus' or 'Pulse Swallowing' prescaler system, illustrated in Fig.5. In this method, the prescaler is able to divide by two integers *N* and *N* + 1. The two counters *A* and

M are programmable and are clocked in parallel, the divider being set initially to the $N + 1$ ratio. When the A counter is full, the divider is set to divide by N until the M counter is full, giving a total division ratio of $MN + A$. This system is limited to a minimum division ratio of $N^2 - N$ if every value of N is to be achieved (no 'skipped' channels) and the M counter must always be programmed to a bigger number than the A counter. Within these limitations, however, a fully programmable divider is achieved and so f_{ref} can now equal the channel spacing.

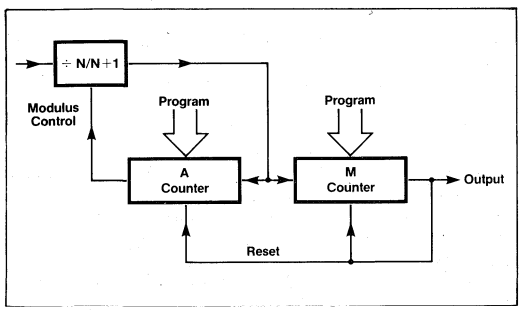


Fig.5 Two modulus divider

Another and more subtle limitation is in the delay times of the various components within the loop. When the circuit (Fig.5) has counted down so that the M counter has been filled, the whole system is reset, and quite obviously, must achieve this in a time equal to $N + 1$ cycles of the input frequency e.g. in a ÷64/65 prescaler, at 1GHz, the reset of the M and A counters must be achieved in 65 cycles or in this case, 65ns. This means that the propagation delays plus set up/release times plus reset delays must not exceed 65ns and it is this area where trouble can often be expected, especially at temperature extremes. Although a 1GHz synthesiser with a 64/65 divider only sees an input frequency of 15MHz for 1GHz input, the set up/release time and delays may well easily reach 85-90ns and the system will thus fail.

If the propagation through the divider $= t_d$
the set up time $= t_s$
the release time $= t_r$
the propagation delay through the A and M counters $= t_c$

then

$$f_{max} = \frac{N}{(t_d + t_s + t_c)} \text{ or } \frac{N}{(t_d + t_r + t_c)}$$

whichever is least.

One of the areas in which an increase in loop delay time can inadvertently occur is if the A and M counters trigger from a different edge to the dual modulus prescaler. This can cause a major diminution in available loop delay, as can an attempt to physically separate the divider and control circuits. Other deleterious affects have been noted, such as radiation of the divider output to the VCO, producing high frequency sidebands, so practical synthesisers are best produced with little physical spacing between divider and control circuit.

The control circuit is a practical device in a number of technologies, although modern devices exclusively use CMOS to minimise power consumption. Prescalers are still mainly exemplified by bipolar technology, advances in which have seen major reductions in power consumptions in recent years - for example from 65mA at 5V for a divide by 10/11 operating at 250MHz in 1976 to 4mA at 5V for a divide by 40/41 operating at 225MHz today. Some equipments still build up the A and M counters from discrete ICs and then add phase detectors, reset circuitry and so on, but such equipments are by now obsolete in design and extremely expensive to manufacture. Nevertheless, the lessons of tolerancing delays necessary in such designs should not be forgotten just because the majority of circuitry is now hidden inside a block of silicon.

The choice of prescaler ratio is governed by a number of factors. Discussed so far have been minimum ratio and loop delay. However, the output frequency of the divider must be low enough for the A and M counters to function. Summarising

1. $f_{in} \leqslant N f_{max\ control}$
   where N is the divider ratio
   $f_{max\ control}$ is control circuit maximum operating frequency.
2. $f_{min} \leqslant \dfrac{N}{\text{total loop delay}}$
3. $P_{min} = N^2 - N$
   where P_{min} is the minimum divide ratio.
   N is the dual modulus divider ratio.

Various values for N exist in proprietary devices. These range from 3/4 to 128/129: binary values (32/33, 64/65, 128/129) are popular for ease of programming from ROMs and microprocessors, while decimal and BCD are used for thumbwheel switch programming.

Programming is a straightforward exercise for binary division and the following method is recommended.

1. The A counter should contain x bits such that
   $$2^x = N$$
2. If more bits are included in the A counter, these should be programmed to zero.

e.g.
$N = 64 = 6$ bits
$A = 10$ bits
then the 4 MSB are programmed to zero.

3. The M and A counters are treated as being combined so that the MSB of the M counter is the MSB of the total and LSB of the A counter is the LSB of the total.

e.g.
A synthesiser operating from 430-440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.
$P = f/f_{ref}$ and f_{ref} = channel spacing = 25kHz
$P_{min} = 430/0.025 = 17200$
$P_{max} = 440/0.025 = 17600$

Minimum possible divide ratio is $N^2 - N = 4032$
where N is two modulus divider ratio

Maximum allowable loop delay $= \dfrac{64}{440 \times 106} = 145\text{ns}$

Total divide ratio, P, is given by
$P = NM + A$
$N = 64$, as a 64/65 divider is used
P_{min} from above is 17200
Therefore $17200 = 64M + A$
And $M \geqslant A$

Let $A = 0$ Then $M_{min} = \dfrac{17200}{64} = 268.75$

$= 268$

and $M_{max} = \dfrac{17600}{64} = 275.0$

Thus the M counter must be programmable from 268 to 275 as required: the M counter must have at least 9 bits.

For a frequency of 433.975MHz

$$P = 433.97/0.025 = 17359$$

therefore $$M = \frac{17359}{64} = 271.2343$$

The A counter is programmed for the remainder i.e.

$$0.2343 \times 64 = 15$$

From this, the A counter is programmed to 15 and the N counter to 271. The output frequency can now be checked.

$P = NM + A$
$= 271 \times 64 + 15 = 17359$
and this is the required divider ratio.

The two modulus prescaler is therefore able to offer the advantages of producing a programmable divider operating at a very high frequency, but consuming a fraction of the power of such a divider. This enables the reference frequency to equal the channel spacing, thus allowing maximisation of loop bandwidth with its concomitant faster lock up time. It is limited by total loop delay, maximum operating frequencies of dividers and counters, and in minimum count values, but is nevertheless a powerful tool for the synthesiser designer.

The limitation on the value of P_{min}, the minimum ratio can be avoided by the use of three and four modulus dividers. The use of a four modulus counter allows a very wide frequency range to be covered with one device, but at the expense of a much higher power dissipation. Typical of such devices are the Plessey SP8901 and SP8906. Power consumptions for 2-modulus dividers typically range from 4mA at 200MHz (Plessey SP8792/3) through 11mA at 520MHz (Plessey SP8716/8/9) to 25mA at 1GHz (Plessey SP8703).

LOOP BANDWIDTH AND PHASE NOISE

As stated earlier, phase noise is a very important parameter in frequency synthesisers. Too many early synthesisers suffered from phase noise problems which manifested themselves as poor equipment performance in such areas as multiple signal selectivity and ultimate signal to noise ratio. The performance of the synthesiser may be degraded or improved by changing the loop bandwidth, depending upon the characteristics and parameters involved.

The general characteristics of a phase locked loop (PLL) are that for signals injected into the loop it acts as a low pass filter for signals inside the loop bandwidth, and as a high pass filter for signals outside the loop bandwidth. To analyse the performance, consider modulation of the VCO at very low frequencies. The output of the phase detector will be a low frequency signal of phase such as to attempt to remove the modulation imposed on the VCO. As the modulation frequency increases, the error component of the phase detector output is not passed by the loop filter, and so the modulation is not removed by the loop. Note that the modulation is phase modulation (PM) up to the filter break point, and frequency modulation (FM) thereafter. In the 'in-between' range, some interesting distortion effects can occur, especially when excessive group delay exists in the loop filter.

The relationship of loop filter bandwidth to phase noise is now apparent. Phase noise from the oscillator corresponding to frequencies below the filter bandwidth will be removed by the loop, while phase noise components outside the loop bandwidth will be unaffected by the loop. Under these circumstances then, the VCO output spectrum will be cleaned up by the loop. However, for frequencies inside the loop bandwidth, other factors enter. Variations in the reference frequency cause variations in output frequency from the synthesiser, and phase noise components at the reference frequency are purely the frequency domain transforms of time domain frequency instability (Refs. 6,7 and 8). These phase noise effects are multiplied in the loop by the divider ratio. An example (admittedly using gross instability for demonstration) is shown.

If the 430MHz synthesiser has an instability of +1Hz in the 25kHz reference frequency, this is multiplied by P.

i.e. for operation at 433MHz
$P = 433/0.025 = 17320$

Therefore IF +1Hz at 25kHz gives +17.32kHz at final frequency.

Phase noise at the reference frequency is derived from two sources:

(a) the system standard oscillator
(b) the reference chain divider

Oscillators for standards are available with very low phase noise characteristics, and -130 to -170dBc/Hz at 1kHz offset covers the usual range. This phase noise is modified by the reference divider and multiplied by the division ratio as explained above. Of course, phase noise at any offset is reduced by division until the phase noise floor of the divider is reached. Little has been published on the causes of phase noise in dividers, although various measurements have been made (Ref. 9). It has been suggested that TTL and CMOS dividers are better than ECL and CMOS is better at low (10-20Hz) offsets. At a 1kHz offset, ECL levels of about -155 to -165dBc/Hz appear usual. The explanations for the occurence of phase noise is intuitively regarded as being jitter in the transition point of the signal: on this basis, one would not expect CMOS to be so good as TTL insofar as the rise and fall times will be somewhat slower. Regrettably, the difficulty and cost of making meaningful measurements is an inhibiting factor: data on the phase noise performance of Gallium Arsenide dividers would be of considerable interest, especially at small frequency offsets.

From the above discussion, a phase noise floor of some -150dBc/Hz can be expected at the end of the reference frequency divider chain if a good frequency standard is used, while a low cost one may well be at about -130dBc/Hz. In our 430MHz synthesiser, a degradation at 1kHz (if the loop is wide enough) of some 84dB will be seen, so inside the loop bandwidth, the noise performance will be limited to -130 + 84 = -46dBc/Hz. At lower offset frequencies, the phase noise of dividers and frequency standards is worse, so the phase noise performance is now being defined by the loop, rather than the VCO. These are worst case figures, but the ultimate signal to noise ratio of an FM receiver can clearly be seen to be easily limited at UHF by multiplied phase noise. Fortunately, the noise enhancement by the loop is such that pre-emphasis of the modulation provides major improvements in signal to noise ratio.

Nevertheless, it is obvious that the choice of loop bandwidth is compromised by the ultimate signal to noise level required by the system and that such factors as reference oscillator noise level and divider noise cannot be totally disregarded. Operation in the usual cellular radio bands at 800 or 900MHz makes the situation some 6dB worse than that analysed above and the use of a psophometric audio weighting in the equipment is advisable. Sub audible tones may well need fairly high deviation if signal to noise performance is not to be severely limited on them, although modern decoders will work with a negative signal to noise ratio (Ref.10).

In the single loop synthesiser, the phase noise in adjacent channels, which determines the adjacent channel performance, is, to a first order, unaffected by the loop and its parameters. Second order effects such as noise modulation

by such loop components as high value resistors and operational amplifiers may be negated by the use of a passive low pass filter prior to the VCO. Phase noise in the oscillator is discussed below.

Even where the effects of multiplied phase noise may be ignored, such as where the reference divider chain noise is sufficiently low, certain other problems occur in the loop filter design. Many of these are associated with the phase detector employed, which in many areas has been a digital phase/frequency detector. Various types of detector have been used over the years, from an OR gate producing a variable mark space ratio to the well known 2 D type detector. The first of these used integration of the variable mark-space ratio to produce the required output, while the latter (Fig.6) produces minimal width pulses on both Φu and ΦD when in the zero phase error condition. Unfortunately, the zero phase error state exists for a degree of phase error dependent upon the propagation of the gates and a phase error/output voltage characteristic such as Fig.7 is achieved. The performance in the central flat portion of the characteristic means that the loop gain falls to zero when the phase error reaches some small but finite value, and this leads to an increase in the low frequency phase noise of the loop. This phenomenon is of course related to the reference frequency of the loop, being worse at high comparison frequencies.

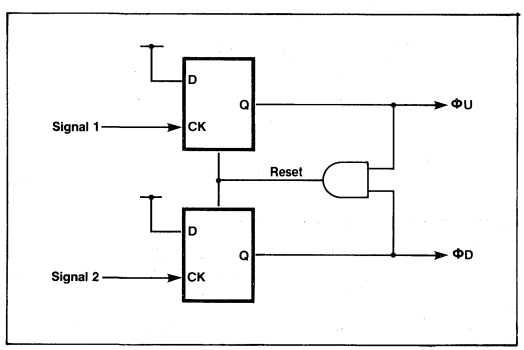


Fig.6 Dual D type phase discriminator

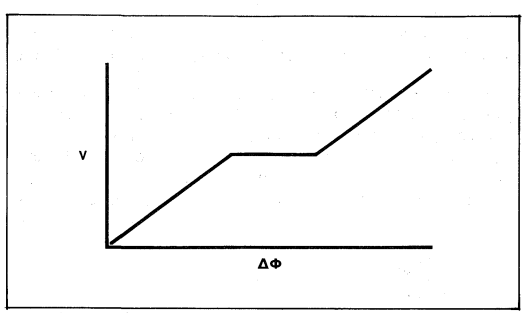


Fig.7 Transfer characteristic of phase discriminator with a charge pump

Although a number of approaches have been made to minimise this problem, including the provision of a leakage path across the VCO control line (Ref. 16), the better approach is to use a linear phase detector of high gain to 'fill in' the gap in the response. An additional benefit of this method is that if the digital phase detector has a 'tri-state' output for the area in which the dead zone occurs and the linear phase detector operates, then the phase detector output at comparison frequency is reduced, allowing either a wider loop bandwidth for the same comparison frequency sideband rejection, or increased rejection, or to some extent, both. The analog phase detector may easily be given a very high gain and narrow range of operation - say a 2 degree range with a gain of 600 volts/radians, but only a limited lock range. It is however, essential to ensure that saturation of this detector, and indeed of the loop filter/amplifier is minimised, as under channel change conditions, the control line and thus the filter amplifiers can be driven hard into saturation. A long recovery time here may well make a mockery of any lock up time calculations. It is this approach which has been adopted in the NJ8820 series of CMOS control circuits from Plessey with a large degree of success.

The choice of loop bandwidth is also governed by the time to change channel, and here again, compromise is often necessary. For example, a lock up time of 1ms and a loop bandwidth of 100Hz are apparently mutually incompatible. By using the two detector approach outlined above however, the loop bandwidth for the digital detector may be made much wider than the analogue detector, thus providing a form of adaptive filtering. The basic loop equation for a type 2 2nd order loop is

$$\omega_n = \sqrt{\frac{K_0 K_v}{N t_1}}$$

where ω_n = loop natural frequency, K_v = VCO gain in Rad/S-v, K_0 = phase detector gain in volts/rad, N = division ratio and t_1 = integrator time constant, shows the dependence of ω_n, the loop natural frequency on N. It should be noted the 3dB bandwidth of the loop and the natural frequency ω_n, are not identical - except for a damping factor, $D = 3.02$.

It was stated earlier that noise caused by the phase detector and loop filter is easily filtered to avoid noise in adjacent channels and the use of low-noise components in loop filters (NOT a 741!) is advisable. Where possible, time constants should use large capacitors and small resistors to minimise KTBR noise. 1/*f* noise can be a problem with operational amplifiers, and where loop bandwidth is high, slew rate is important if the dynamic loop bandwidth is to beary any relationship to the small signal case.

To summarise, the choice of loop bandwidth affects close in phase noise and lock up time. Phase noise is produced by dividers, phase detectors and filters, and when multiplication ratios are high, the reference frequency phase noise can be dominant when multiplied. To minimise this effect, the loop bandwidth can be narrowed, since noise outside the loop bandwidth is determined soley by the VCO. Typical divider phase noises of -150 or -160dBc/Hz can be expected, so low cost reference oscillators can dominate the noise performance.

VOLTAGE CONTROLLED OSCILLATORS

Many engineers consider VCO design to be a black art, and although some art is occasionally involved, VCOs are amenable to analysis.

In the single loop synthesiser, the phase noise performance outside the loop bandwidth is dominated by the VCO, with the noise generation by passive components in the loop filter generally being of lesser importance.

Scherer, Leeson (Ref.12) and Robins (Ref.13) have analysed oscillator phase noise performance and Scherer (Ref.14) has demonstrated the applicability of Leeson's equations and uses the equation

$$L_{(f)} = \tfrac{1}{8} \left[\frac{FkT}{P_s}\right] \frac{(fo)^2}{(f)} \left[\frac{1}{Q} + \frac{P_o}{\tfrac{1}{2}CV^2 2\pi f.}\right]^2 \quad \text{Eq. 1}$$

where $L_{(f)}$ is the SSB phase noise at an offset F
F is the Noise Figure of the amplifier in the oscillator
k is Boltzmann's Constant
T is the Temperature
P_s is the available signal power
f_o is operating frequency
f is the offset at which the power is to be calculated
Q is working Q of the tuned circuit
C is tank capacity
V is tank current peak voltage
P_o is rf output power

By inspection of Eq. 1, it may be seen that the phase noise is proportional to Q^{-2} and also to (frequency offset)$^{-2}$. This means that for each octave decrease in the offset frequency, the noise power will increase by 4 times or at 6dB/octave. As the frequency offset decreases 1/f or flicker noise becomes important: this 'break' frequency can be as high as 50MHz with GaAs devices. From Eq. 1, it may be determined that a low phase noise oscillator will have a large voltage swing, a high working Q and provide little output power to the load. There is of course a limit as to the level of power required, as the noise of any subsequent buffer amplifiers will degrade the oscillator.

A major compromise in the design of equipment is the choice of VCO frequency. If, for example, a 800MHz cellular radio type of receiver is considered, some fairly straightforward calculations will serve to act as a guide. Starting with the receiver parameters, we will assume that a 70dB rejection of a signal two channels (60kHz) away is required. A numbr of receiver sub system parameters are involved.

(a) Synthesiser phase noise
(b) IF filter performance
(c) Co-channel rejection ratio
(d) Gain compression of stages before the main IF selectivity.

Of these parameters, (c) is the least obvious in its applicability. Ref.1 showed how oscillator noise was mixed onto a wanted signal by a strong unwanted signal. The degradation of a wanted signal by this noise obviously depends upon the relative levels of signal and noise, and because the noise is on the same frequency, the Co-channel rejection. Typically, this means that a noise level within the IF passband of some 8dB less than the signal is required. Thus for the 70dB rejection, oscillator noise at -78dB is required, and 80dB would thus be the design aim.

Conversion of this level to dBc/Hz is not straightforward because of the non linear slope of the phase noise. However, for narrow bandwidths at large offsets, little error is obtained by approximating the phase noise slope to a straight line. This may be illustrated as follows:

From Eq. 1, the power spectrum at an offset beyond the flicker noise knee is given by:

$$P_o = Kf^{-2}$$

where P is the noise power
K is a constant
f is the offset

For a frequency band bounded by f_{lower} and f_{upper}, the noise power is:

$$P_t = \int_{f_L}^{f_U} Kf^{-2}\,df = \left[-Kf^{-1}\right]_{f_L}^{f_U}$$

$$= K(f_L^{-1} - f_U^{-1})$$

Therefore

$$K = \frac{P_t}{(f_L^{-1} - f_U^{-1})}$$

P_t has been defined as the phase noise in the band = -80dB therefore

$$K = \left[\frac{10^{-8}}{\frac{1}{53.5 \times 10^3} - \frac{1}{67.5 \times 10^3}}\right] = 2.58 \times 10^{-3}$$

To find the phase noise in a 1Hz bandwidth at an offset f

$$P = Kf^{-2}$$

so at 53.5kHz

$$P = \frac{2.58 \times 10^{-3}}{(53.5 \times 10^3)^2} = 0.901 \times 10^{-15}$$

$$= -120.5\text{dBc/Hz}$$

At 60kHz

$$P = -121.4\text{dBc/Hz}$$

and at 67.5kHz

$$P = -122.5\text{dBc/Hz}$$

If the 'break point' for 1/f noise is above 60kHz, then the spectral density is determined by noise rising at f^{3}. Similar procedures are followed:

$$P_o = K'f^{-3}$$

$$P_t = \int_{f_L}^{f_U} K'f^{-3}\,df = -K'\left[\frac{f^{-2}}{2}\right]_{f_L}^{f_U}$$

$$= \frac{-K'}{2}(f_U^{-2} - f_L^{-2})$$

$$= \frac{K'}{2}(f_L^{-2} - f_U^{-2})$$

Using similar figures, the performance required is:

53.5kHz	-120.0dBc/Hz
60.0kHz	-121.5dBc/Hz
67.5kHz	-123.0dBc/Hz

The error by assuming a linear relationship is given by:

IF bandwidth = 15kHz
therefore noise power is 10 log$_{10}$ 15 x 10^{3}dB greater than in a 1Hz bandwidth
which is 41.8dB
therefore if the noise power is 80dB down on the signal, total carrier to noise power ratio is -121.8dBc/Hz at 60kHz.

This in fact gives a requirement some 0.4dB higher than previously calculated and in 120dB is obviously negligible.

Having decided upon the level of allowable oscillator noise, it is now possible to calculate the best methods of achieving this level. Using Scherer's figures from Ref.13 for a 400MHz oscillator which will be doubled, using parameters of:

Q = 200
C = 23pF
V = 10V pk
$\frac{FKT}{P^2} = \left[\frac{6nV}{1V}\right]^2$ where 6nV is the noise voltage and 1V is the input before limiting.

The noise power P at a 30kHz offset is, from Eq. 1, -135dBc/Hz.

So far flicker noise has been ignored. Flicker noise is a low frequency phenomonen which causes problems by intermodulation with the carrier frequency to produce noise sidebands. The 'break point' at which flicker noise becomes dominant varies but a UHF VCO of the type under consideration would probably have a break point at about 50-150kHz offset from the carrier. Eq. 1 needs some

modification to include this factor and a multiplicand of

$$\frac{(1 + f_e)}{f}$$

may be used, where f_e is the 1/f noise corner frequency.

The previously calculated noise will now be degraded by about 8dB under these conditions, (assuming $f_e = 150kHz$) and will now be -127dBc/Hz. This is about 5dB inside the previously calculated requirement. Note that calculations have been made on the basis of a 30kHz offset to allow for doubling the oscillator frequency.

Considering an oscillator with a fundamental frequency of 800MHz, a number of problems appear. Ignoring for the time being the increased noise figure of the device, the available Q of components is considerably less - for example high quality chip capacitors can offer *Q's* of about 200, leading to working *Q* of about 100. Calculating noise levels for a 60kHz offset with all other parameters constant except tank capacity which is 12pF (half the 400MHz oscillator) the noise at 60kHz is -105dBc/Hz or about 17dB outside the requirement. Obviously, these figures are no more than a guide, but the suggestion is that the doubled 400MHz oscillator will meet requirements, while the 800MHz oscillator will not (see Fig.8).

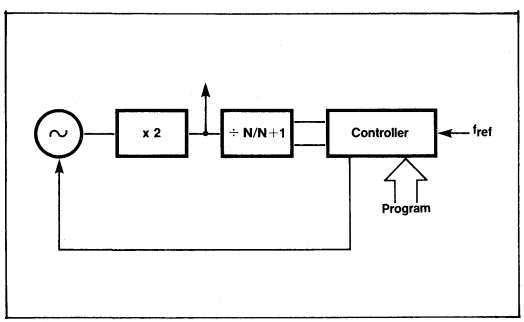


Fig.8 Use of a lower frequency oscillator for improved phase noise

Flicker noise can be reduced by the inclusion of local DC negative feedback, such as an unbypassed emitter resistor, but a major requirement is to choose a suitable device. In general a low phase noise oscillator will run at high power, using a device with both low flicker noise and low high frequency noise, and with high gain and minimum damping on the tuned circuit. In fact, in many applications, the thermionic tube is attractive! *Q* should be as high as possible, and where VCOs are concerned, the MHz/V should be minimised. This is because of the effects of noise - at 10MHz/V, 1 microvolt of noise will produce 10Hz of FM deviation.

Where relatively wide frequency ranges are concerned, the variation in loop bandwidth may cause problems.

$$\omega_n = \sqrt{\frac{K_o K_v}{N t_1}}$$

where ω_n = natural loop frequency
K_o = VCO constant
K_v = phase detector constant
N = divider ratio
t_1 = integrator time constant

ω_n varies with *N*, and where desirable to maintain equal lock up times and loop bandwidth, K_v may be designed to vary with *N*. Several methods exist, but the use of a transmission line VCO can prove useful, as the effective inductance increases with frequency. The use of a suitable length of transmission line can provide an oscillator tuneable from 130 to 190MHz with a coarse tuning trimmer, and electrically tuneable over 6MHz at the bottom of the band to 8.75MHz at the top, thus maintaining ω_n sensibly constant. The use of PIN diodes to switch capacitors is possible, although care must be taken not to degrade *Q* e.g. a 10pF capacitor at 150MHz has $X_c = 106\Omega$. A PIN diode with an ON resistance of 0.5Ω will give $Q_{MAX} = 212$, assuming a perfect capacitor, and as considered earlier, this can have disastrous effects on phase noise performance.

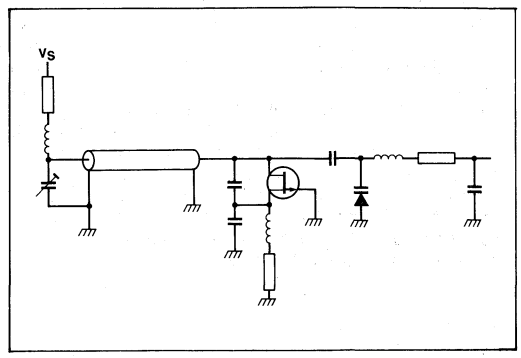


Fig.9 Transmission line VCO using the line as an impedance inverter

An initially attractive method of realising the transmission line VCO is shown in Fig.9, where a length of line is used as a reactance inverter, changing the capacity into an inductance. The use of a Smith Chart will, however, show that the resulting inductance will have a low reactance unless the terminating capacitor is large and the line relatively long (greater than ⅛ wavelength). This leads to a low *Q* circuit as the resistance of the line is constant, and measurements made using a 16cm rigid coax 75Ω line with a loss of 4dB/100ft at 150MHz gave a *Q* of less than 100. This line was terminated with an air spaced trimmer. The same line as a shortened capacitively loaded resonator as in Fig.10 had a *Q* of over 250.

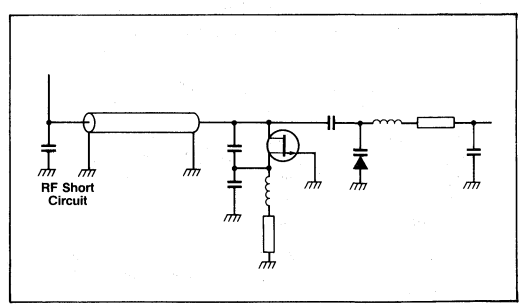


Fig.10 Transmission line VCO using a shortened λ/4 line capacitively loaded

SUMMARY

The compromises in the synthesiser design are now apparent: a narrow bandwidth is required to minimise multiplied reference noise, but a wide bandwidth is needed to minimise lock up time. A high oscillator frequency may be required to avoid spurious outputs and multiplier chains, while a low frequency and multiplier chain give the best performance on system phase noise and possibly power consumption. The classical way to minimise these problems is the two loop synthesiser, but cost is a determining factor effecting the compromise finally reached. Power consumption is always a problem and unfortunately is more demanding at high frequencies while increasing channel occupancy will lead to ever tighter performance requirements in terms of phase noise and switching time.

Modern integrated circuits help the designer by providing better phase detectors and faster lower power dividers. Nevertheless, the single loop synthesiser has been shown to involve a number of compromises in its design, and in some cases, these compromises may limit the final equipment performance level. The single loop synthesiser is very useful, but is not universally applicable.

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The care and feeding of High Speed Dividers

Circuit design and layout for high speed dividers operating at frequencies up to 2GHz owe much more to analog RF design techniques than normal digital ones and the limitations on flexibility and component choice inherent in UHF RF design are of paramount importance in successful designs.

PRACTICAL DESIGN CONSIDERATIONS

High speed divider applications require the printed circuit boards to be mechanically designed with two considerations in mind:

(1) Electrical performance
(2) Mechanical and thermal performance.

These two considerations are inter-related; for example, the use of 1/16 inch thick fibreglass PC board may be desirable mechanically, but a 50Ω stripline on this thickness of board is about 5/32 inch wide, and is thus too wide to pass between the pins of an IC.

Most of the heat conducted from a dual-in-line IC package is removed from the bottom of the package. Less than 10 % is conducted out by the leads, and because of the cavity between the chip and lid, relatively little through the top of the package.

For this reason, the use of a double-layer PC board layout is recommended, with a ground plane top surface. Where 1/32 inch thick material is used, a top surface ground plane will add substantially to the heat dissipation capabilities of the board.

For use at very high frequencies, consideration must be given to the type of component used. Carbon composition resistors are more nearly resistive at high frequencies than either carbon or metal film types, and are available in very small sizes. Bypass capacitors need to be chosen carefully if they are to act as low impedances, as series inductance leads to an increasing impedance with frequency above the series resonant frequency of the device. As a guide, a 1000pF disc ceramic capacitor with 1/4 inch leads will be self resonant at about 75MHz, and will appear as an inductive impedance of about 22Ω at 800MHz. The use of chip capacitors is recommended above 500MHz, although leaded monolithic ceramic capacitors with suitably short leads are often acceptable.

The use of a ground plane for RF decoupling purposes is often recommended, and can be helpful. However, the danger is that the ground current paths in the plane are not defined very well, and because of this lack of definition, the ground plane can cause unsatisfactory operation. Probably the best method is to return all the bypass capacitors to a single point (as in Fig.1) and return this point to the ground plane.

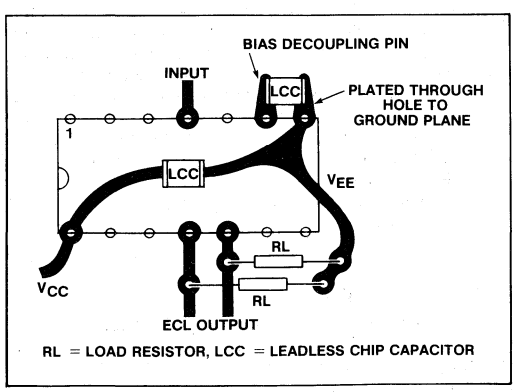

Fig.1 Single point grounding

Also note that in Fig.1 the output load resistors have their grounded ends connected together and a common return used. Because the currents in the resistors are in antiphase, cancellation of the inductive effects taken place, and the path followed by the relatively large output currents is controlled. Defining the ground current path is more important in applications like frequency synthesis, where a relatively large part of the system may be on one PCB.

It is well known that the effect of mismatching a transmission line is to cause variations in the voltage along the line. Standard practice at Plessey Semiconductors has been to use a 5:1 attenuator manufactured from 'microdot' resistors as an attenuator feeding a 50Ω sampling oscilloscope or a power meter. Although a high VSWR will exist on the line from the generator to the test fixture, the theory is that the line from the power meter to the attenuator will be a matched line, and so the power measured is 14dB lower than the power at the device input pin. This method has been proved very successful, even if simple, and offers some advantages over the use of hybrids or directional couplers.

The use of a matched 50Ω system can help, and using microstrip techniques, a track with a defined impedance is reasonably practical. The impedance of a microstrip line is given by:

$$Z_O = 377\ (L/w)\ (1/\varepsilon_r)$$

Where L = dielectric thickness, w = width of track and ε_r is the relative permeability of the board material.

Some correction factors have to be applied, and typically, on 1/16 inch glass fibre epoxy board, the following sizes provide a guide to track width

100Ω - 1mm
75Ω - 2mm
50Ω - 4mm

These impedances rely on the ground plane on the obverse of the board being complete, and where boards are wave soldered, it may be necessary to make arrangements to prevent blistering.

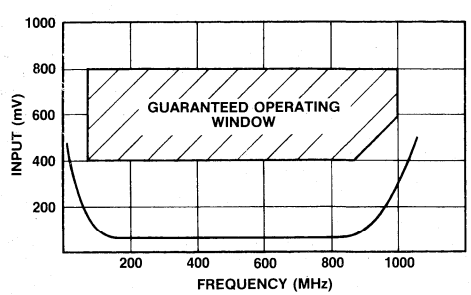

Fig.2 Example of input sensitivity curves

The input level of a divider should be maintained within the guaranteed operating window shown on its data sheet (Fig.2). Excessive input can vary in its effects, from causing permanent damage to miscounting, especially when cold. Running the device at too low a level can cause problems, even though the level is within the 'typical' performance line of the device. An ECL output signal on pin 6 of the device in

Fig.3 can couple 60mV of signal to the input shown on Fig.2 at 500MHz. Such a level of coupling can lead to divider jitter if the input signal is low, and it becomes very necessary to keep the inputs and outputs well separated at the higher frequencies. This includes ECL lines to modulus control pins on two modulus dividers.

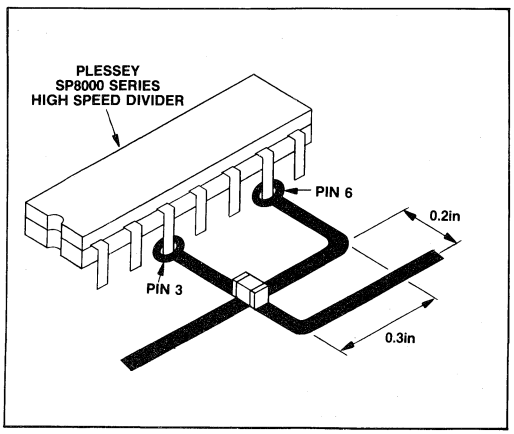

Fig.3 Coupling between parallel tracks

Most dividers are edge triggered, and although they are specified over a frequency range with sine wave input, they will operate to lower frequencies provided a suitably high slew rate is provided on the input signal. This is generally of the order of 100 to 200 volts/microsecond. This should be achieved by shaping of the input signal, for example by limiting, rather than by overdriving the device.

The outputs of devices may be of the following forms:

(1) ECL
(2) Open collector TTL
(3) TTL
(4) CMOS

Of these, the ECL output is well defined; some devices require external load resistors and the data sheet should be consulted. Where these external resistors are required, suitable interconnection techniques should be used between them and the device; the resistors should be carefully chosen for their non-inductive properties when output frequencies are very high. Where an ECL output divider drives another divider it is best to AC couple, since few dividers are strictly ECL-compatible on their inputs.

Open collector TTL outputs are relatively slow. Although the negative edge is limited in speed by the turn-on time of the output transistor, the rising edge is limited by the external load resistor and capacitance to ground. In practice this means that short narrow tracks are required to the following device, and a minimum 'fan-in' load provided. In addition, open collector TTL should not be used above about 10MHz output frequency.

True TTL outputs are not so limited, because of the active pull-up. Nevertheless, the use of such outputs at frequencies above about 25-30MHz is not recommended, especially into capactive loads. Loads of more than 30pF should not be driven faster than about 15MHz. Note that the current drawn by true TTL outputs increases with increasing load capacitance.

CMOS outputs are, on the face of it, TTL-compatible. However, investigation will show that the outputs are not guaranteed to meet TTL levels at TTL currents and it is not recommended that CMOS output devices be used to directly drive TTL. Where an interface of this sort is required, an active transistor interface should be used.

Fig.4 shows a circuit for an ECL-TTL interface, using a line receiver. Simple circuits using one or two transistors cannot be guaranteed to work over all the tolerances of ECL output voltages and temperature ranges.

Interfacing to dividers is not difficult if a few simple rules are obeyed. These are:

(1) Observe the input requirements - guaranteed input operating area, and slew rate.
(2) Do not use open collector outputs above 10MHz.
(3) Do not use CMOS outputs to drive TTL.
(4) Use a sensible layout with good components, and sensible values - 0.1 microfarad ceramic capacitors are NOT bypasses at 1.5GHz.

Treating dividers as RF linear devices is probably the best way to ensure successful applications at high frequencies. There is no magic in HF design, only intelligent layout and sensible component choice.

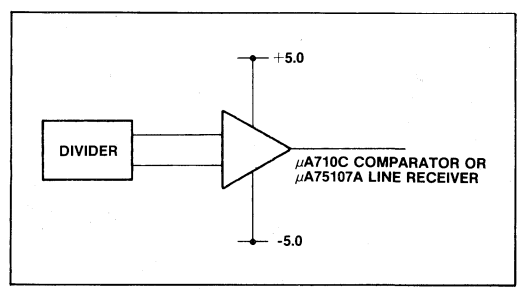

Fig.4 ECL/TTL interface

Impedance Matching

The use of microstrip techniques has been mentioned already. However, in itself this will not produce a matched network and various possibilities exist to improve the matching at the input of a device. These include Tchebycheff impedance transforming networks, narrow band 'L' matching networks, and at high enough frequencies, the use of transmission lines. Wideband matching is often difficult, and attempts should be made to use networks that have the lowest possible working Q. This is for two reasons: firstly a high Q network will not only be narrow band, but will have the capability of increasing the losses, and secondly, a low Q network is generally more tolerant of component variations.

The greater losses in high Q circuits occur because of the greater circulating current: the loss power is I^2R, so that if the Q is doubled with all else constant, the power loss is increased by 4 times.

The easiest method of determining matching components is by means of the Smith Chart.

THE SMITH CHART

The input impedance of SP8000-series high speed dividers varies as a function of frequency and is therefore specified on the datasheets by means of Smith Charts. The following information is included in this handbook as a guide to their interpretation and use.

Construction of the chart

The chart is constructed with two sets of circles, one set comprising circles of CONSTANT RESISTANCE (Fig. 5) and the other circles of CONSTANT REACTANCE (Fig. 6). The values on these circles are normalised to the characteristic impedances of the system by dividing the actual value of resistance or reactance by the characteristic impedance e.g. in a 50Ω system, a resistance of 100Ω is normalised to a value of 2.0.

By combining Figs. 5 and 6 to form Fig. 7, a chart is produced in which any normalised impedance has a unique position on the chart, and the variation of this impedance with frequency or other parameters may be plotted.

A further series of circles may be plotted on the chart: these are circles of constant VSWR, and represent the degree of mismatch in a system. The VSWR is the ratio of the device impedance to the characteristic impedance, and is always expressed as a ratio greater than 1: thus a 25Ω device in a 50Ω system gives rise to a 2:1 VSWR. These circles of constant VSWR have been added in Fig. 7.

Any point can be represented on the Smith Chart: for example an impedance of 150-*j*75Ω can be represented by a normalised impedance (in a 50 Ω system) of 3-*j*1.5 and this point is plotted in Fig. 7 as point A.

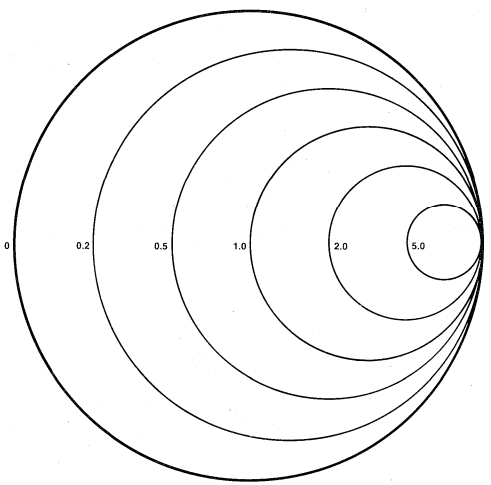

Fig.5 Constant resistance circles

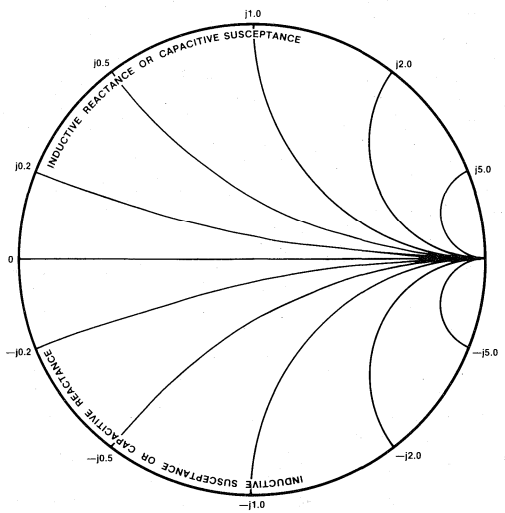

Fig.6 Constant reactance circles

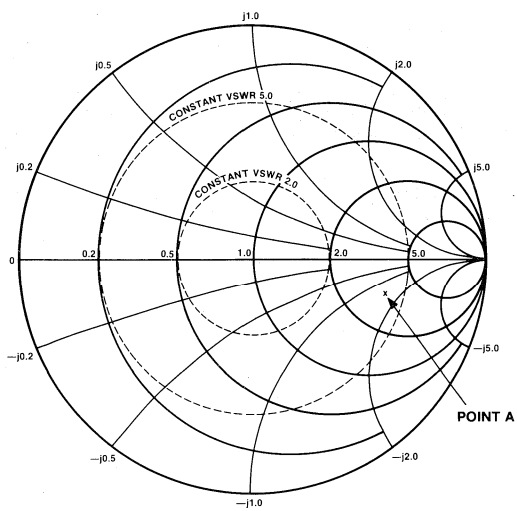

Fig.7 The complete chart

Network calculations

The main application for Smith Charts with integrated circuits is in the design of matching networks. Although these can be calculated by use of the series to parallel (and vice-versa) transforms, followed by the application of Kirchoff's Laws, the method can be laborious. Although the Smith Chart as a graphical method cannot necessarily compete in terms of overall accuracy, it is nevertheless more than adequate for the majority of problems, especially when the errors inherent in practical components are taken into account.

Any impedance can be represented at a fixed frequency by a shunt conductance and susceptance (impedances as series reactance and resistance in this context). By transferring a point on the Smith Chart to a point at the same diameter but 180° away, this transformation is automatically made (see Fig. 8) where A and B are the series and parallel equivalents.

It is often easier to change a series RC network to its equivalent parallel network for calculation purposes. This is because as a parallel network of admittances, a shunt admittance can be directly added, rather than the tortuous calculations necessary if the series form is used. Similar arguments apply to parallel networks, so in general it is best to deal with admittances for shunt components and reactances for series components.

Admittances and impedances can be easily added on the Smith Chart (see Fig. 9). Where a series inductance is to be added to an admittance (i.e. parallel R and C), the admittance should be turned into a series impedance by the method outlined above and in Fig. 8. The series inductance can then be added as in Fig. 9 (see also Fig. 10).

Point A is the starting admittance consisting of a shunt capacitance and resistance. The equivalent capacitive impedance is shown at point B. The addition of a series inductor moves the impedance to point C. The value of this inductor is defined by the length of the arc BC, and in Fig. 10 is $-j0.5$ to $j0.43$ i.e. a total of $j0.93$. This reactance must of course be denormalised before evaluation. Point C represents an inductive impedance which is equivalent to the admittance shown at Point D. The addition of shunt reactance moves the input admittance to the centre of the chart, and has a value of $-j2.0$. Point D should be chosen such that it lies on unity impedance/conductance circle: thus a locus of points for point C exists.

This procedure allows for design of the matching at any one frequency. Wide band matching is more difficult and other techniques are needed. Of these, one of the most powerful is to absorb the reactance into a low pass filter form of ladder network: if the values are suitably chosen, the resulting input impedance is dependent upon the reflection coefficient of the filter.

At frequencies above about 400MHz, it becomes practical to use sections of transmission line to provide the necessary reactances, and reference to one of the standard works on the subject is recommended.

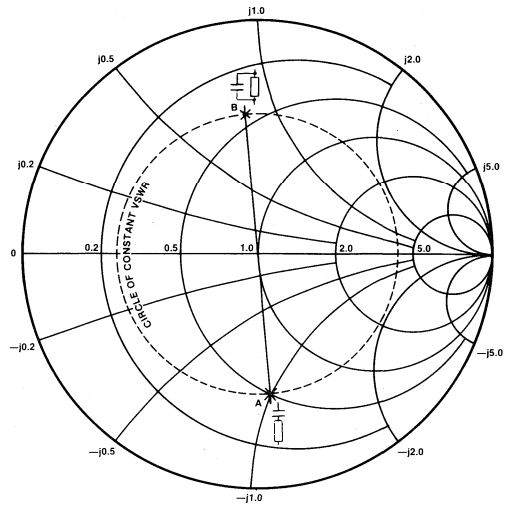

Fig.8 Series reactance to parallel admittance conversion

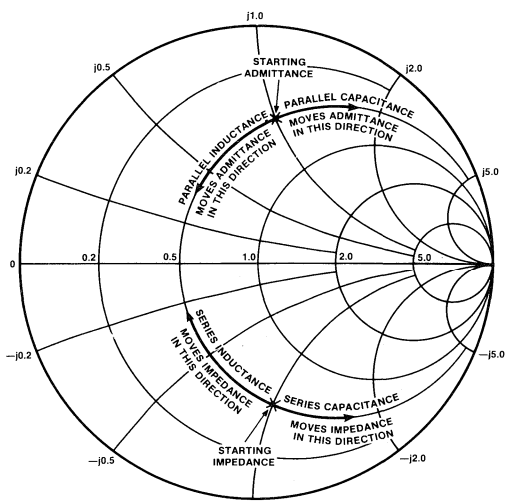

Fig.9 Effects of series and shunt reactance

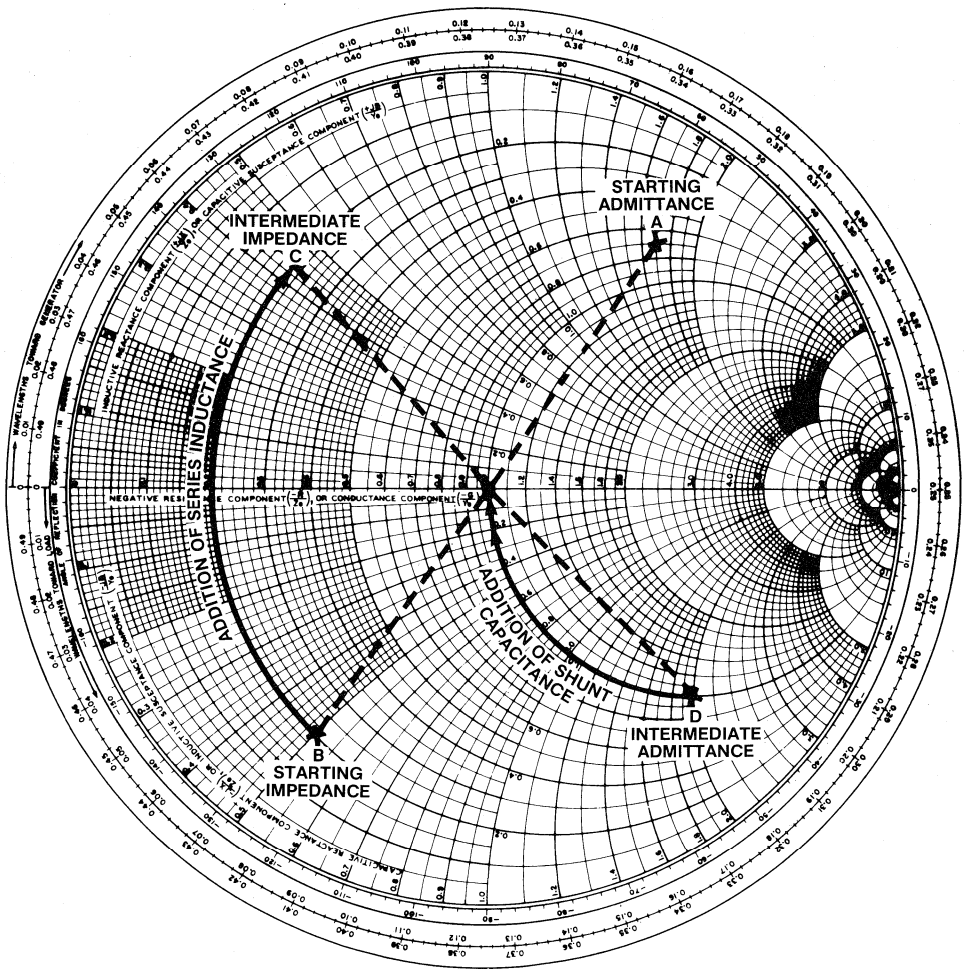

Fig.10 Matching design using the Smith Chart

PHASE NOISE AND DIVIDERS

Phase noise is becoming increasingly important in systems and it is necessary to minimise its effects. First, however, phase noise must be defined.

A spectrally pure signal of a given frequency would appear on a perfect spectrum analyser display as a single straight line as in Fig.11. If the signal is frequency modulated with a discrete modulation frequency, the result will be a comb of frequencies as in Fig.12, while modulation with noise will produce an output spectrum as in Fig.13. Note that the noise density decreases as the offset from the carrier increases. This effect is the result of the effectively lower modulation index *m*. In the case of a Voltage Controlled Oscillator modulated by white noise, a similar effect will be seen, because for a given deviation *f*, the modulation index *m*, (= 1/*fmod*) is greater for lower frequencies than for higher frequencies. Thus the number of sidebands is greater for lower frequencies, and the noise spectral density increases as the carrier is approached.

The causes of phase noise in dividers are not well understood, but the effects of internal noise on the switching point of the various flip-flops cannot be ignored. The 1/*f* noise will obviously inter-relate to the phase noise if this is so, and it is interesting to note that various measurements of Gallium Arsenide dividers suggest performances 20 to 30dB worse than for ECL dividers. Rohde (ref. 4) suggests that TTL and CMOS are much better than ECL, although little work has been published in this field, possibly because of the measurement difficulties.

The non-saturating nature of ECL, the fact that the transistors are designed and processed for high speed rather than low noise, and the smaller signal swings than TTL or CMOS, lead intuitively to the conclusion that ECL should be worse than either of these other two logic families. This appears to be the case, while the high 1/*f* noise knee of Gallium Arsenide devices leads to the high relatively close in phase noise.

Devices with slow output edges, such as open collector TTL output stages may also be expected to be worse, which is again born out in practice.

Minimisation of phase noise requires the use of well-filtered supplies, correct input levels and minimisation of noise in level changing circuitry.

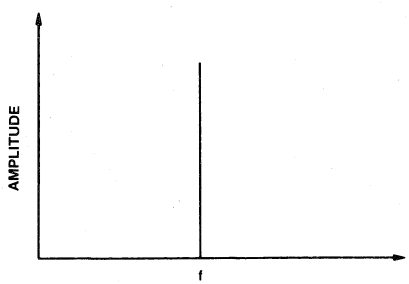

Fig.11 Spectrally pure signal

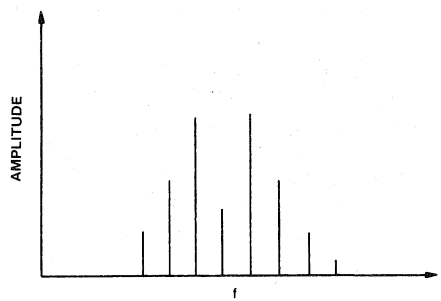

Fig.12 Spectrally pure signal, frequency modulated with single tone

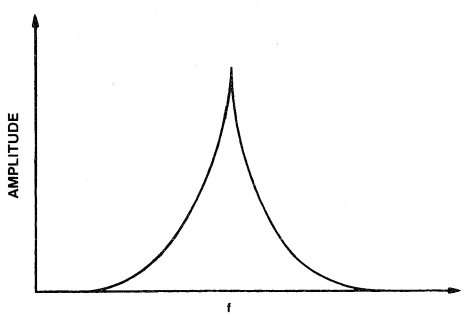

Fig.13 Spectrally pure signal, frequency modulated by noise

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Universal Programmer for GPS Synthesiser ICs

The programmer described in this application note will provide the data required to program any of the Plessey NJ8820 or NJ88C30 series of Synthesiser ICs. This circuit can be made from readily available CMOS logic ICs and a single 2K byte eprom (type 2516), and requires only a +5V supply.

BRIEF CIRCUIT DESCRIPTION

The program cycle is initiated by pressing the momentary switch S1. This generates a pulse which clocks the 4013 D-latch which in turn resets the 4040 counter; the same clock pulse is passed to the output buffer as a program enable signal for the NJ8820 or NJ8821/23.

The Q2 to Q7 outputs of the counter then sequentially address 64 locations in the eprom, the start address of which is determined by Hex switch S2 which is used to set bits A9 to A6 of the eprom address. The data outputs of the eprom D6-D4 are used to generate data select signals DS2-DS0 (NJ8821/23) and to provide a 3-bit address to the 4051 multiplexer which in turn selects one of the eight hex switches S3-S10.

The MSB of switch S2 selects, via the 74HC157 multiplexer, either the data bits D6-D4 from the eprom or the data select signals DS2-DS0 from input buffers (NJ8820).

Data output D3-D0 (NJ8820/21/23) from the output buffer is determined by setting the 8 hex switches S3-S10. The serial data output is derived from D3-D0, via a 74HC153 multiplexer, which is in turn controlled by data bits D3 and D2 from the eprom.

Eprom data output D1 and D0 generate the clock and enable signals respectively.

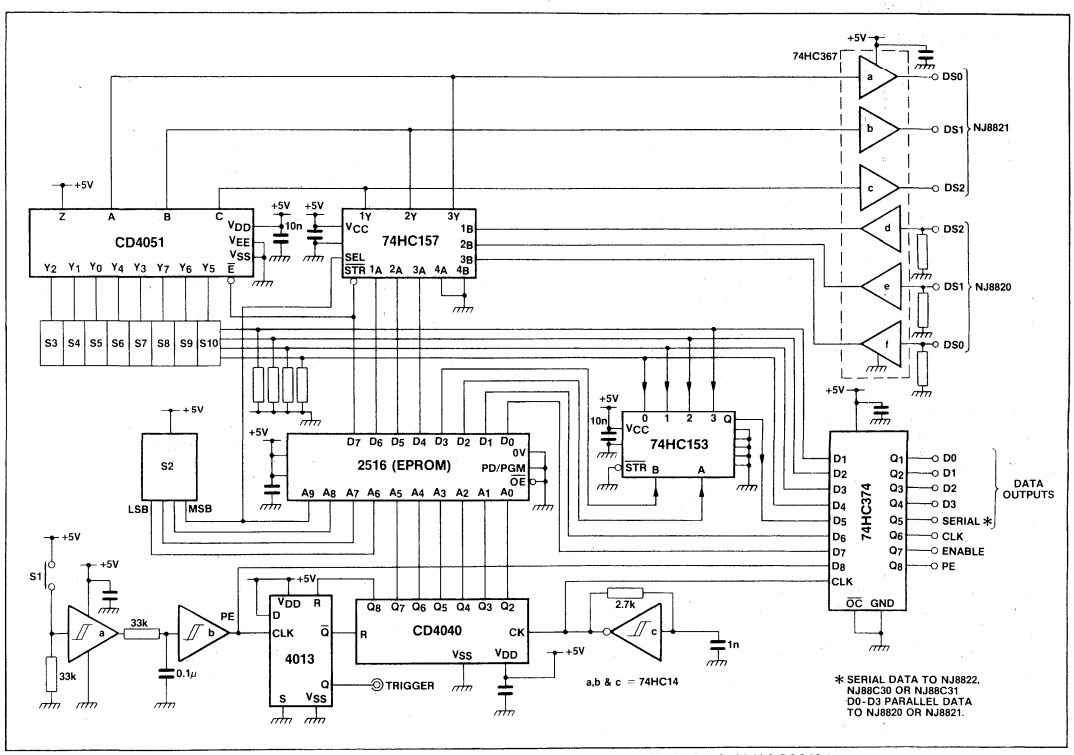


Fig.1 Universal programmer for NJ8820/21/22/23/24/C25 & NJ88C30/31

Switch	2				1				0				4			
	MSB			LSB	MSB			LSB	MSB			LSB	MSB			LSB
NJ8820/1/2/3/4	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	-	-	-	A6	A5	A4
NJ88C30/31	-	R2	R1	R0	-	-	-	-	-	-	-	-	-	-	-	-

Switch	3				7				6				5			
	MSB			LSB	MSB			LSB	MSB			LSB	MSB			LSB
NJ8820/1/2/3/4	A3	A2	A1	A0	-	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
NJ88C30/31	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

NOTE:

When entering the data for the NJ8820 series of devices it is necessary to multiply the M divide ratio by 4 prior to conversion to hexadecimal. It is necessary to divide the R divide ratio by 2 prior to conversion to hexadecimal to take into account the fixed divide by 2 in the reference chain.

Table 1 Switch settings for various synthesiser types

A_9	A_8	A_7	A_6	Synthesiser Type
0	0	0	0	**NJ8821/3**
0	0	0	1	**NJ8822/4 (17 Bits)**
0	0	1	0	**NJ8822/4 (28 Bits)**
0	0	1	1	**NJ88C30/31**
0	1	0	0	**NJ88C25 (19 Bits)**
0	1	0	1	**NJ88C25 (30 Bits)**
1	0	0	0	**NJ8820**

Table 2 Eprom addressing

A5 to A0 is determined by the 4040 counter outputs Q7-Q2 to give 64 timing slots per synthesiser type. Start addresses A9 to A6 are set by switch S2.

Table 4 is an example of the eprom data for the NJ8822. The start address 0040 is set by hex switch S2.

It can be seen how the data generates the clock and enable signals, the control signals for the parallel to serial conversion in the 74HC153 Mux and the selection of the switches S3-S10. In this case S6 and S7 are selected, these contain the data for the 'A' counter which is the first to be sent to the device.

A complete memory map of the eprom is given in Table 5.

D7	0	DS0-DS2 and Data outputs enabled
	1	DS0-DS2 and Data outputs disabled

D6	D5	D4	Switch selected
0	0	0	S5
0	0	1	S4
0	1	0	S3 LHS switch
0	1	1	S7
1	0	0	S6
1	0	1	S10 RHS switch
1	1	0	S9
1	1	1	S8

D3	D2	Serial data
0	0	MSB D3
0	1	D2
1	0	D1
1	1	LSB D0

D1	Clock O/P
D0	Enable O/P

Table 3 Eprom data

			Switch Select			Parallel to Serial		CK	EN
Address	**Data**	**O/P Enable**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
040	80	1	0	0	0	0	0	0	0
041	02	0	0	0	0	0	0	1	1
042	47	0	1	0	0	0	1	1	1
043	45	0	1	0	0	0	1	0	1
044	4B	0	1	0	0	1	0	1	1
045	49	0	1	0	0	1	0	0	1
046	4F	0	1	0	0	1	1	1	1
047	4D	0	1	0	0	1	1	0	1
048	33	0	0	1	1	0	0	1	1
049	31	0	0	1	1	0	0	0	1
04A	37	0	0	1	1	0	1	1	1
04B	35	0	0	1	1	0	1	0	1
04C	3B	0	0	1	1	1	0	1	1
04D	39	0	0	1	1	1	0	0	1
04E	3F	0	0	1	1	1	1	1	1
04F	3D	0	0	1	1	1	1	0	1

Table 4 Example of eprom data organization

																	Eprom Start Addr (Hex)	Switch No.
NJ8821/3	80	00	01	01	00	10	11	11	10	20	21	21	20	30	31	31	00	0
	30	40	41	41	40	50	51	51	50	60	61	61	60	70	71	71		
	70	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
NJ8822/4 17 Bit	80	02	47	45	4B	49	4F	4D	33	31	37	35	3B	39	3F	3D	40	1
	23	21	27	25	2B	29	2F	2D	13	11	17	15	1B	19	1F	1D		
	03	01	07	01	07	02	80	80	80	80	80	80	80	80	80	80		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
NJ8822/4 28 Bit	80	02	47	45	4B	49	4F	4D	33	31	37	35	3B	39	3F	3D	80	2
	23	21	27	25	2B	29	2F	2D	13	11	17	15	1B	19	1F	1D		
	03	01	07	05	77	75	7B	79	7F	7D	63	61	67	65	6B	69		
	6F	6D	53	51	57	55	5B	59	5F	5D	5F	5E	80	80	80	80		
NJ88C30/31	80	26	24	2A	28	2E	2C	32	30	36	34	3A	38	3E	3C	72	C0	3
	70	76	74	7A	78	7E	7C	62	60	66	64	6A	68	6E	6C	52		
	50	56	54	5A	58	5E	5C	5D	80	80	80	80	80	80	80	80		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
NJ88C25 19 Bit	80	02	47	45	4B	49	4F	4D	33	31	37	35	3B	39	3F	3D	100	4
	23	21	27	25	2B	29	2F	2D	13	11	17	15	1B	19	1F	1D		
	03	01	07	05	0B	09	0F	0D	8F	8D	8F	8E	80	80	80	80		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
NJ88C25 30 Bits	80	02	47	45	4B	49	4F	4D	33	31	37	35	3B	39	3F	3D	140	5
	23	21	27	25	2B	29	2F	2D	13	11	17	15	1B	19	1F	1D		
	03	01	07	05	0B	09	0F	0D	77	75	7B	79	7F	7D	63	61		
	67	65	6B	69	6F	6D	53	51	57	55	5B	59	5F	5D	5F	5E		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		6
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		7
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80	80		
NJ8820	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	200	8
	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		
	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00		

Table 5 Eprom memory map

Using the SP8835 in 3.5GHz Synthesisers

Until recently, prescalers have only been available (at reasonable consumer prices) for frequencies up to about 1GHz. Now, with the rapid improvement of silicon technology, Plessey Semiconductors has developed a range of dividers for frequencies for up to 3.5GHz.

The following application note explains how one of these devices can easily be used with two standard integrated synthesisers. The first example is of a 3.5GHz synthesiser using the SP8835 ÷ 4 (3.5GHz) together with the SP5000 (1GHz synthesiser chip). The second example is again a 3.5GHz synthesiser, but using the SP8835 ÷ 4 with an SP8704 ÷ 128/9 (dual modulus divider 1GHz) and the NJ8820. This second example can be programmed to give a smaller frequency step size than the first example, but requires more components.

High speed dividers are primarily used in frequency synthesisers, either phase locked loops or frequency locked loops. Synthesisers incorporate a voltage controlled oscillator which is controlled via a feedback network so that it oscillates at a predetermined frequency. In most cases, this synthesised frequency can be altered (by external programming) to tune the oscillator over a range of frequencies (band). The prescaler is used in such a system to reduce the oscillator's frequency to one that can be compared with a standard known reference frequency (usually obtained from a crystal oscillator and divider). This frequency comparison can be made in several ways, for example a phase comparison using a phase detector (PLL) or a frequency comparison using a frequency counter (μPC) in a frequency locked loop.

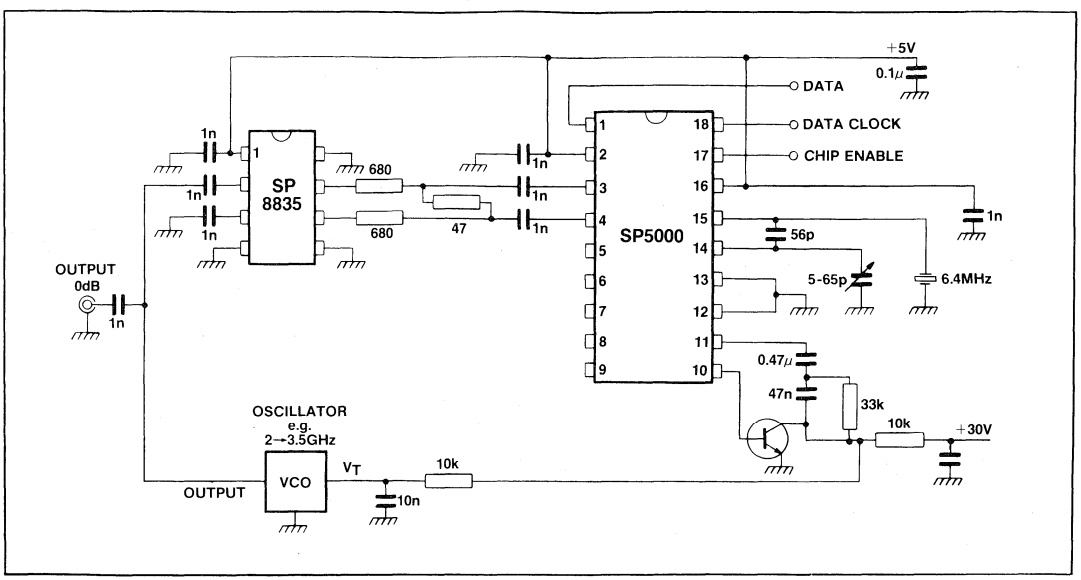


Fig.1 SP8835 and SP5000 - 3.5GHz synthesiser

3.5GHz SYNTHESISER USING SP8835 AND SP5000

The SP8835 (÷4) interfaces very easily with the SP5000 (see Fig.1). The only interface circuit used is an attenuator so that the output from the SP8835 does not overload the input of the SP5000 (the SP5000 has very good sensitivity for TV applications). The rest of this application circuit is identical to the standard application circuits of the two devices as shown in their relevant data sheets. With a 4MHz crystal used in the reference oscillator, a synthesiser can be programmed to synthesise frequencies up to 3.5GHz with a minimum frequency step size of 500kHz. The range of frequencies over which the synthesiser will synthesise is determined by the voltage controlled oscillator used.

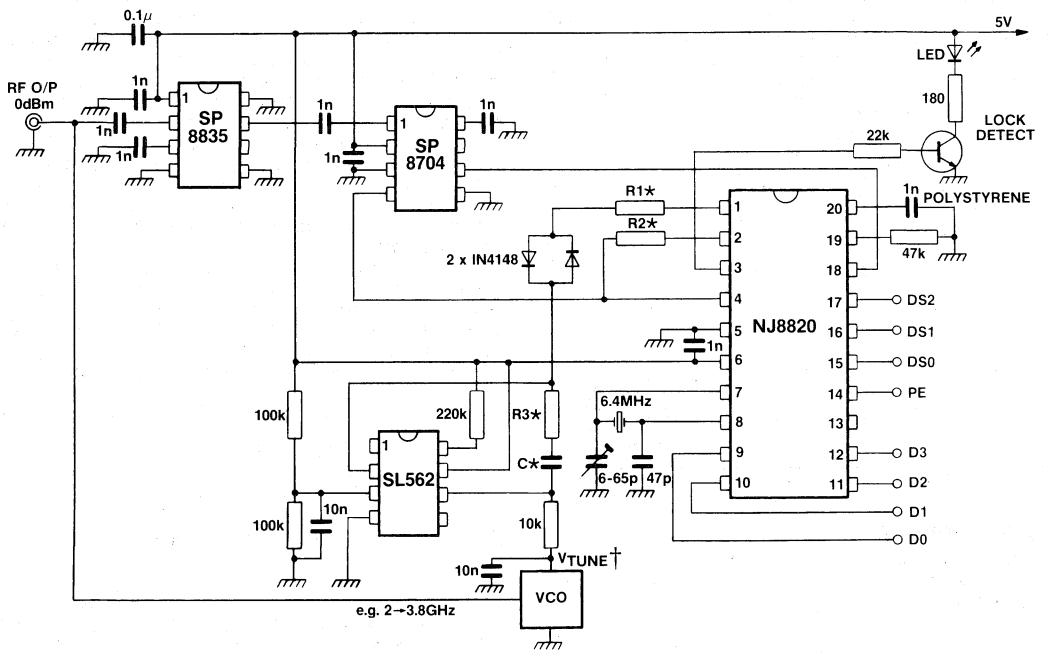
When laying out the PCB for this application, a board with an earth plane should be used, all decoupling capacitors should be placed as near as possible to the devices and all high frequency links should be 50Ω track.

3.5GHz SYNTHESISER USING SP8835, SP8704, NJ8820 AND SL562

If the SP8835 is used in conjunction with an SP8704 (÷128/129) and an NJ8820 with loop filter amplifier (SL562), a synthesiser with a minimum frequency step size of 100kHz can be constructed (using a 6.4MHz crystal, see Fig.2). The devices interface to each other very easily as shown in the circuit diagram. No attenuation or amplfication is needed to match input and output levels. The only section of the synthesiser that needs careful design is the loop filter which is dependent on the type of oscillator used and the phase noise requirements. With a small frequency step size of 100kHz, which is a very small percentage of the synthesised frequency, a low loop bandwidth is required for adequate sideband suppression. A 200Hz loop filter gives adequate sideband suppression for a 3.5GHz synthesiser for use in a satellite TV reception system (C band direct conversion). The loop filter component calculations are explained in the 'Radio Synthesiser Circuits' applcation booklet.

PCB layout techniques are the same as the previous example.

These are just a few examples of applications for high speed dividers. They can very easily be used in conjunction with a larger modulus, lower frequency divider to produce a frequency low enough for a microprocessor to be able to count and can therefore be used in a frequency locked loop. This is useful if a microprocessor is already used in the system.



NOTES

† V_{TUNE} approximately 0 to 5V. If a greater voltage range is required, the supply to the SL562 may be increased to a maximum of 20V. Pin 3 of the SL562 should be maintained at 2.5V.

* Values for the loop filter components R1, R2, R3 and C can be calculated as described in the Loop Filter Design application note.

Fig.2 3.5GHz synthesiser using SP8835, SP8703, NJ8820 and SL562

The SP2001 Direct Frequency Synthesiser AN68

Historically, frequency synthesis has been implemented either by the use of non-coherent mixing or coherent phase locked loop (PLL) techniques. The advent of high speed circuitry capable of digital to analog conversion as well as high speed digital functions, has made it possible to implement a different form of synthesis.

In the Direct Frequency Synthesiser (DFS), the production of the output frequency is achieved using the block diagram of Fig 1. Here a phase accumulator provides the address to a ROM in which the desired wave shape is stored, and the output of the ROM is fed to the DAC to provide the derived output waveform.

The address to the ROM is produced by adding a binary number, K, to the content of the N bit accumulator, and the resulting sum is transferred to the latch at each reference clock cycle. Each time the adder overflows a new cycle is started, and the rate at which this occurs is the output frequency, which is set by the programed number K.

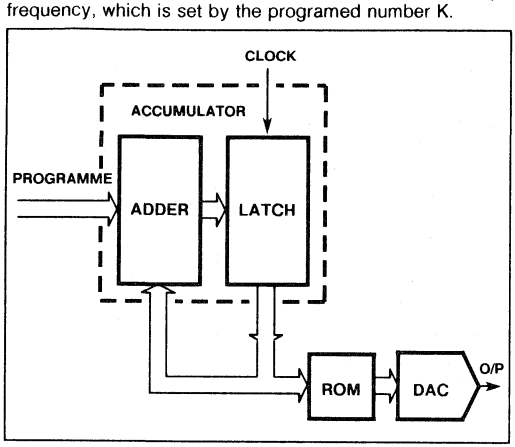


Fig.1 Direct frequency synthesiser

OUTPUT FREQUENCY

The output frequency is determined by the numbers N and K (number of bits in the accumulator and the programed number).

$$f_{OUT} = \frac{Kf_C}{2^N}$$

where f_C is the clock frequency.

The minimum output frequency is produced when K = 1 i.e.:

$$f_{OUT} = \frac{f_C}{2^N}$$

The smallest increase is from K = 1 to K = 2 i.e.:

$$\frac{f_C}{2^N} \text{ to } \frac{2f_C}{2^N} \text{ and is thus } \frac{f_C}{2^N}$$

The step size is thus fixed by N and so, for a 16-bit accumulator, is

$$\frac{f_C}{65536}$$

The internal ROM is programed with a half cosine wave so that the amount of ROM required is minimised (128x8). The ROM output is an 8-bit word for driving the DAC .

SPURIOUS OUTPUTS

In order to minimise spurious outputs, it is important that the DAC settles as quickly as possible: in this respect, a 10-bit DAC settling to 9 bits in a given time is better than a 12-bit DAC settling to 8 bits in the same time. Thus the use of a very fast DAC is indicated, and the GPS SP98608 8bit, 2ns to ½ LSB DAC is the best practical current realisation

Spurious outputs are also dependent upon the clock and output frequencies. Because the phase quantisation is truncated by the use of less than N bits of ROM and DAC, a set of spurious PM sidebands exists at a carrier-to-sideband spacing dependent upon the values of K, N and f_C.

The DAC settling time is the primary factor in defining the spurious output levels in the SP2001 demonstration board - at least at high frequencies. This may be seen by the improvement at low output frequencies, where oversampling is taking place, and in the improvement noted with lower clock frequencies.

Frequency accuracy is determined by the accuracy of the external clock, as in all synthesisers. The PLL synthesiser phase noise is dominated by reference frequency phase noise only within the loop bandwidth, and this constraint does not apply to the DFS. Thus the phase noise output of the DFS is derived from 3 sources:-

(i) Phase noise of the reference clock. This is reduced by

$$20 \log_{10}\left[\frac{f_C}{2^N}\right] K \text{ at any offset}$$

(ii) Phase jitter introduced within the digital circuitry
(iii) Noise introduced by the DAC

Measurements indicate that at 10MHz output and 326.78MHz clock frequency, the phase noise at a 19kHz separation is of the order of -133dBc/Hz, which is within 3dB of the clock phase noise.

USING THE SP2001

In order to minimise spurious outputs, it is advisable that the inputs to the DAC are time-coincident. Where a DAC with latched inputs is used, such as the GPS SP98608, this requirement is slightly eased. Good ECL layout practices should be followed, with minimum lead length bypasses.

The circuit diagram of a suitable PC board is shown in Fig 2. Because of the short frequency change time exhibited by the SP2001, it is important to ensure that the programming number is presented as a parallel data word with no time skew between bits if the production of a spurious frequency during the frequency change is to be avoided. As stated earlier the spurious output level is related both to the absolute output frequency and the particular values of N and K in use at the time, as well as the clock frequency. The spurious outputs are improved at 3dB/octave reduction in frequency as the settling time of the DAC becomes less of a contributing factor.

THE SP2001 DEMONSTRATION BOARD

This board, the circuit of which is shown in Fig. 5, uses PCB mounted switches for programming. It is fed with a 327.680MHz clock and the PCB switches provide binary selection e.g:

LSB	gives 5kHz steps
LSB + 1	gives 10kHz steps
LSB + 2	gives 20kHz steps

Thus, to program an output frequency, the program number is:

$$\frac{f_{OUT}}{5kHz} \text{ expressed in binary}$$

The board requires supplies of -5.2V and -2V: The clock input level required is +5dBm

CIRCUIT DESCRIPTION

The clock input to the SP2001 is fed through internal signal conditioning circuitry to provide suitable internal ECL swings.

The accumulator input is derived from the parallel ECL programming lines, for which, for the purpose of the demonstration board, are driven by the programming switches, when the switches are open, the particular bit is programmed as a '1'.

The output of the SP2001 ROM is fed to an SP98608 8-bit, high speed, DAC. The output from this is an approximate sine wave at the programed frequency. The output level is at about +5dBm into 50Ω, while the output impedance, being a current source, is determined by the value of output resistance and in this case is 50Ω.

By-passing of the supply and DAC internal references are by means of a combination of a chip ceramic and tantalum bead capacitor while the pull-down resistors are single in-line resistor networks.

The R set resistor, which programs the output current of the DAC, may be varied to provide a measure of output level control. $V_{OUT} = 128/R_{SET}$ V p-p.

PERFORMANCE

As in any synthesiser, frequency accuracy is a function of the reference frequency accuracy, as is phase noise. However, unlike the PLL synthesiser, where reference frequency noise is attenuated outside the loop bandwidth, no filtering action of this sort is obtained in the direct waveform synthesiser. Measurements have been made on the SP2001 demonstration board suggesting phase noise levels of -130dBc/Hz at 10kHz, but this was within 1dB of the phase noise density of the synthesised signal generator used as the clock.

Spurious output frequencies may be predicted, although the levels are more indeterminate. The spacing of such spurious outputs from the carrier is a variable with output frequency, and can be very close: asymmetry in the sidebands is probably caused by intermodulation of higher order harmonics in the DAC producing PM of these sidebands. It is frequently considered that an output frequency programmed by 2^{N-1} will produce poor spurious performance.

At 20.475MHz however, spurious outputs are typically of the order of -50dB. The channel change time is approximately 17ns.

It is possible to use the SP2001 in conjunction with a PLL to produce fast steps within a limited frequency range, in the manner of a conventional two-loop synthesiser.

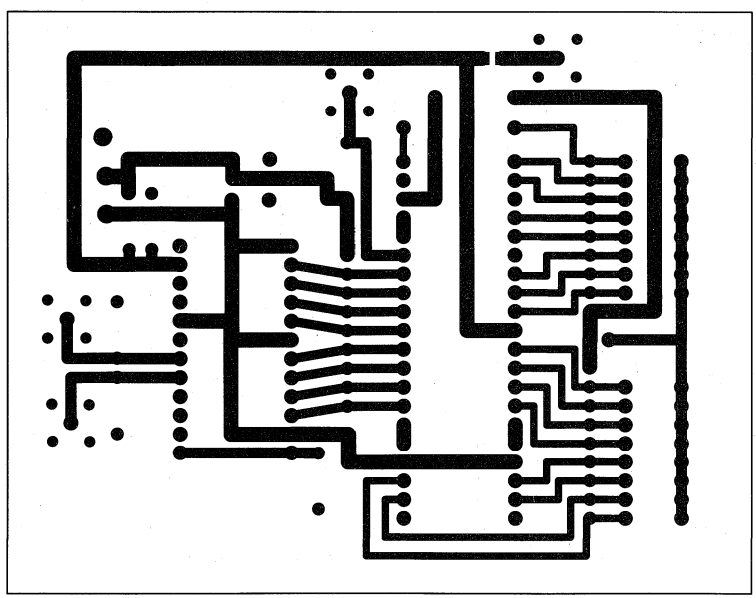


Fig.2 SP2001 demonstration board track layout

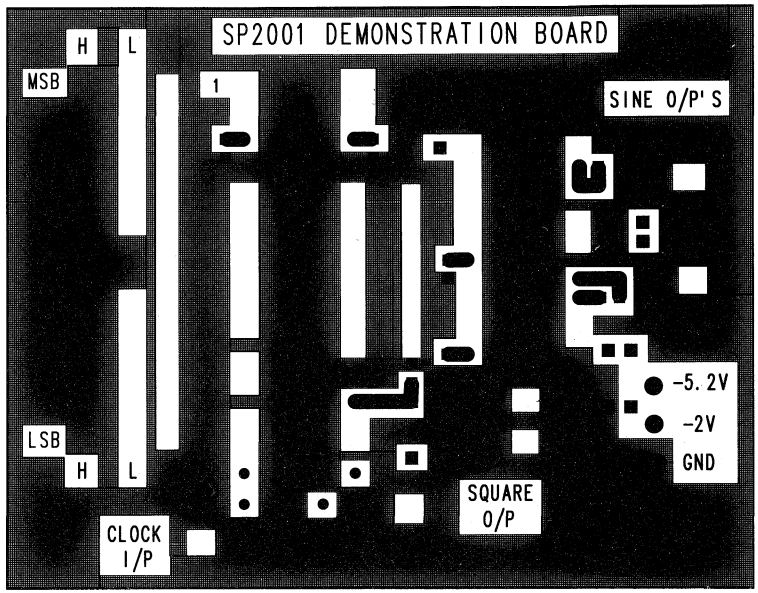


Fig.3 SP2001 demonstration board ground plane

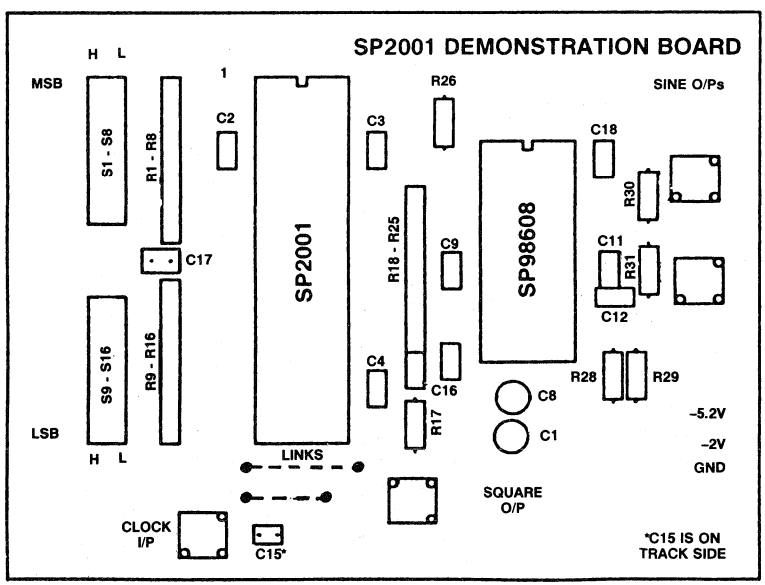


Fig.4 SP2001 demonstration board component layout

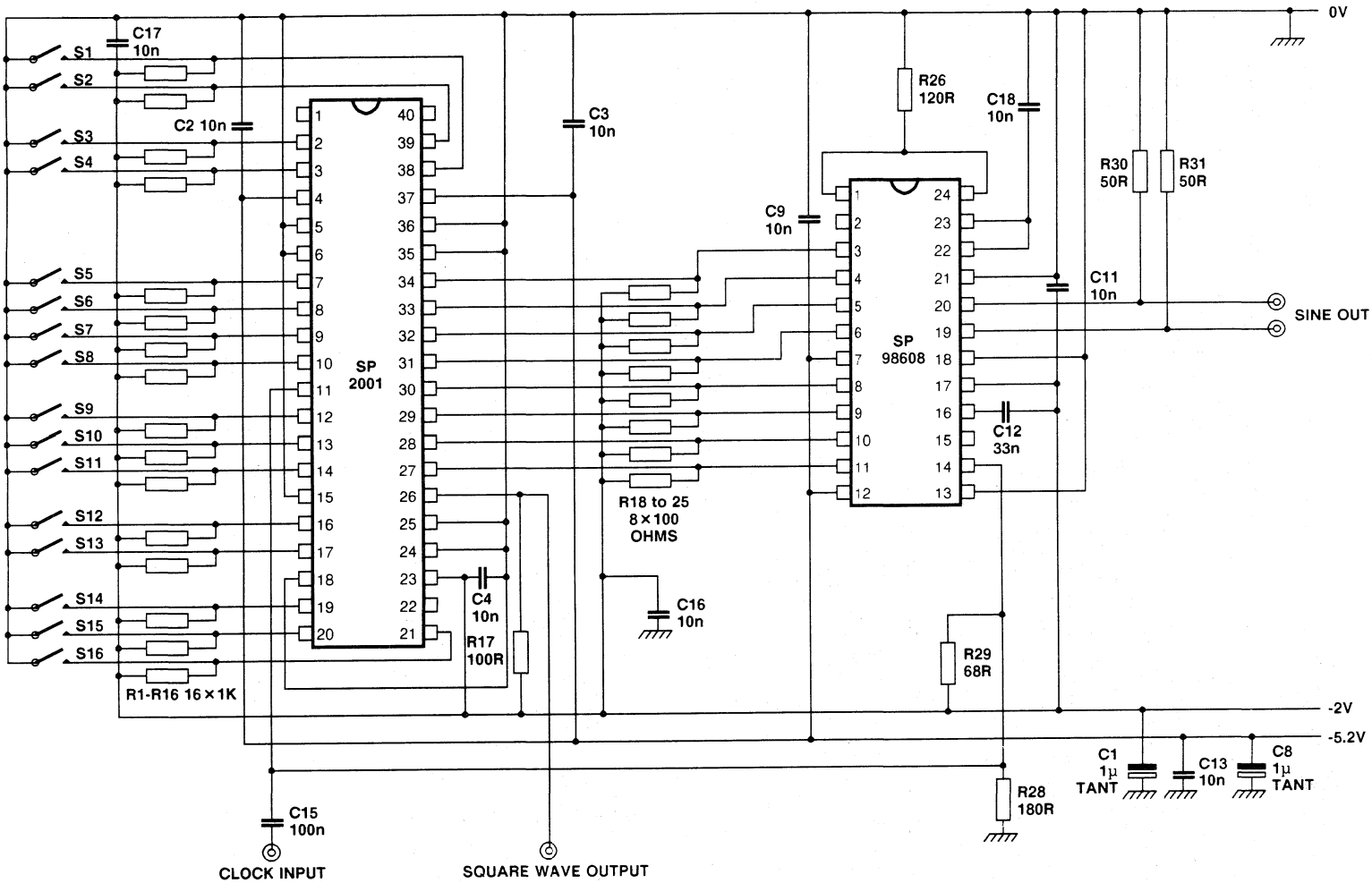


Fig.5 SP2001 demonstration board circuit diagram

Thermal Design

The temperature of any semiconductor device has an important effect upon its long term reliability. For this reason, it is important to minimise the chip temperature; and in any case, the maximum junction temperature should not be exceeded.

Electrical power dissipated in any device is a source of heat. How quickly this heat can be dissipated is directly related to the rise in chip temperature: if the heat can only escape slowly, then the chip temperature will rise further than if the heat can escape quickly. To use an electrical analogy: energy from a constant voltage source can be drawn much faster by using a low resistance load than by using a high resistance load.

The thermal resistance to the flow of heat from the semiconductor junction to the ambient temperature air surrounding the package is made up of several elements. These are the thermal resistance of the junction-to-case, case-to-heatsink and heatsink-to-ambient interfaces. Of course, where no heatsink is used, the case-to-ambient thermal resistance is used.

These thermal resistances may be represented as

$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$

where θ_{JA} is thermal resistance junction-to-ambient °C/W
θ_{JC} is thermal resistance junction-to-case °C/W
θ_{CH} is thermal resistance case-to-heatsink °C/W
θ_{HA} is thermal resistance heatsink-to-ambient °C/W

The temperature of the junction is also dependent upon the amount of power dissipated in the device — so the greater the power, the greater the temperature.

Just as Ohm's Law is applied in an electrical circuit, a similar relationship is applicable to heatsinks.

$T_j = T_{amb} + P_D (\theta_{JA})$,

where T_j = junction temperature
T_{amb} = ambient temperature
P_D = dissipated power

From this equation, junction temperature may be calculated, as in the following examples.

Example 1

An SP8785B is to be used at an ambient temperature of +50 °C. θ_{JA} for the DG16 package with a chip of approximately 1mm sq is 110 °C/W; from the datasheet, P_D max = 598mW and T_j max = 175 °C.

$T_j = T_{amb} + P_D \theta_{JA}$
$= 50 + (0.598 \times 110)$
$= +11.8$ °C

Where operation in a higher ambient temperature is necessary, the maximum junction temperature can easily be exceeded unless suitable measures are taken:

Example 2

An SP8785A is to be used at an ambient temperature of +120 °C. Again, θ_{JA} = 110 °C/W, P_D max = 598mW.

$$T_j = 120 + (0.598 \times 110)$$
$$= +185.8\,°C$$

This clearly exceeds the maximum permissible junction temperature and therefore some means of decreasing the junction-to-ambient thermal resistance is required.

As stated earlier, θ_{JA} is the sum of the individual thermal resistances; of these, θ_{JC} is fixed by the design of device and package and so only the case-to-ambient thermal resistance, θ_{CA}, can be reduced.

If θ_{CA}, and therefore θ_{JA}, is reduced by the use of a suitable heatsink, then the maximum T_{amb} can be increased:

Example 3

Assume that an IERC LIC14A2U dissipator and DC000080B retainer are used. This device is rated as providing a θ_{JA} of 55 °C/W for the DG16 package. Using this heatsink with the SP8785A operated as in Example 2 would result in a junction temperature given by:

$$T_j = 120 + (0.598 \times 55)$$
$$= +153\,°C$$

Nevertheless, it should be noted that these calculations are not necessarily exact. This is because factors such as θ_{JC} may vary from device type to device type, and the efficacy of the heatsink may vary according to the air movement in the equipment.

In addition, the assumption has been made that chip temperature and junction temperature are the same thing. This is not strictly so, as not only can hot spots occur on the chip, but the thermal conductivity of silicon is a variable with temperature, and thus the θ_{JC} is in fact a function of chip temperature. Nevertheless, the method outlined above is a practical method which will give adequate answers for the design of equipment.

It is possible to improve the dissipating capability of the package by the use of heat dissipating bars under the package, and various proprietary items exist for this purpose.

Under certain circumstances, forced air cooling can become necessary, and although the simple approach outlined above is useful, more factors must be taken into account.

SL3522 Applications and Characteristic Data

The following application note provides information to assist users achieve the full performance from the SL3522 in their applications.

Information detailed includes:-

1) A full description of the device architecture and operation including a detailed block diagram. (Fig. 6.)
2) Advisory application notes regarding board layout.
3) A scaled drawing of the pad positions of the SL3522 die for hybrid applications. (Fig. 7.)
4) Typical Log/Lin characteristic of detected level versus RF input level including differential linearity error characteristic. (Figs. 2 & 3.)
5) Typical input impedance characteristic on Smith chart. (Fig. 5.)
6) Typical characteristic of peak to peak differential phase variation across -65dBm to +10dBm input level at various frequencies between 50MHz and 500MHz. (Fig. 4.)

PRODUCT DESCRIPTION

The SL3522 is a complete monolithic successive - detection Log/Limiting amplifier which can operate over an input frequency range of 100MHz to 650MHz. Producing a Log/Lin characteristic for signals between -68dBm to +7dBm; the log amplifier can provide an accuracy of ±1dB.

It consists of 6 gain stages, 7 detector stages, a limiting RF output buffer and a video output amplifier. The power supply connections to each section are isolated from each other, to aid stability. Each of the gain stages and detector stages has approximately 12dB of gain, and a significant amount of on-chip RF decoupling also to aid stability.

The limiting RF output buffer provides a balanced limited output level of 0dBm on each RF output line (pins 9 & 10), for input signal levels in excess of -65dBm (when input applied to pins 27 & 28). It can be isolated from the other parts of the log/limiting amplifier, by disconnecting the RF Output Buffer GND (pin 8) from 0V. This feature will aid stability in applications which do not require a limited RF output.

The video amplifier provides a positive-going output signal proportional to the log of the amplitude of an RF input applied to pins 27 & 28. The gain and offset of the video amplifier can be adjusted by means of 3 resistors - R_G, R_T and R_O which are connected to the Gain Adjust pin (pin 19), Trim Ref (pin 18) and Offset adjust (pin 17) respectively. With R_T set to 1.5kΩ, R_G can be set to any value between 1kΩ and 2.2kΩ to achieve a range in log slope of ±20%, centred on 20mV/dB. Similarly R_O can be set to any value between 1K.Ω and 2.2kΩ and achieve a range in offset between -0.5V and +1.0V.

The RF input pins (pins 27 and 28) have a 50Ω terminating resistor connected between them on-chip. These in turn are capacitively coupled to the I/P gain stage. The RF input has provision to be driven either balanced or single ended.

The SL3522 consumes approximately 1.1 watts of power when all parts of the circuit are powered up from a ±5.0V power supply. As the circuit uses a class A based differential architecture the power consumption of the RF gain stages, detectors and RF output buffers will be independent of input signal level. However, the Video Output (pin 13) is single ended, and the power consumption of the video amplifier will vary with RF input signal level on pins 27 and 28.

If the SL3522 is operated with the RF output buffer disabled (i.e. RF output buffer GND (Pin 8) left floating,) the power consumption will drop to approximately 0.95W, when all other parts of the circuit are powered up from a ±5.0V power supply.

APPLICATION NOTES

Refer to Application circuit in Fig. 1.

RF Output Buffer

The SL3522 device contains 70dB of broadband RF gain with 3dB bandwidth of 450MHz. When the RF OUTPUT buffer is powered up, this gain can be realised at the RF O/P +/- pins (9 & 10). Operating the device with the RF output buffer powered down removes the RF output and results in a Log Amplifier with enhanced stability and reduced power consumption.

The RF O/P GND pin (8) is the positive supply to the RF output buffer. If this pin is left open circuit the RF output amplifier powers down and saves 30mA power consumption from the V_{EE} supply.

The RF O/P V_{EE} pin (11) should **always** be connected to the V_{EE} supply rail even if the RF output buffer is powered down, by operating with pin 8 left open-circuit.

If the RF O/P buffer is to be used, care is required in layout to ensure stability.

Application Suggestions

The following precautions should be observed when configuring the device for application :-

a) The device should be mounted on a ground plane, and all supply decoupling should be RF-quality chip capacitors. The leads to the decoupling capacitors should be kept as short as possible.

b) The RF V_{EE} pins (3, 5, 7, 20, 22, 24 and 26) should connect to a low impedance copper plane. A two layer PCB should help to achieve this.

c) The load current at the video output pin should be returned to the VIDEO O/P V_{CC} pin (14) via a 10nF capacitor connected to the return line of the video load, avoiding any common impedance path.

d) The VIDEO O/P V_{EE} pin (12) should be decoupled DIRECTLY to the VIDEO O/P V_{CC} pin (14), with a 10nF capacitor.

e) The unscreened lead length at the RF input should be kept to a bare minimum. If being driven single ended, the RF input return line should be isolated from, but kept in very close proximity to the ground plane and connected to the ground plane via a 50Ω chip or bead resistor at pin 28. The RF input can also be driven differentially.

e) If the device is operated with the RF OUTPUT BUFFER powered up then care must be taken to present both the RF O/P- pin (9) and RF O/P+ pin (10) with matched loads. Each pin should ideally be loaded with a 50Ω terminated transmission line. The device stability is very sensitive to imbalance at the output. Driving highly reactive SWR loads is not recommended for stability reasons.

g) Although the RF O/P ± pins (10 & 9) have DC blocking capacitors shown, they may be operated with a DC load to ground. However, a DC offset of approx -400mV will exist on each RF O/P pin. It will NOT be possible to power-down the output buffer under these conditions.

h) The RF input is isolated from the input amplifier by two series on-chip capacitors. The device includes an on chip 50Ω termination resistor which is connected directly across the RF input pins (27 & 28).

Gain and Offset Trimming

Gain and offset trimming are unilaterally independent. Adjustment of gain has an effect on the offset, but adjustment of offset does **not** affect the gain.

The gain and offset control is achieved by adjusting R_G and R_O respectively. The control is dependent upon their difference from the trim - reference resistor R_T. Differing temperature coefficients in **all** of these resistors will lead to variations in gain and offset over the temperature range. It is recommended that resistors of identical type be used, to maintain operating stability over temperature.

Video Performance

In order to achieve the specified video transient performance, it is important to ensure that the resistor connected to the trim - reference pin (18), has a parasitic capacitance **less** than 5pF. This resistor should have a nominal value of 1.5kΩ. Additionally, the load must be **not** less than 200Ω resistive with **not** more than 20pF of shunt capacity.

Because of the difficulty of making a valid fall-time measurement, this parameter is unspecified. It is that time corresponding to a 30MHz bandwidth system incorporating critical damping.

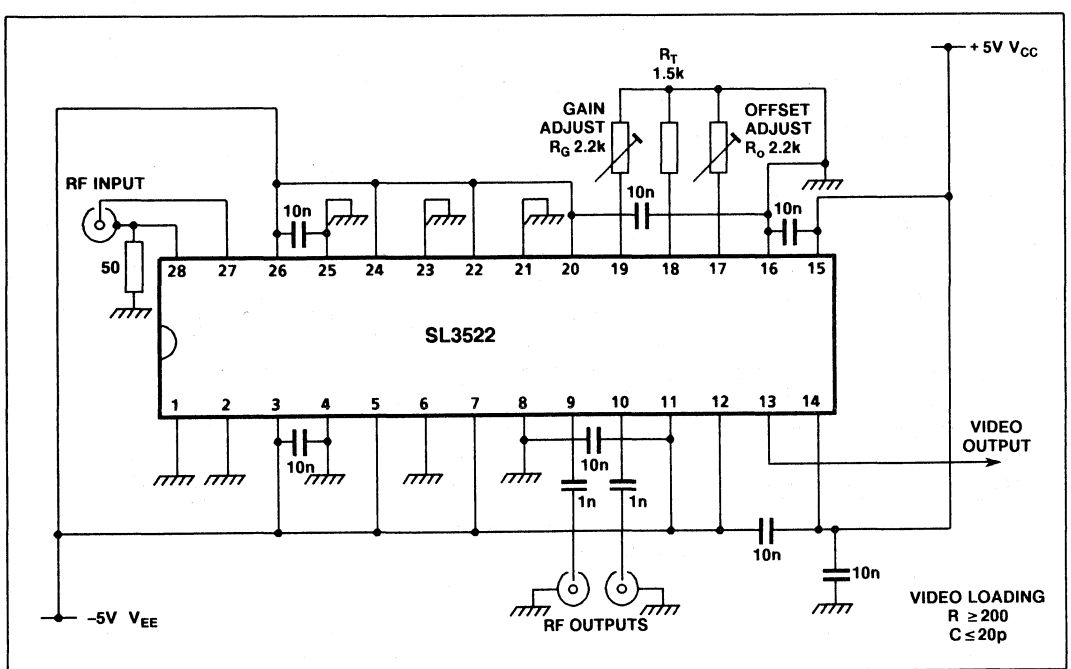


Fig.1 Test and applications circuit

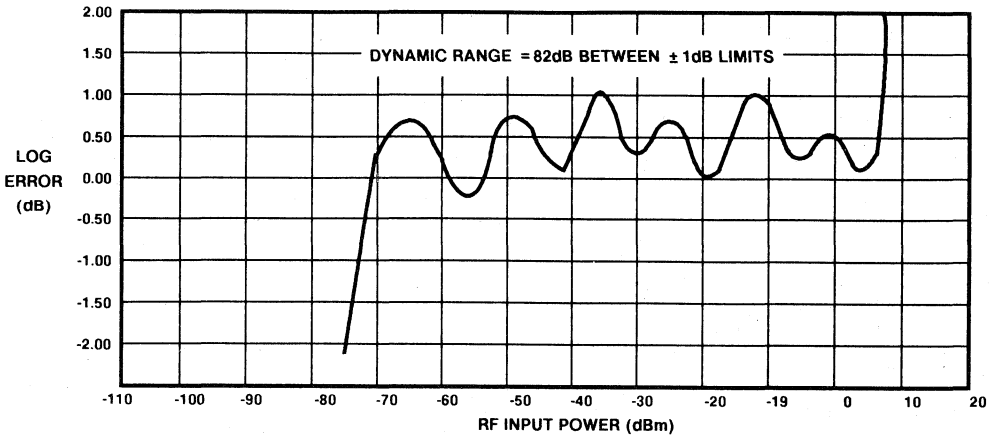


Fig. 2. Typical Differential Log/Linear

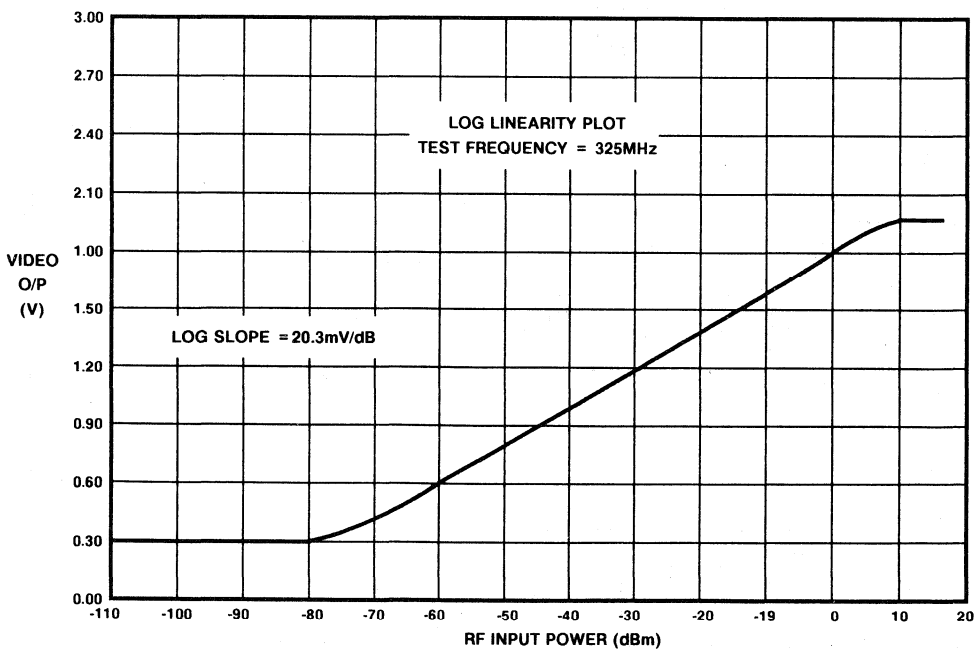


Fig. 3. Typical Log/Linear Characteristic

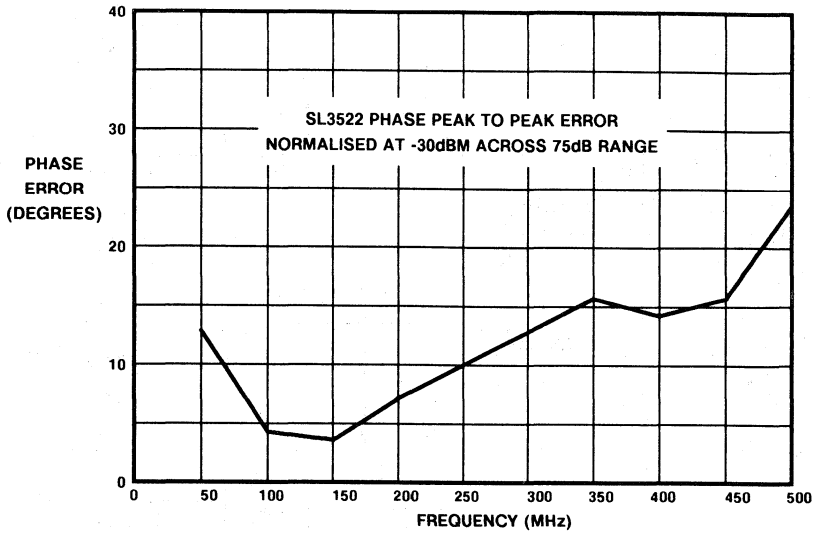


Fig. 4. Typical Peak to Peak Phase Variation v. IF Frequency
(Input power between -65dBm and +10dBm normalised to phase at -30dBm)

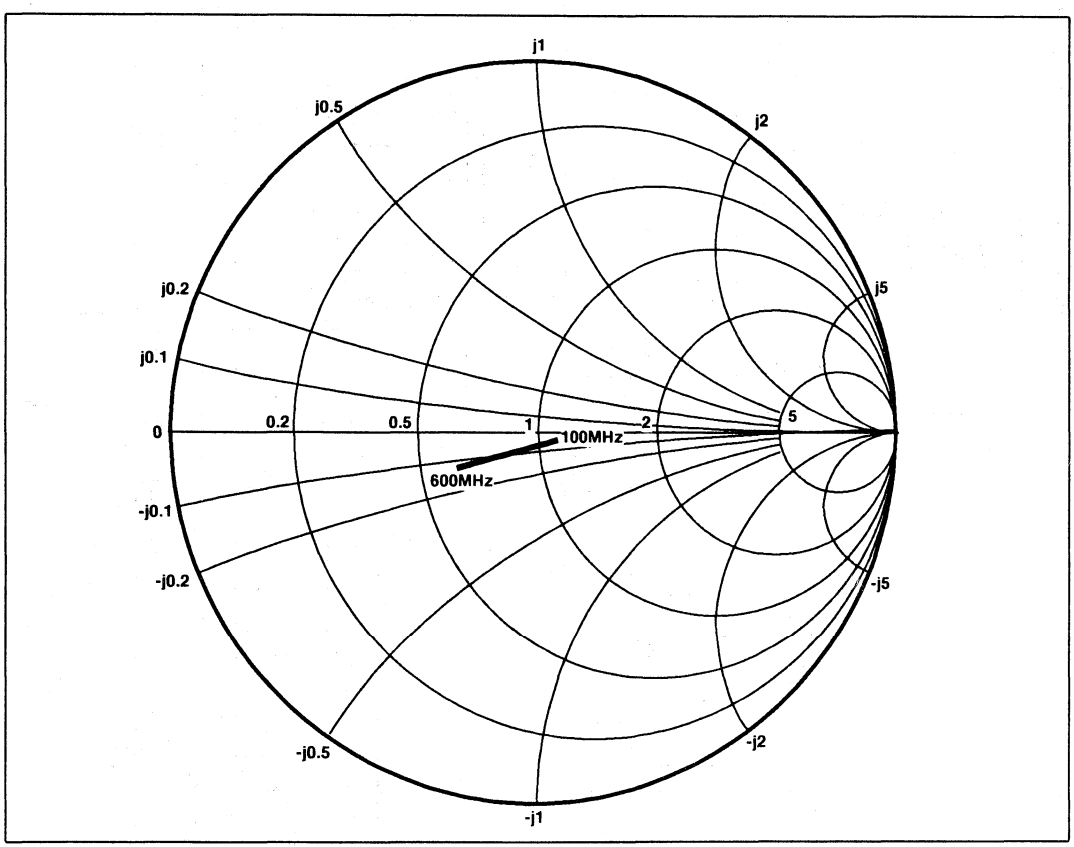


Fig.5. SL3522 Typical Impedance Normalised to 50Ω. -20dBm I/P Level

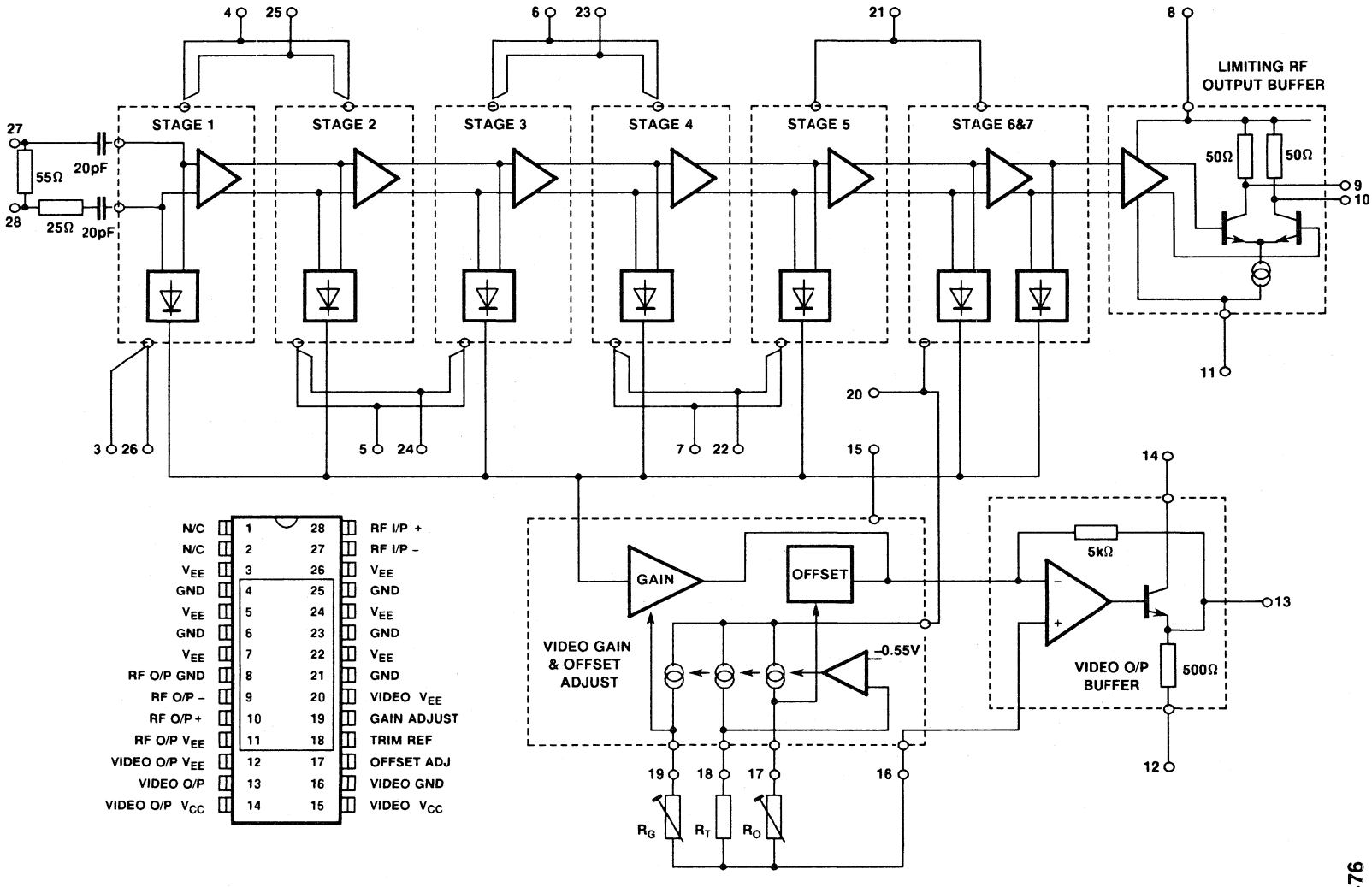
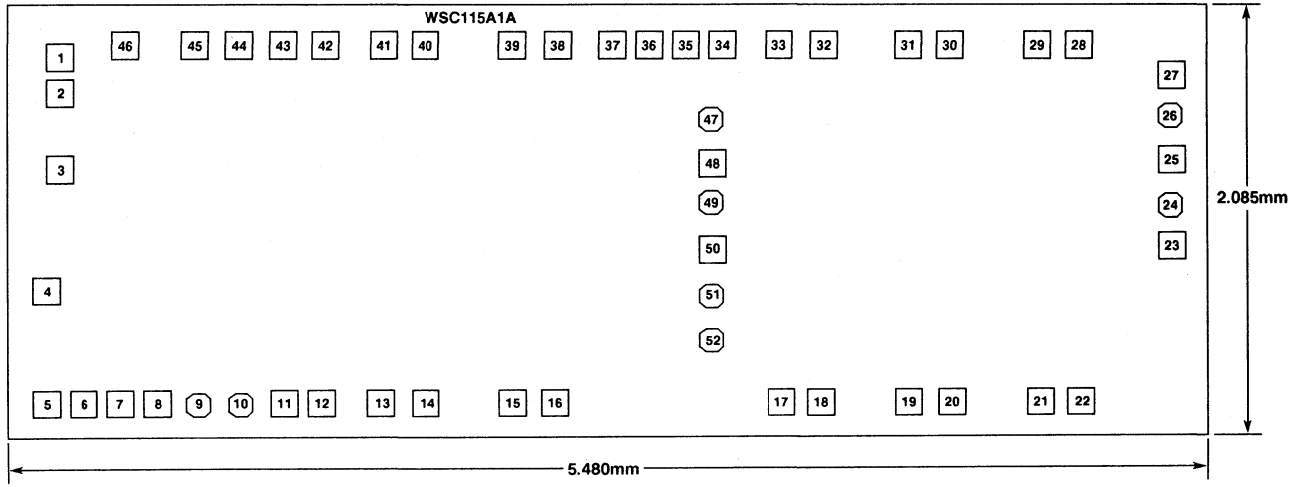


Fig. 6. SL3522 Schematic Diagram



TO SCALE

Terminals ((x) denotes MC package pin number)							
1	VIDEO O/P (13)	15	V_{EE} 4A (22)	29	GND 1B (4)	43	RF O/P – (9)
2	VIDEO O/P V_{CC} (14)	16	GND 4A (23)	30	GND 2B (4)	44	RF O/P + (10)
3	GAIN V_{CC} (15)	17	GND 3A (23)	31	V_{EE} 2A (5)	45	RF BUF O/P V_{EE} (11)
4	VIDEO GND (16)	18	V_{EE} 3A (24)	32	V_{EE} 3A (5)	46	VIDEO O/P V_{EE} (12)
5	OFFSET ADJ (17)	19	V_{EE} 2A (24)	33	GND 3B (6)	47	TEST POINT
6	TRIM REF (18)	20	GND 2A (25)	34	TEST POINT	48	TEST POINT
7	GAIN ADJ (19)	21	GND 1A (25)	35	TEST POINT	49	TEST POINT
8	GAIN V_{EE} (20)	22	V_{EE} 1A (26)	36	TEST POINT	50	TEST POINT
9	TEST POINT	23	TEST POINT	37	TEST POINT	51	TEST POINT
10	TEST POINT	24	RF I/P SIGNAL (27)	38	GND 4B (6)	52	TEST POINT
11	V_{EE} 6A (20)	25	TEST POINT	39	V_{EE} 4B (7)		
12	GND 6A (21)	26	RF I/P RETURN (28)	40	V_{EE} 5B (7)		
13	GND 5A (21)	27	TEST POINT	41	RF BUF O/P GND (8)		
14	V_{EE} 5A (22)	28	V_{EE} 1B (3)	42	RF BUF O/P GND (8)		

Fig. 7 SL3522 pad map for bare IC dice

NOTES
1. All pads with square cross-section = 120μm × 120μm
2. All pads with octagonal cross-section = 100μm × 100μm
3. Chip is passivated with polyimide

Section 5

MIL-STD-883C Class B

GEC Plessey Semiconductors is in conformance with the requirements of MIL-STD-883C Notice 11 paragraph 1.2.1 and can supply product requiring the use of this standard.

Approval has been issued by DGDQA against DEF-STD 05-21 (equivalent to AQAP1) and by NSI to BS9000. A number of detailed device approvals to BS9300 and BS9400 have been granted.

The following pages detail the manufacturing procedures required to conform to MIL-STD-883C Class B.

Screening procedures

MIL-STD-883C Class B

Stage/Operation	MIL-STD-883C Methods and Comments
Wafer processing	GPS process
Circuit probe test	To GPS probe test spec.
Chip separation	GPS process
Chip inspection and selection	Method 2010 condition B
Chip bond and inspect	GPS process
Wire bond and inspect	GPS process
Internal visual	Method 2010 condition B
Customer source inspection	Optional extra
Encapsulation	GPS process
Temperature cycling	Method 1010 condition C
Constant acceleration	Method 2001 condition E, Y1 only
Seal test	Method 1014
Visual inspection	For catastrophics, as Method 5004
Interim electrical test	To device spec. with read and record, as Method A
Burn-in test	Method 1015, 168 hours at 125°C
Post burn-in electrical	As interim electrical, as Method 5004
PDA calculations	Subgroup 1 min. 5% max.
Final electrical test	100% subgroups 1,2,3,4,5,6,7,8,9,10, and 11, as device spec. and Method 5004
Code	As device spec.
Seal test	Method 1014 (as necessary)
External visual	Method 2009
Form inspection lot	As MIL-M-38510
Select samples for conformance test	As Method 5005
Group A tests	Subgroups 1,2,3,4,5,6,7,8,9,10, and 11, as device spec. and Method 5005
Group B tests	Subgroups 2,3 and 5 (devices classified as static sensitive) as device spec. and Method 5005
Group C tests	Subgroup 1 as per device spec. and Method 5005 (generic data may be used if available)
Group D tests	Subgroups 1,2,3,4,5,6,7 and 8 as device spec. and Method 5005 (generic data may be used if available)
Prepare data package	
Inspect devices, pack and ship with data and C of C	As required

Conformance testing

MIL-STD-883C Class B Method 5005.11

Group A Electrical Tests

Subgroup	MIL-STD-883C Methods and Comments	LTPD	Sample Size
1	Static tests at +25°C	2	116
2	Static tests at maximum rated operating temperature	2	116
3	Static tests at minimum rated operating temperature	2	116
4	Dynamic tests at +25°C	2	116
5	Dynamic tests at maximum rated operating temperature	2	116
6	Dynamic tests at minimum rated operating temperature	2	116
7	Functional tests at +25°C	2	116
8	Functional tests at max. and min. operating temperatures	2	116
9	Switching tests at +25°C	2	116
10	Switching tests at maximum rated operating temperature	2	116
11	Switching tests at minimum rated operating temperature	2	116

All non-destructive. Performed on each inspection lot as per MIL-M-38510 3.1.3.8

MIL-STD-883C Class B Group B Electrical Tests

Subgroup	Test	Method	Sample Size	Destructive/ Non-destructive
2	(a) Resistance to solvents	2015	4	D
3	(a) Solderability	2022 or 2003	3	D
5	(a) Bond strength	2011	4	D

Performed on each inspection lot as per MIL-M-38510 3.1.3.8

MIL-STD-883C Class B Group C Electrical Tests

Subgroup	Test	Method	Sample Size	Destructive/ Non-destructive
1	(a) Steady state life test (b) End point electrical parameters	1005	45	ND

Generic test data may be used for Group C tests

MIL-STD-883C Notice 4 Page 3 Clause 17

'... Group C and D shall have been completed on date codes within 52 weeks **prior** to the date code of product being submitted for acceptance. Group C data shall be on a die in the same microcircuit **group**....with the same **material, design** and **process** and from the same **plant** as the die represented.'

MIL-M-38510F Page 5 Clause 3.1.3.13

'Microcircuit group. Microcircuits which are designed to perform the same type of basic **circuit function**....within a given **circuit technology** (e.g. ....ECL....Linear, Hybrid, MOS) which are designed for the same supply, bias and signal voltages and for input/output compatibility and which are fabricated by use of the same basic **die construction** and **metallization**; the same **die attach** method; and by use of bonding interconnects of the same size, material and attachment method.'

Conformance testing (continued)

MIL-STD-883C Class B Group D Electrical Tests

Subgroup	Test	Method	Sample Size	Destructive/ Non-destructive
1	(a) Physical dimensions	2016	15	ND
2	(a) Lead integrity	2010	15	D
	(b) Seal	1014	15	D
	(1) Fine			
	(2) Gross			
3	(a) Thermal shock	1011	15	D
	(b) Temperature cycling	1010		
	(c) Moisture resistance	1004		
	(d) Seal	1014		
	(1) Fine			
	(2) Gross			
	(e) Visual examination			
	(f) End point electrical parameters			
4	(a) Mechanical shock	2002	15	D
	(b) Vibration, variable frequency	2007		
	(c) Constant acceleration	2001		
	(d) Seal	1014		
	(1) Fine			
	(2) Gross			
	(e) Visual examination			
	(f) End point electrical parameters			
5	(a) Salt atmosphere	1009	15	D
	(b) Seal	1014		
	(1) Fine			
	(2) Gross			
	(c) Visual examination			
6	(a) Internal water vapour content	1018	5	D
7	(a) Adhesion of lead finish	2025	15	D
8	(a) Lid torque	2024	5	D

Generic test data may be used for Group D tests

MIL-STD-883C Notice 4 Page 3 Clause 17
'... Group C and D shall have been completed on date codes within 52 weeks **prior** to the date code of product being submitted for acceptance. Group D data shall be on the same package type....and from the same **plant** as the die represented.'
MIL-M-38510F Page 5 Clause 3.1.3.12
'Package type. A package type is a package which has the same **case outline, configuration**....(the physical shape of the case outline not including dimensions)...., **materials** (including bonding wire and die attach), **piece parts** (excluding preforms which differ only in size), and **assembly processes**.'

Packaging and coding

Lead finish

Devices will be supplied with the following lead finishes as standard:

Package Type	Lead Finish (MIL-M-38510 3.5.6.3.2)
Metal Can (CM) Sidebrazed Ceramic DIL (DC) Leadless Chip Carrier (LC)	Gold plate over Nickel plate
Ceramic DIL (DG)	Hot solder dip over Tin plate

ESD protection

GEC Plessey Semiconductors considers all devices to be sensitive to electrostatic discharge to varying degrees (but at least to category A). All units are therefore marked with the equilateral triangle ESD sensitivity indicator.

In addition, all devices are packaged and shipped in conductive material or packaged in anti-static material with an external field shielding barrier in accordance MIL-M-38510.

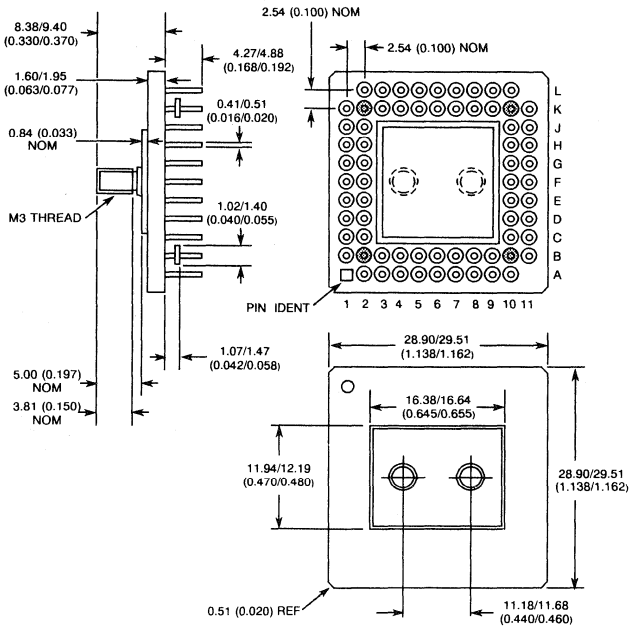
Device marking

All devices are marked with the following coding:

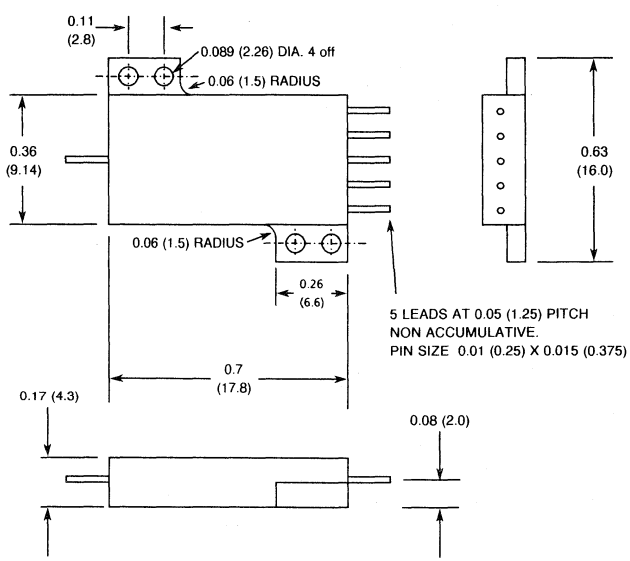
1. GPS logo or 'GPS' (manufacturer's identity).
2. ESD sensitivity indicator (equilateral triangle).
3. Date code (per MIL-M-38510).
4. Assembly lot identifier. Suffix letter added to date code indicating lot identity within production week.
5. Device type number - 'AC' indicating a MIL-STD-883C Class B compliant device.
6. Process/Assembly site identifier (two-letter code). Initial letter 'S' indicates GPS Swindon UK Wafer Process site. Second letter 'J' indicates GPS Swindon assembly site.
7. Pin 1 identifier. This may be either a package notch or dot for dual-in-line packages, gold corner for leadless chip carriers or tab for metal can packages.

Section 6
Package Outlines

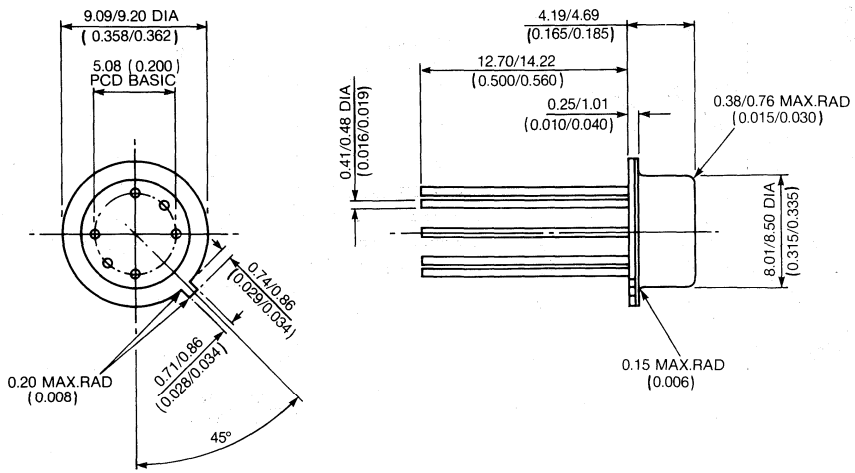
NOTE: On all package outlines, dimensions are shown thus: mm (in).



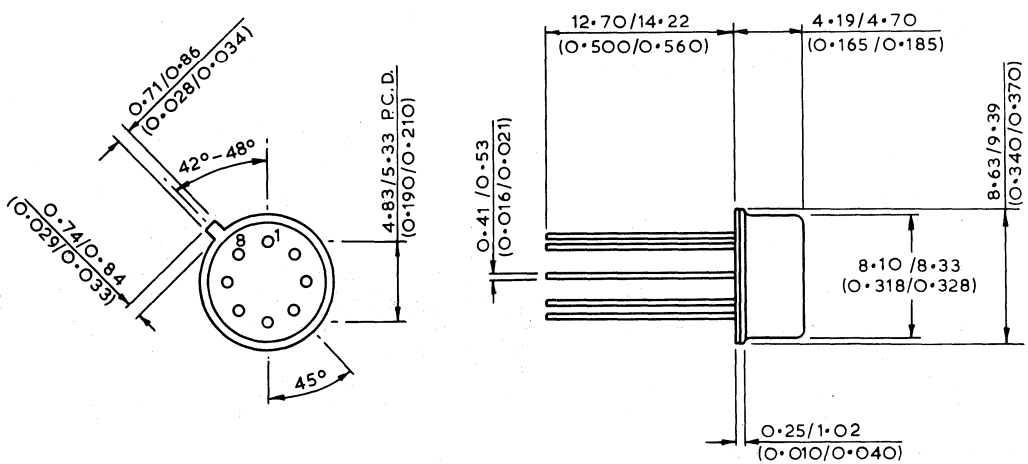
68-PIN PIN GRID ARRAY - AC68 (POWER)



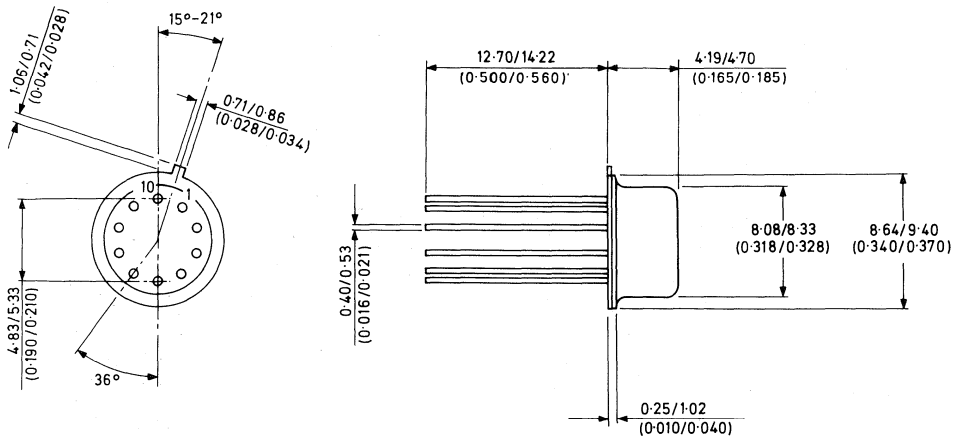
6-PIN METAL PACKAGE - BM6



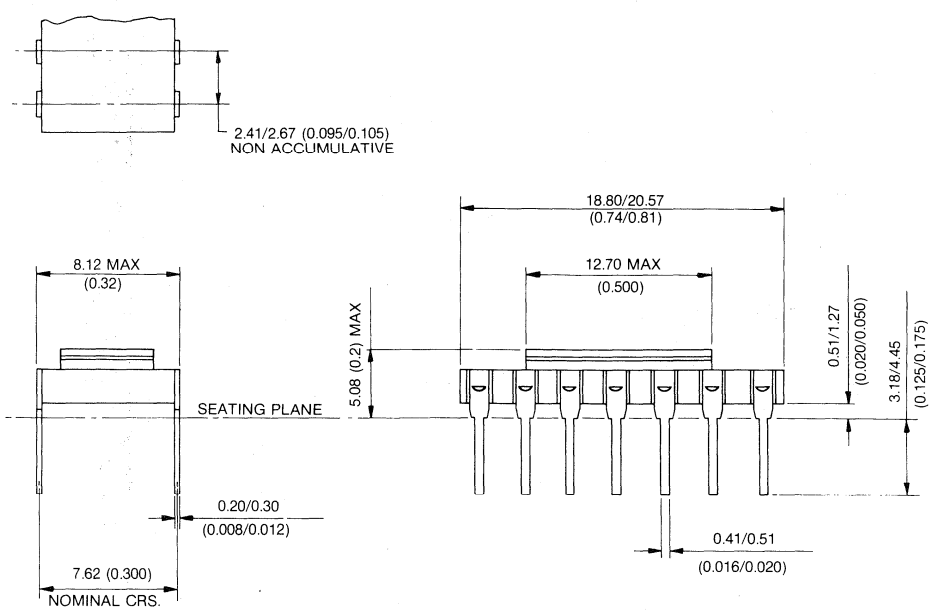
6-LEAD METAL CAN - CM6



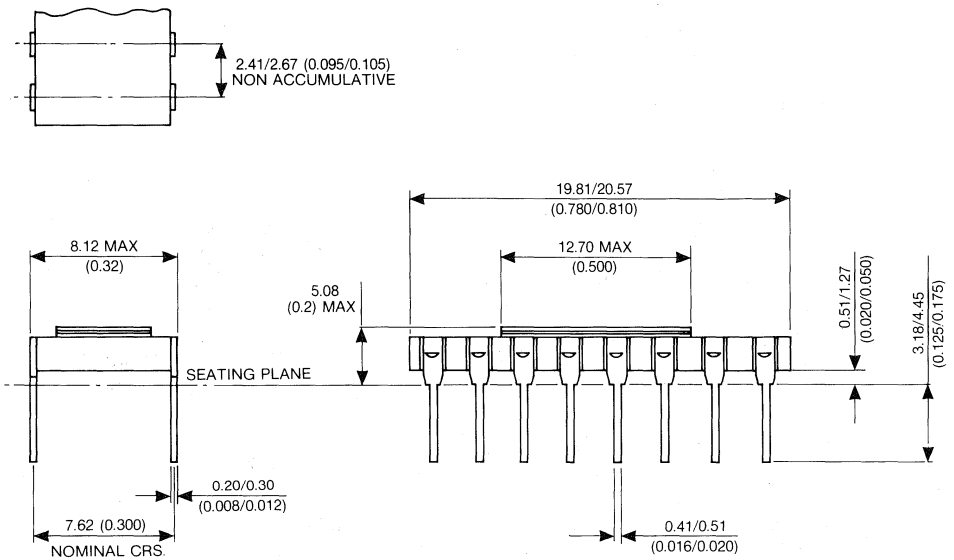
8-LEAD METAL CAN - CM8



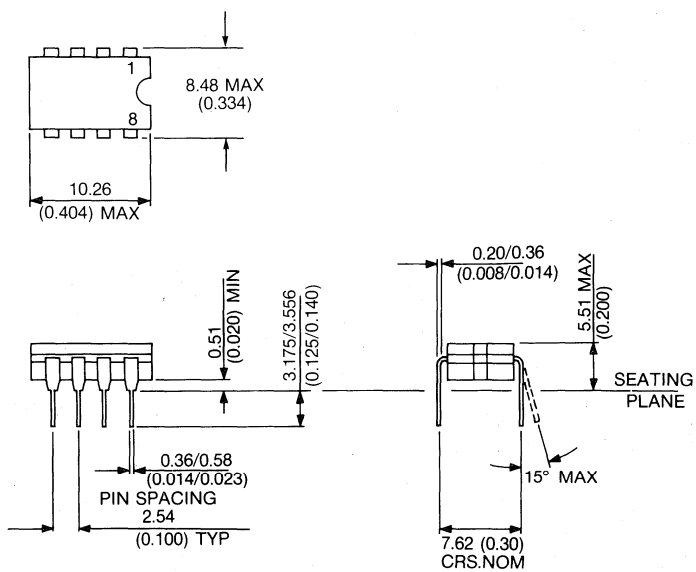
10-LEAD METAL CAN - CM10



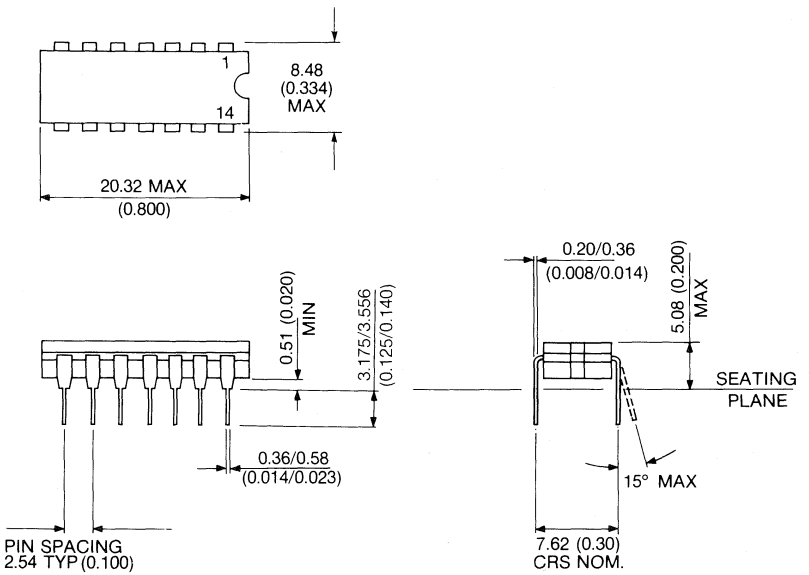
14-LEAD SIDEBRAZED CERAMIC DIL - DC14



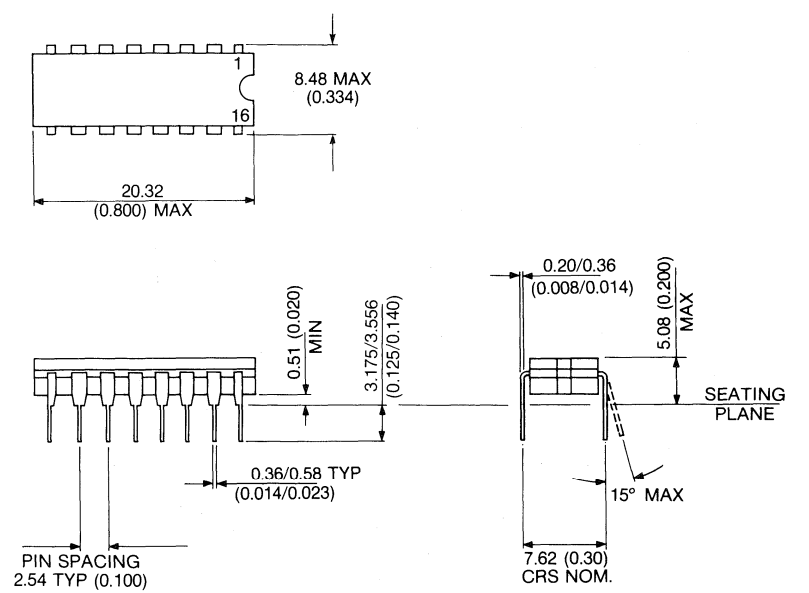
16-LEAD SIDEBRAZED CERAMIC DIL - DC16



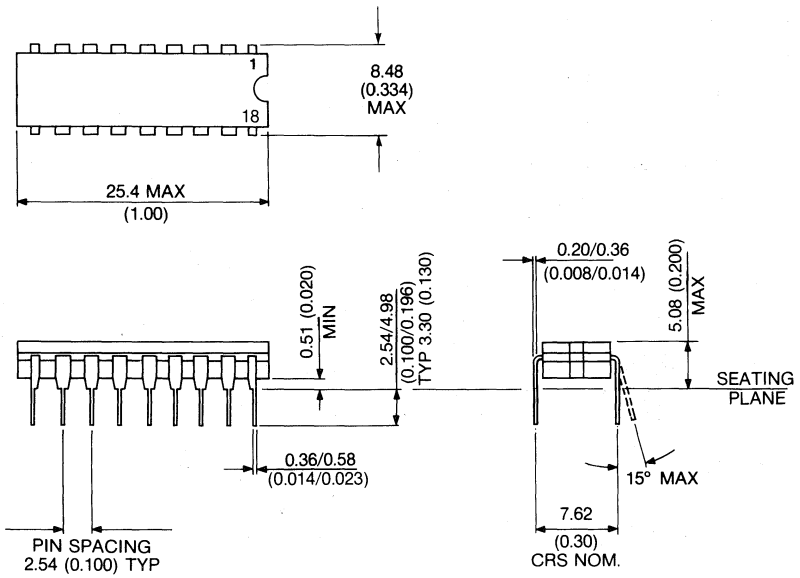
8-LEAD CERAMIC DIL - DG8



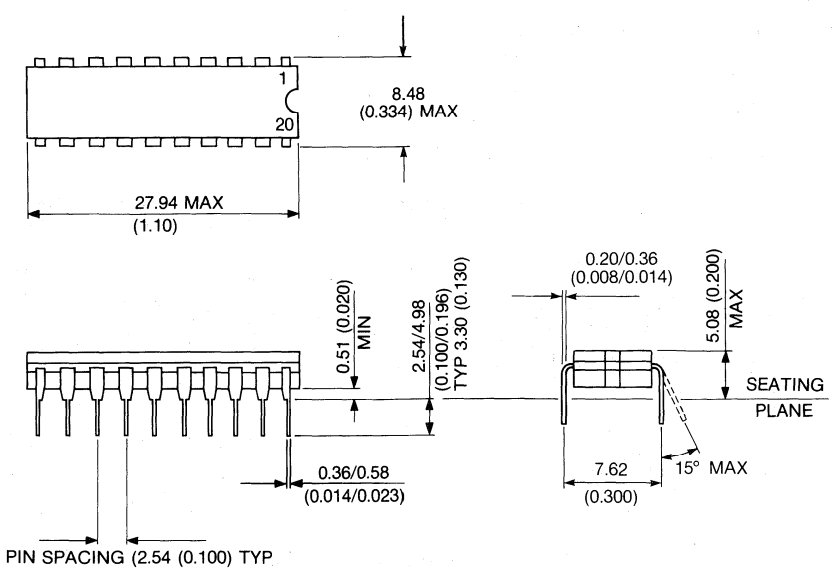
14-LEAD CERAMIC DIL - DG14



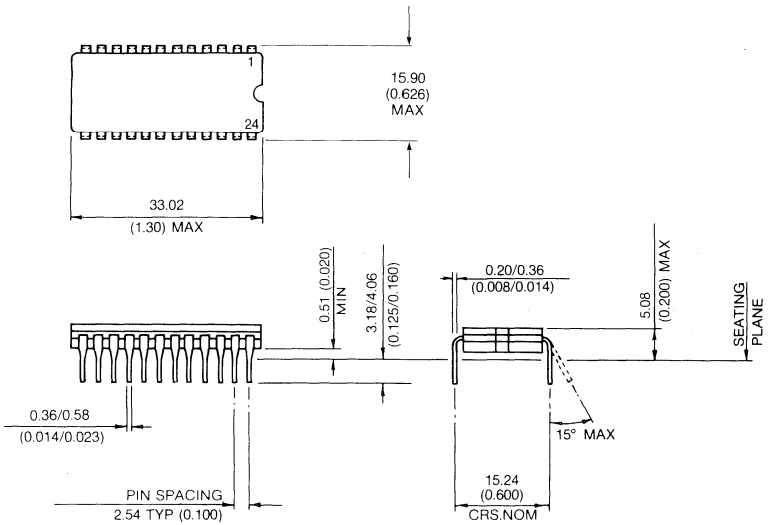
16-LEAD CERAMIC DIL - DG16



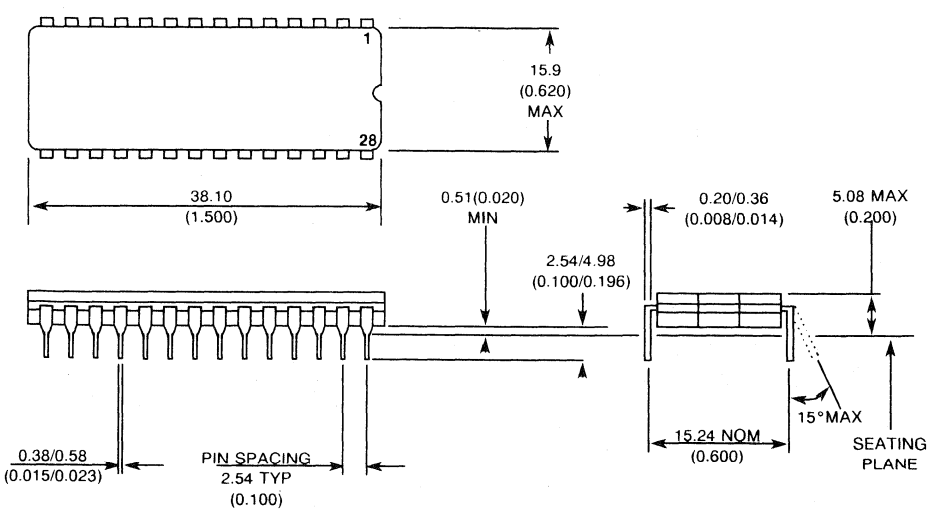
18-LEAD CERAMIC DIL - DG18



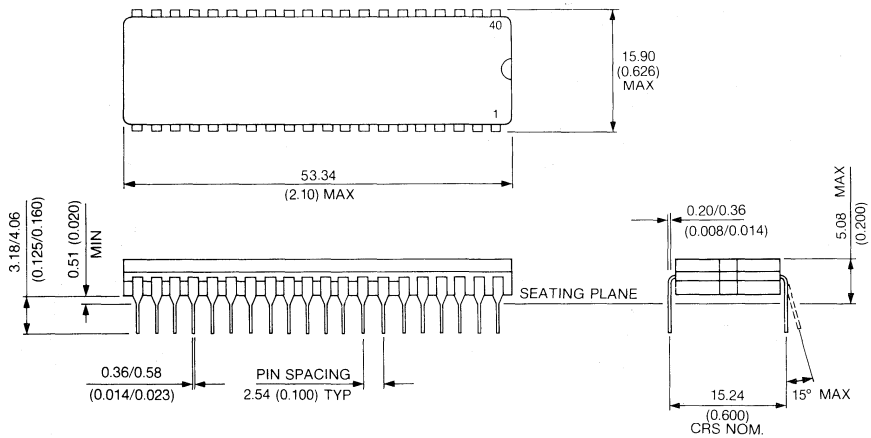
20-LEAD CERAMIC DIL - DG20



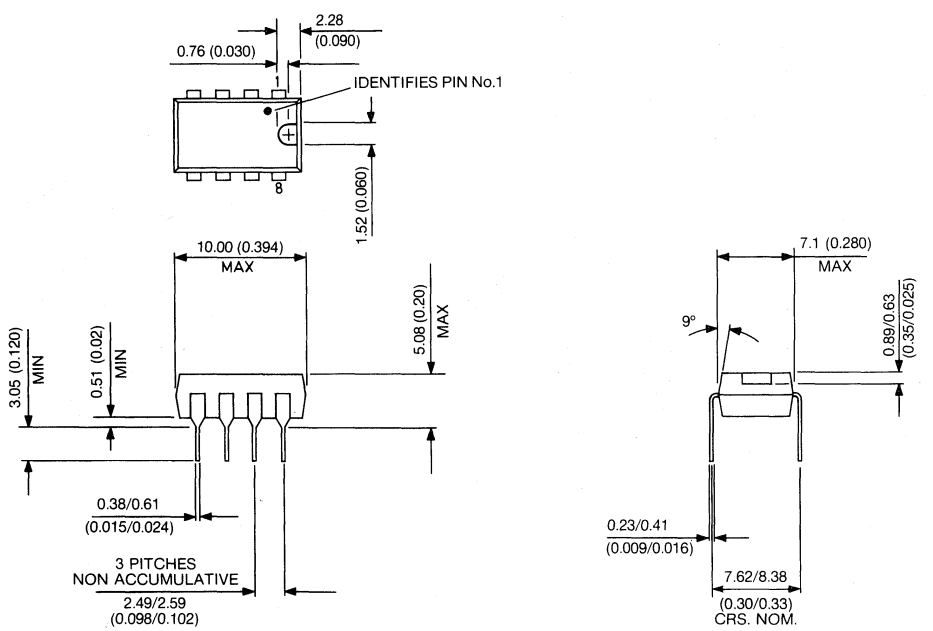
24 LEAD CERAMIC DIL
CERDIP - DG24



28-LEAD CERAMIC DIL- DG28



40-LEAD CERAMIC DIL CERDIP - DG40



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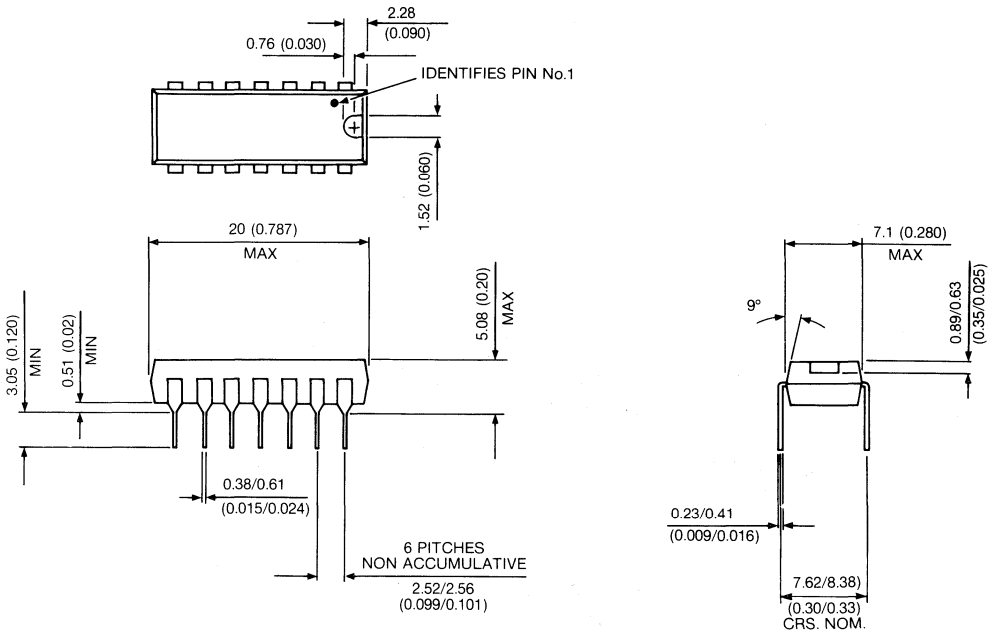

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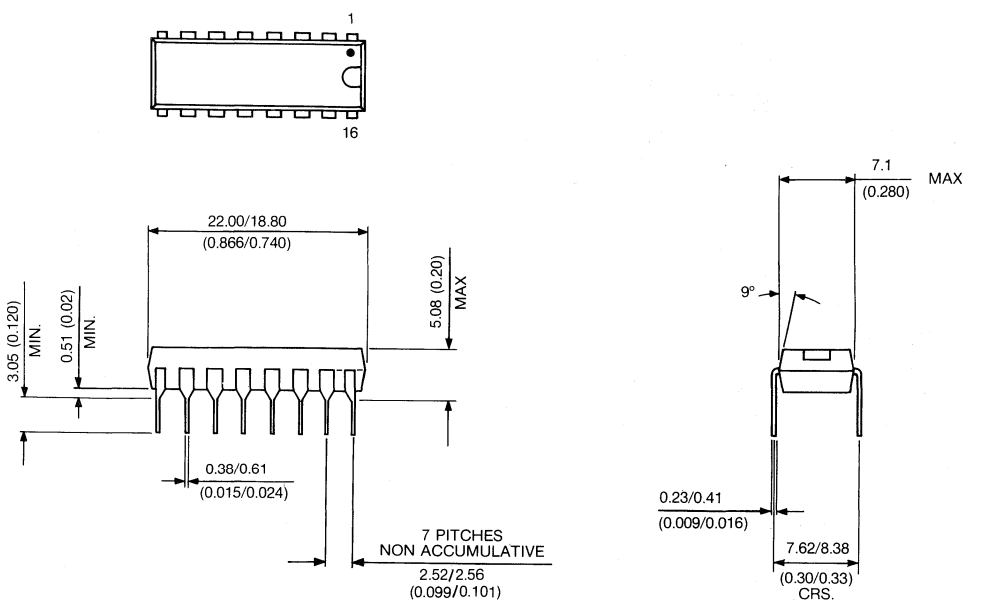

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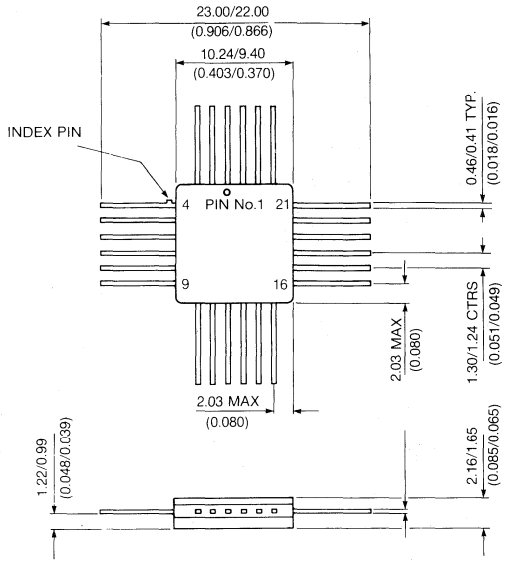

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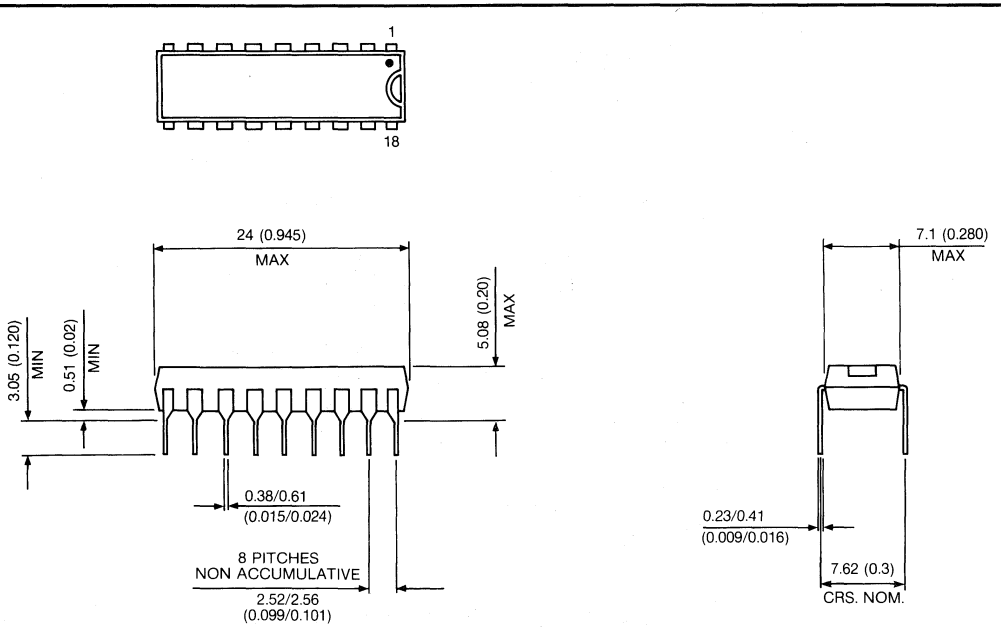

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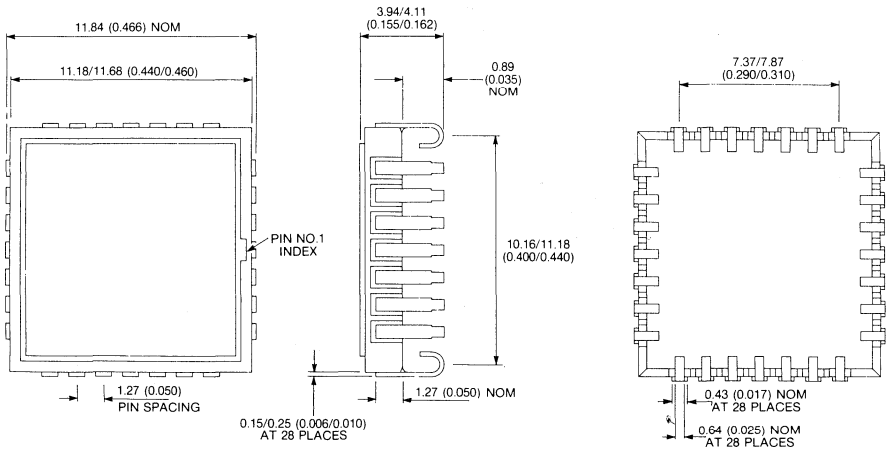

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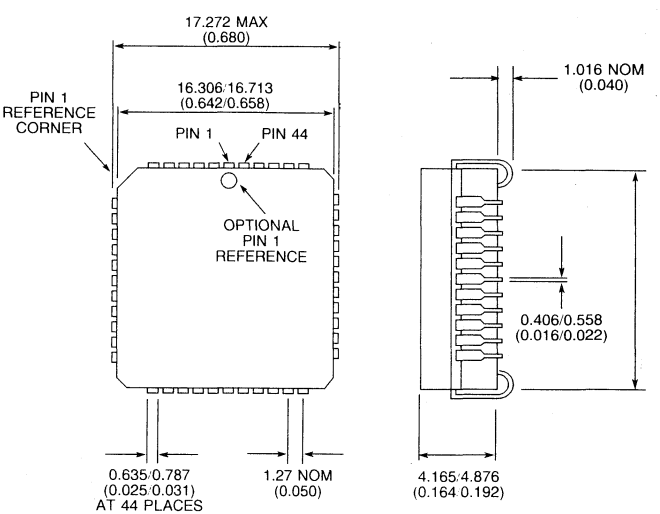

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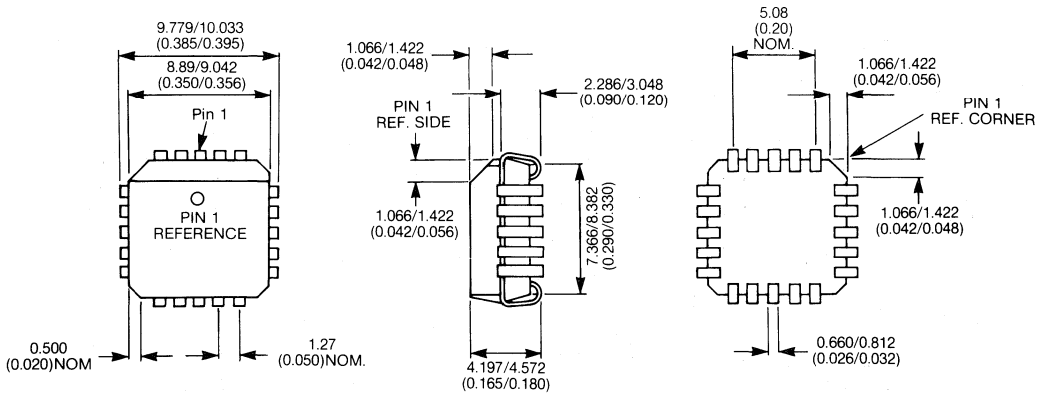

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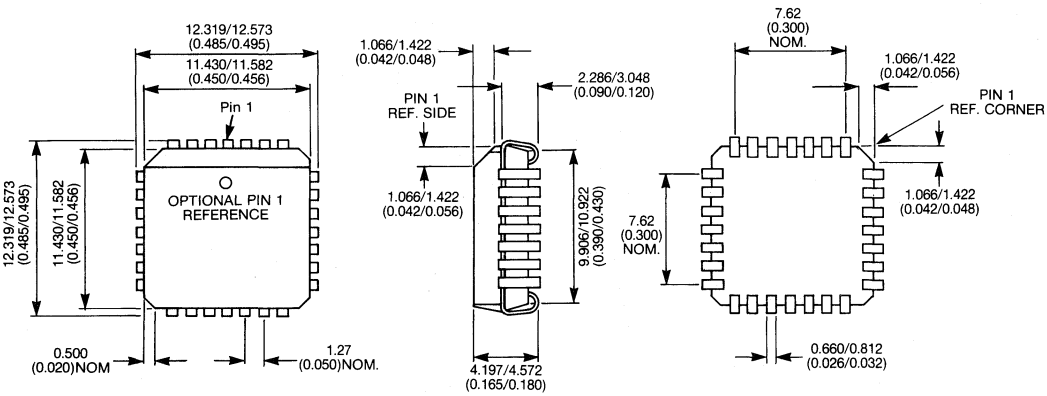

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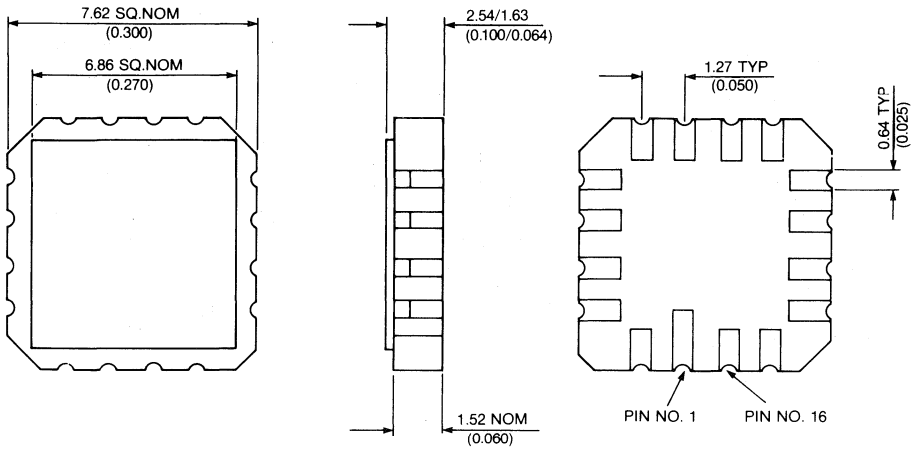

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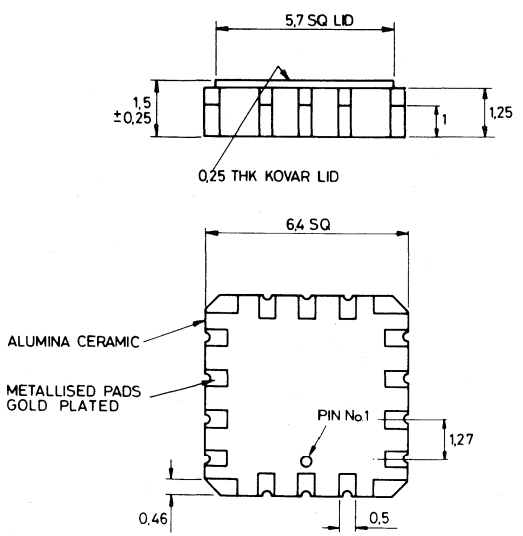

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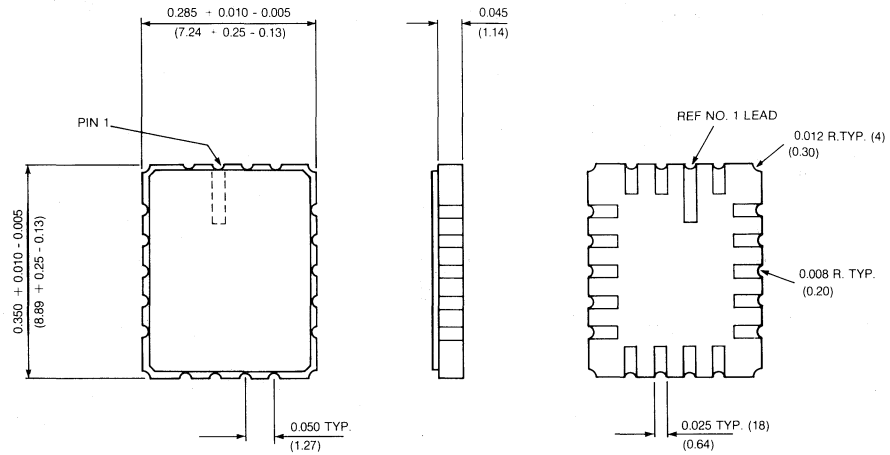

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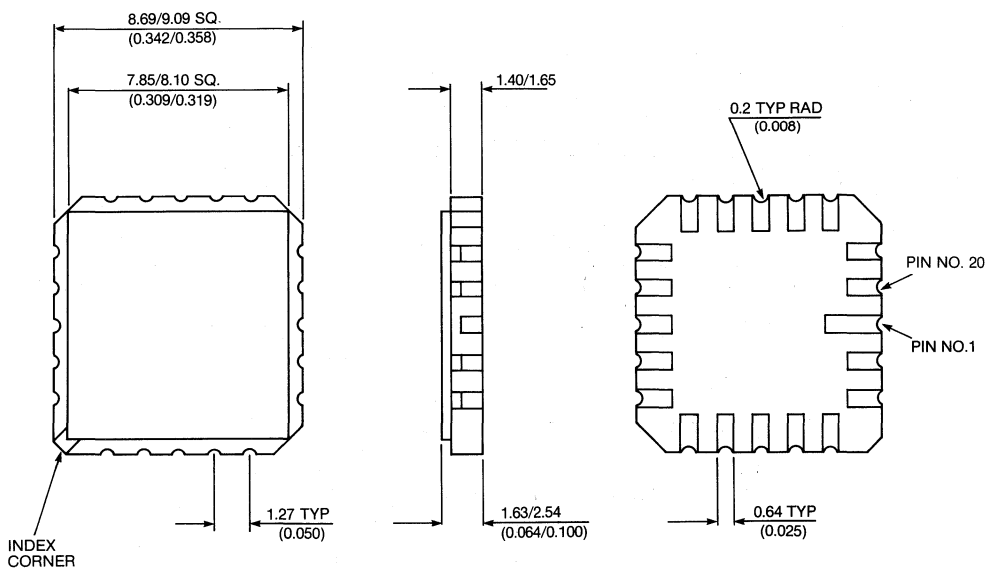

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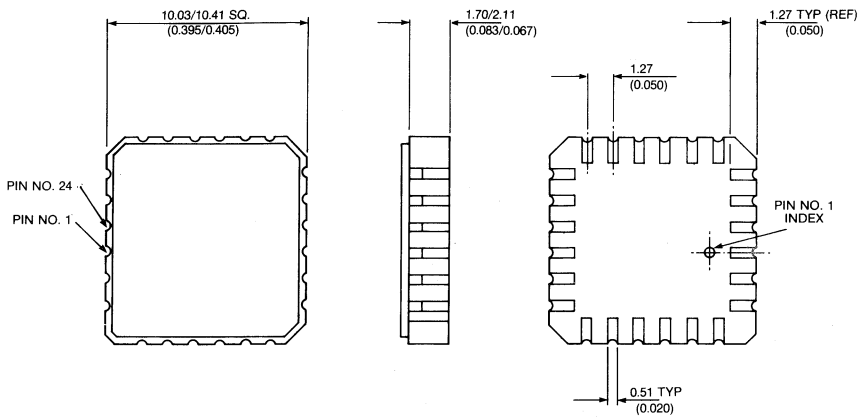

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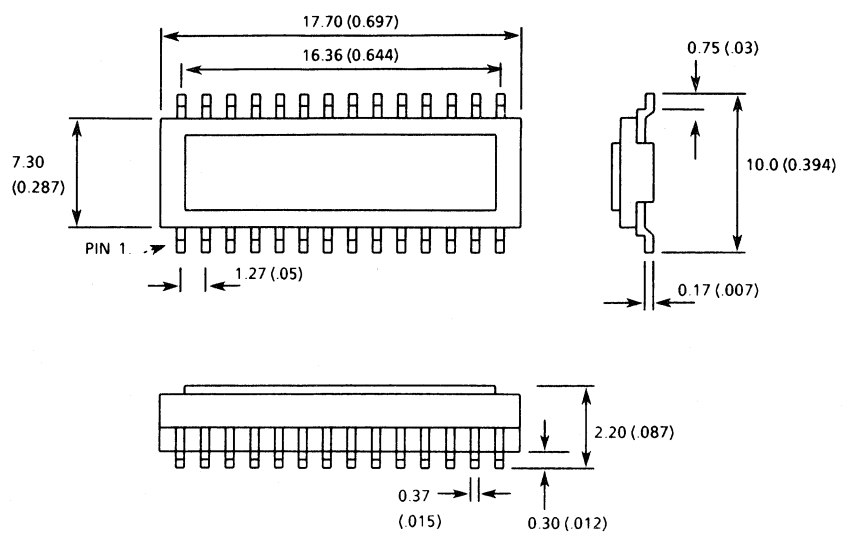

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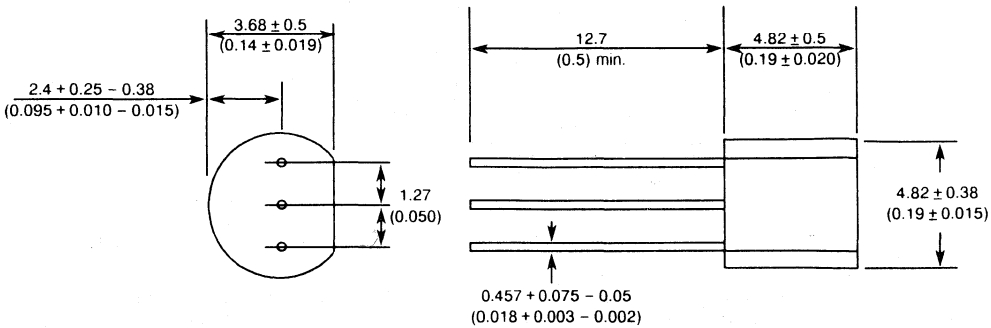

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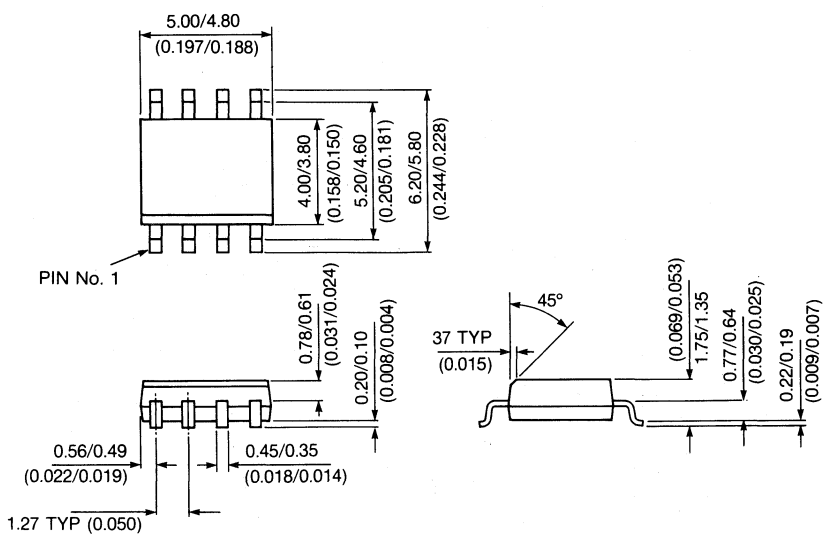

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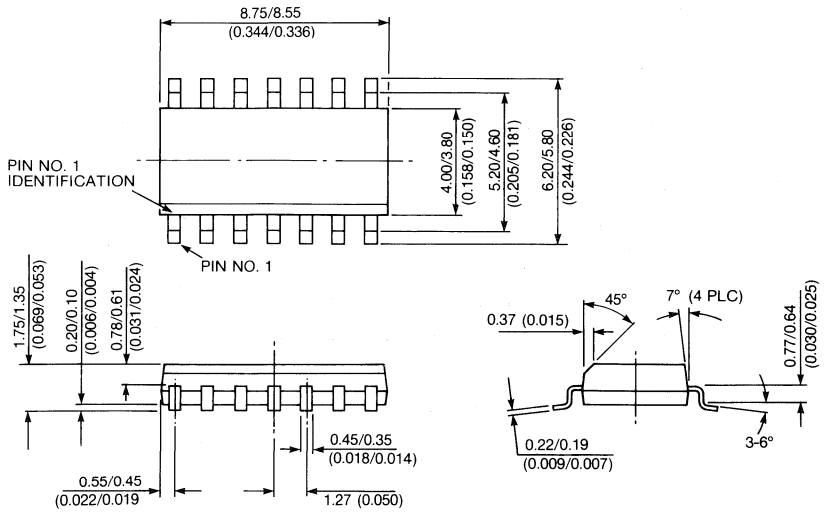

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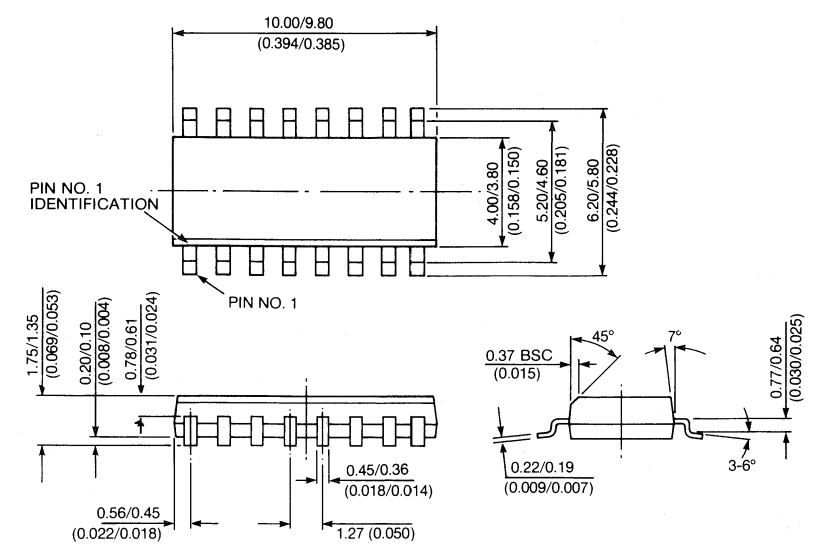

16-LEAD MINIATURE PLASTIC DIL - MP16

Section 7
Locations

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JAPAN	**Cornes & Company Ltd.,** Maruzen Building, 2-3-10 Nihonbashi, Chuo-ku. Tokyo 103. Tel: 3 272 5771. Tx: 24874. Fax: 3 271 1479. **Cornes & Company Ltd.,** 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 6 532 1012.Tx: 525-4496. Fax: 6 541-8850. **Microtek Inc.,** Itoh Bldg, 7-9-17 Nishishinijuku. Tokyo 160. Tel: 3 371 1811. Tx: 27466. Fax: 3 369 5623.
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Norway	**Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, 0596 Oslo. Tel: 2 64 11 50. Tx: 71963 Fax: 2 643443.
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SPAIN	**Anatronic SA,** Avda de Valladolid 27, 28008 Madrid. Tel: 91 542 4455. Tx: 47397. Fax: 91 2486975.
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THAILAND	**Westech Electronics Co. Ltd,** 77/113 Moo Ban Kitikorn, Ladprao Soi 3, Ladprao Road, Ladyao, Jatujak, Bangkok 10900. Thailand. Tel: 2 5125531. Fax: 2 2365949.
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Clermont-Ferrand, 2 bis, Avenue Fonmaure, 63400 Chamalieres. Tel: 73 36 71 41 Tx: 990928.
Marseille, Z.A. Artizanord 11, 13015 Marseille. Tel: 91 03 12 12. Tx: 441313.
Toulouse, 78, Chemin Lanusse, 31200 Toulouse. Tel: 61 26 14 10. Tx: 520897.

CGE Composants SA:

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Tel: 08136 7092. Tx: 5270505. Fax: 08136 7398.

AS Electronic Vertriebs GmbH, In den Gaerten 2, 6380 Bad Homburg 6. Tel: 06172 458931. Fax: 06172 42000.

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Micronetics GmbH, Weil de Staedter Str. 45, 7253 Renningen 1. Tel: 071 59 6019. Tx: 724708. Fax: 071 59 5119.

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Elbatex AG., Hardstr 72, CH-5430 Wettingen. Tel: 41 56 27 51 11. Tx: 826300. Fax: 41 56 27 19 24.

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Gothic Crellon Ltd., 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY.
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Gothic Crellon Ltd., P.O.Box 301, Elizabeth House, 22 Suffolk Street, Queensway, Birmingham B1 1LZ.
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Tel: (0895) 445522. Tx: 21958. Fax: (0895) 422044.

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Tel: 0279 626777. Tlx: 818801. Fax: 0279 441687.

2001 Electronic Components Ltd, Woolners Way, Stevenage, Herts SG1 3AJ.
Tel: 0438 742001. Tlx: 827701. Fax: 0438 742002.

Unitel Ltd., Unitel House. Fishers Green Road, Stevenage, Herts.
Tel: (0438) 312393. Tx: 825637. Fax: (0438) 318711.

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(To countries other than those listed) **GEC Plessey Semiconductors Ltd.,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts, UK SN2 5AY. Tel: (0793) 518510. Tx: 444410. Fax: (0793) 518582.

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Microstar Technologies, 7050 Bramelea Rd., #27A Mississaugo, Ontario L5SITI Canada. Tel: (416) 671-8111
COLORADO **Analog Solutions,** 5484 White Place, Boulder, CO 80303. Tel: (303) 442-5083.
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FLORIDA 668 N. Orlando Ave., Suite 1015 B, Maitland. FL 32751. Tel: (407) 539-1700. Fax: (407) 539-0055.
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GEC PLESSEY

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